SN74LS259

8-Bit Addressable Latch

The SN74LS259 is a high-speed 8-Bit Addressable Latch designed for general purpose storage applications in digital systems. It is a multifunctional device capable of storing single line data in eight addressable latches, and also a 1-of-8 decoder and demultiplexer with active HIGH outputs. The device also incorporates an active LOW common Clear for resetting all latches, as well as, an active LOW Enable.

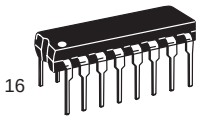
- Serial-to-Parallel Conversion
- Eight Bits of Storage With Output of Each Bit Available
- Random (Addressable) Data Entry
- Active High Demultiplexing or Decoding Capability
- Easily Expandable
- Common Clear

GUARANTEED OPERATING RANGES

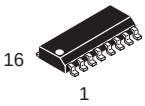
Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	4.75	5.0	5.25	V
T_A	Operating Ambient Temperature Range	0	25	70	°C
I_{OH}	Output Current – High			–0.4	mA
I_{OL}	Output Current – Low			8.0	mA

ON Semiconductor
Formerly a Division of Motorola
http://onsemi.com

LOW
POWER
SCHOTTKY



PLASTIC
N SUFFIX
CASE 648

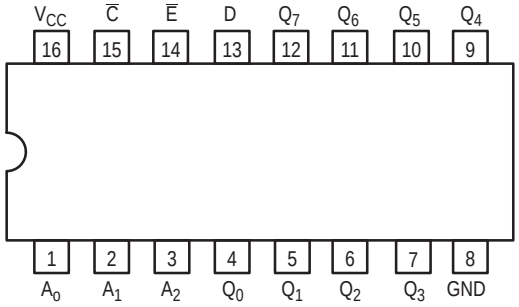


SOIC
D SUFFIX
CASE 751B

ORDERING INFORMATION

Device	Package	Shipping
SN74LS259N	16 Pin DIP	2000 Units/Box
SN74LS259D	16 Pin	2500/Tape & Reel

CONNECTION DIAGRAM DIP (TOP VIEW)

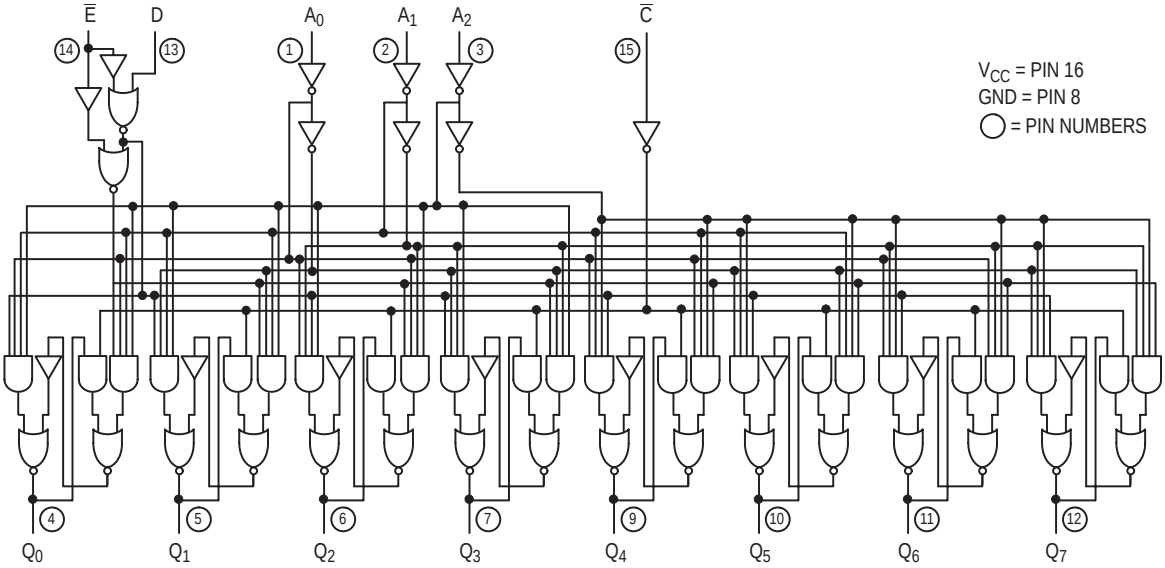


PIN NAMES		**LOADING** (Note a) HIGH	LOW
A_0, A_1, A_2	Address Inputs	0.5 U.L.	0.25 U.L.
D	Data Input	0.5 U.L.	0.25 U.L.
$\overline{E}$	Enable (Active LOW) Input	1.0 U.L.	0.5 U.L.
$\overline{C}$	Clear (Active LOW) Input	0.5 U.L.	0.25 U.L.
$Q_0 - Q_7$	Parallel Latch Outputs	10 U.L.	5 U.L.

NOTES:

a) 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.

LOGIC DIAGRAM



FUNCTIONAL DESCRIPTION

The SN74LS259 has four modes of operation as shown in the mode selection table. In the addressable latch mode, data on the Data line (D) is written into the addressed latch.The addressed latch will follow the data input with all non-addressed latches remaining in their previous states. In the memory mode, all latches remain in their previous state and are unaffected by the Data or Address inputs.

In the one-of-eight decoding or demultiplexing mode, the addressed output will follow the state of the D input with all other inputs in the LOW state. In the clear mode all outputs are LOW and unaffected by the address and data inputs.

When operating the SN74LS259 as an addressable latch, changing more then one bit of the address could impose a transient wrong address. Therefore, this should only be done while in the memory mode.

The truth table below summarizes the operations.

MODE SELECTION

$\overline{E}$	$\overline{C}$	MODE
L	H	Addressable Latch
H	H	Memory
L	L	Active HIGH Eight-Channel Demultiplexer
H	L	Clear

TRUTH TABLE

						PRESENT OUTPUT STATES								
$\overline{C}$	$\overline{E}$	D	A_0	A_1	A_2	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	MODE
L	H	X	X	X	X	L	L	L	L	L	L	L	L	Clear
L	L	L	L	L	L	L	L	L	L	L	L	L	L	Demultiplex
L	L	H	L	L	L	H	L	L	L	L	L	L	L	
L	L	L	H	L	L	L	L	L	L	L	L	L	L	
L	L	H	H	L	L	L	H	L	L	L	L	L	L	
•	•	•		•					•					
•	•	•		•					•					
•	•	•		•					•					
•	•	•		•					•					
•	•	•		•					•					
L	L	H	H	H	H	L	L	L	L	L	L	L	H	
H	H	X	X	X	X	Q_{N-1} →								Memory
H	I	I	L	L	L	L	Q_{N-1}	Q_{N-1}	Q_{N-1} →					Addressable
H	L	H	L	L	L	H	Q_{N-1}	Q_{N-1} →						Latch
H	L	L	H	L	L	Q_{N-1}	L	Q_{N-1} →						
H	L	H	H	L	L	Q_{N-1}	H	Q_{N-1} →						
•	•	•		•					•					
•	•	•		•					•					
•	•	•		•					•					
•	•	•		•					•					
•	•	•		•					•					
H	L	L	H	H	H	Q_{N-1} →						Q_{N-1}	L	
H	L	H	H	H	H	Q_{N-1} →						Q_{N-1}	H	

X = Don't Care Condition
L = LOW Voltage Level
H = HIGH Voltage Level
Q_{N-1} = Previous Output State

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V_{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs	
V_{IK}	Input Clamp Diode Voltage		−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	2.7	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
V_{OL}	Output LOW Voltage		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
			0.35	0.5	V	I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current			20	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
				0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current			−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Short Circuit Current (Note 1)	−20		−100	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current			36	mA	V_{CC} = MAX	

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

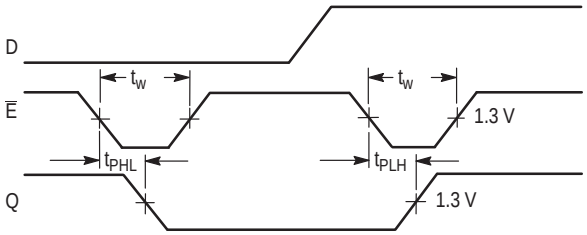
AC CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t_{PLH} t_{PHL}	Turn-Off Delay, Enable to Output Turn-On Delay, Enable to Output		22 15	35 24	ns ns	C_L = 15 pF
t_{PLH} t_{PHL}	Turn-Off Delay, Data to Output Turn-On Delay, Data to Output		20 13	32 21	ns ns	
t_{PLH} t_{PHL}	Turn-Off Delay, Address to Output Turn-On Delay, Address to Output		24 18	38 29	ns ns	
t_{PHL}	Turn-On Delay, Clear to Output		17	27	ns	

AC SET-UP REQUIREMENTS (T_A = 25°C, V_{CC} = 5.0 V)

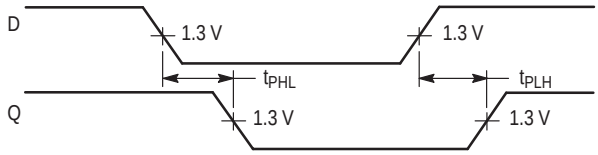
Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
t_s	Input Setup Time	20			ns
t_W	Pulse Width, Clear or Enable	15			ns
t_h	Hold Time, Data	5.0			ns
t_h	Hold Time, Address	20			ns

AC WAVEFORMS



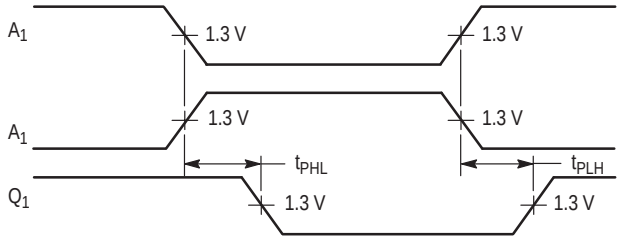
OTHER CONDITIONS: $\overline{C}$ = H, A = STABLE

Figure 1. Turn-on and Turn-off Delays, Enable To Output and Enable Pulse Width



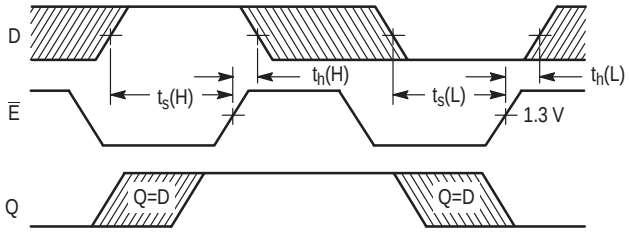
OTHER CONDITIONS: $\overline{E}$ = L, $\overline{C}$ = H, A = STABLE

Figure 2. Turn-on and Turn-off Delays, Data to Output



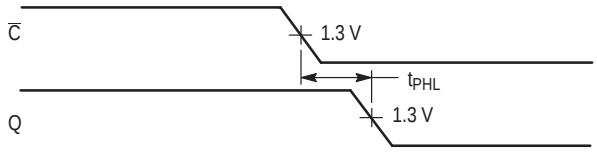
OTHER CONDITIONS: $\overline{E}$ = L, $\overline{C}$ = L, D = H

Figure 3. Turn-on and Turn-off Delays, Address to Output



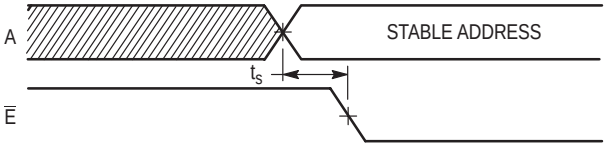
OTHER CONDITIONS: $\overline{C}$ = H, A = STABLE

Figure 4. Setup and Hold Time, Data to Enable



OTHER CONDITIONS: $\overline{E}$ = H

Figure 5. Turn-on Delay, Clear to Output



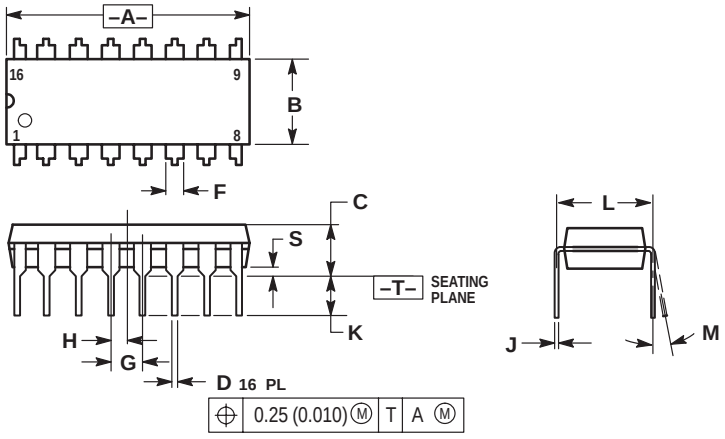
OTHER CONDITIONS: $\overline{C}$ = H

Figure 6. Setup Time, Address to Enable (See Notes 1 and 2)

NOTES:
1. The Address to Enable Setup Time is the time before the HIGH-to-LOW Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.
2. The shaded areas indicate when the inputs are permitted to change for predictable output performance.

PACKAGE DIMENSIONS

N SUFFIX
PLASTIC PACKAGE
CASE 648–08
ISSUE R

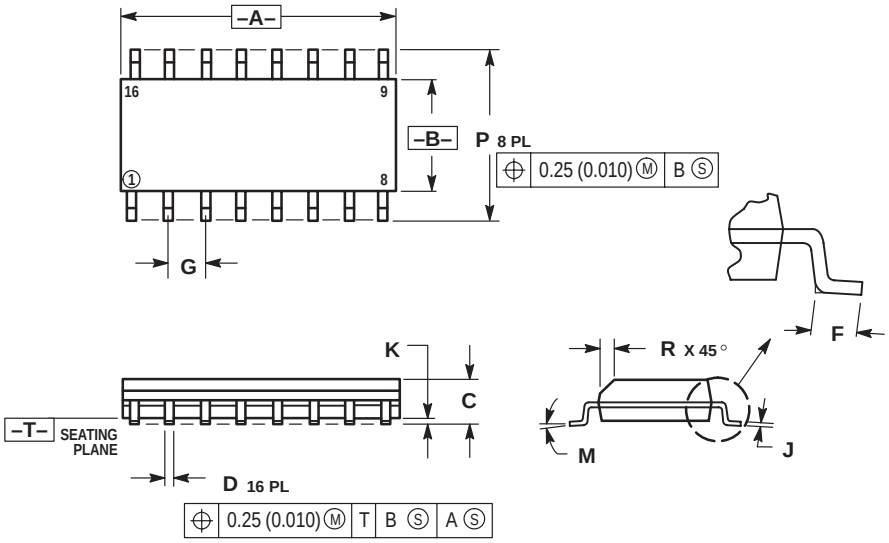


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0 °	10 °	0 °	10 °
S	0.020	0.040	0.51	1.01

PACKAGE DIMENSIONS

D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751B–05
ISSUE J



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

PUBLICATION ORDERING INFORMATION

North America Literature Fulfillment:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303–675–2175 or 800–344–3860 Toll Free USA/Canada
Fax: 303–675–2176 or 800–344–3867 Toll Free USA/Canada
Email: ONlit@hibbertco.com

N. American Technical Support: 800–282–9855 Toll Free USA/Canada

EUROPE: LDC for ON Semiconductor – European Support
German **Phone:** (+1) 303–308–7140 (M–F 2:30pm to 5:00pm Munich Time)
Email: ONlit–german@hibbertco.com
French **Phone:** (+1) 303–308–7141 (M–F 2:30pm to 5:00pm Toulouse Time)
Email: ONlit–french@hibbertco.com
English **Phone:** (+1) 303–308–7142 (M–F 1:30pm to 5:00pm UK Time)
Email: ONlit@hibbertco.com

ASIA/PACIFIC: LDC for ON Semiconductor – Asia Support
Phone: 303–675–2121 (Tue–Fri 9:00am to 1:00pm, Hong Kong Time)
Toll Free from Hong Kong 800–4422–3781
Email: ONlit–asia@hibbertco.com

JAPAN: ON Semiconductor, Japan Customer Focus Center
4–32–1 Nishi–Gotanda, Shinagawa–ku, Tokyo, Japan 141–8549
Phone: 81–3–5487–8345
Email: r14153@onsemi.com

Fax Response Line: 303–675–2167
800–344–3810 Toll Free USA/Canada

ON Semiconductor Website: http://onsemi.com

For additional information, please contact your local
Sales Representative.