

NDF0610 / NDS0610

P-Channel Enhancement Mode Field Effect Transistor

General Description

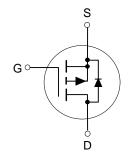
These P-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process has been designed to minimize on-state resistance, provide rugged and reliable performance and fast switching. They can be used, with a minimum of effort, in most applications requiring up to 180mA DC and can deliver pulsed currents up to 1A. This product is particularly suited to low voltage applications requiring a low current high side switch.

Features

- -0.18 and -0.12A, -60V. $R_{DS(ON)} = 10\Omega$
- Voltage controlled p-channel small signal switch
- High density cell design for low R_{DS(ON)}
- TO-92 and SOT-23 packages for both through hole and surface mount applications
- High saturation current







Absolute Maximum Ratings

T_A = 25°C unless otherwise noted

Symbol	Parameter	NDF0610	NDS0610	Units		
V _{DSS}	Drain-Source Voltage	-6	V			
V_{DGR}	Drain-Gate Voltage ($R_{\rm GS} \leq 1 \ {\rm M}\Omega$)	-6	0	V		
V _{GSS}	Gate-Source Voltage - Continuous	±2	20	V		
	- Nonrepetitive (t _p < 50 µs)	±3	V			
I _D	Drain Current - Continuous	-0.18	-0.12	А		
	- Pulsed	-1				
P _D	Maximum Power Dissipation T _A = 25°C	0.8	0.36	W		
	Derate above 25°C	5	2.9	mW/°C		
T_{J},T_{STG}	Operating and Storage Temperature Range	-55 to	°C			
T _L	Maximum lead temperature for soldering purposes, 1/16" from case for 10 seconds	30	°C			
THERMA	L CHARACTERISTICS					
R _{0JA}	Thermal Resistance, Junction-to-Ambient	200	350	°C/W		

Symbol	Parameter	Conditions		Min	Тур	Max	Units
OFF CHA	ARACTERISTICS	-		<u>I</u>	1		·L
3V _{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_{D} = -10 \mu\text{A}$		-60			V
DSS	Zero Gate Voltage Drain Current	$V_{DS} = -48 \text{ V}, V_{GS} = 0 \text{ V}$				-1	μA
			T _J = 125°C			-200	μA
GSSF	Gate - Body Leakage, Forward	$V_{gs} = 20 \text{ V}, V_{ps} = 0 \text{ V}$				10	nA
GSSR	Gate - Body Leakage, Reverse	$V_{gs} = -20 \text{ V}, V_{DS} = 0 \text{ V}$				-10	nA
ON CHAI	RACTERISTICS (Note 1)	<u>.</u>		•			
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = -1$ mA		-1	-2.4	-3.5	V
			T _J = 125°C	-0.6	-2.1	-3.2	
R _{DS(ON)}	Static Drain-Source On-Resistance	$V_{GS} = -10 \text{ V}, I_{D} = -0.5 \text{ A}$	•		3.6	10	Ω
			T _J = 125°C		5.9	16	
		$V_{gs} = -4.5 \text{ V}, I_{D} = -0.25 \text{ A}$			5.2	20	1
			T _J = 125°C		7.9	30	
I _{D(on)}	On-State Drain Current	$V_{GS} = -10 \text{ V}, V_{DS} = -10 \text{ V}$	•	-0.6	-1.6		Α
		$V_{GS} = -4.5 \text{ V}, V_{DS} = -10 \text{ V}$		-0.35			
FS	Forward Transconductance	$V_{DS} = -10 \text{ V}, I_{D} = -0.1 \text{ A}$		70	170		mS
OYNAMIC	CCHARACTERISTICS	·					
Siss	Input Capacitance	$V_{DS} = -25 \text{ V}, \ V_{GS} = 0 \text{ V},$			40	60	pF
Coss	Output Capacitance	f = 1.0 MHz			11	25	pF
C _{rss}	Reverse Transfer Capacitance			3.2	5	pF	
	NG CHARACTERISTICS (Note 1)						
D(on)	Turn - On Delay Time	$V_{DD} = -25 \text{ V}, I_D = -0.18 \text{ A},$			7	10	nS
r	Turn - On Rise Time	$V_{GS} = -10 \text{ V}, R_{GEN} = 25 \Omega$			5	15	nS
D(off)	Turn - Off Delay Time				13	15	nS
f	Turn - Off Fall Time				10	20	nS
Q_g	Total Gate Charge	V _{DS} = -48 V,			1.43		nC
\mathbf{Q}_{gs}	Gate-Source Charge	$I_D = -0.5 \text{ A}, V_{GS} = -10 \text{ V}$			0.6		nC
Q_{qd}	Gate-Drain Charge			0.25		nC	
	DURCE DIODE CHARACTERISTICS			I	<u> </u>		1
s	Maximum Continuous Source Current					-0.18	А
SM	Maximum Pulse Source Current (Note 1)					-1	Α
/ _{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_{S} = -0.5 \text{ A}$			-1.2	-1.5	V
		(Note 1)		-0.98	-1.3	1	
rr	Reverse Recovery Time	$V_{GS} = 0 \text{ V}, I_{S} = -0.5 \text{ A},$ $dI_{F}/dt = 100 \text{ A/}\mu\text{s}$	•		40		ns
	Reverse Recovery Current	— dl _F /dt = 100 A/μs			2.8		Α

Note: 1. Pulse Test: Pulse Width \leq 300 μ s, Duty Cycle \leq 2.0%.

Typical Electrical Characteristics

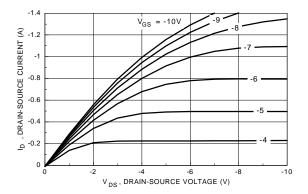


Figure 1. On-Region Characteristics

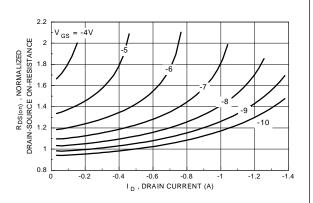


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current

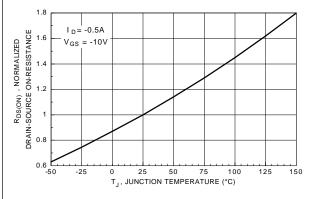


Figure 3. On-Resistance Variation with Temperature

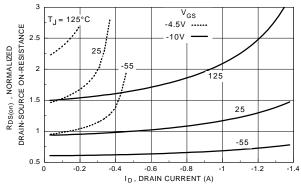


Figure 4. On-Resistance Variation with Drain Current and Temperature

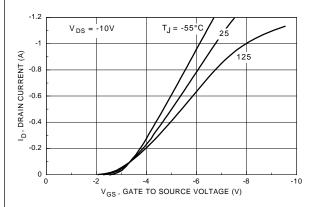


Figure 5. Transfer Characteristics

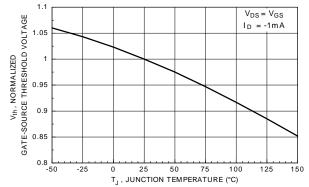


Figure 6. Gate Threshold Variation with Temperature

Typical Electrical Characteristics (continued)

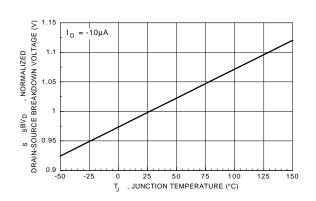


Figure 7. Breakdown Voltage Variation with Temperature

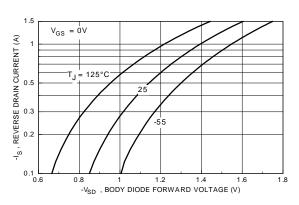


Figure 8. Body Diode Forward Voltage
Variation with Current and Temperature

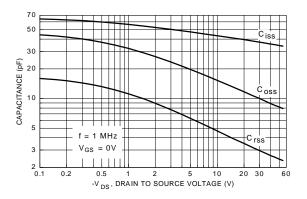


Figure 9. Capacitance Characteristics

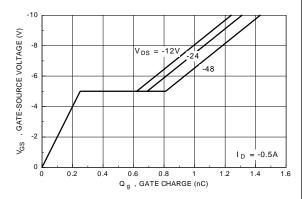


Figure 10. Gate Charge Characteristics

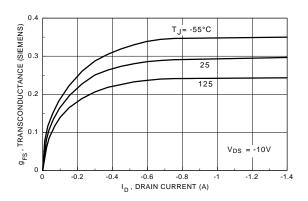


Figure 11. Transconductance Variation with Drain Current and Temperature

Typical Electrical Characteristics (continued)

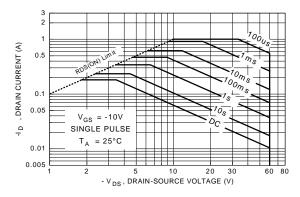


Figure 12. NDF0610 (TO-92)

Maximum Safe Operating Area

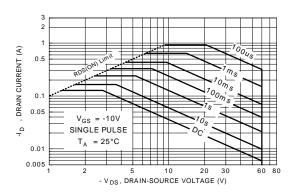


Figure 13. NDS0610 (SOT-23) Maximum Safe Operating Area

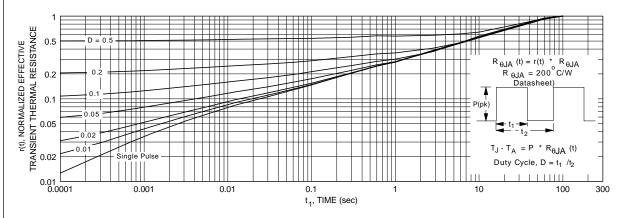


Figure 14. NDF0610 (TO-92) Transient Thermal Response Curve.

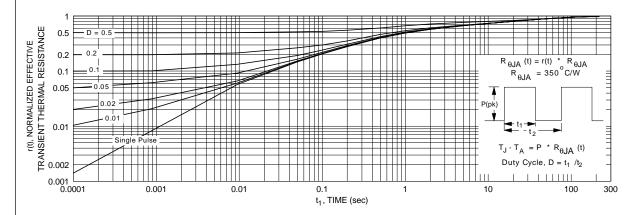
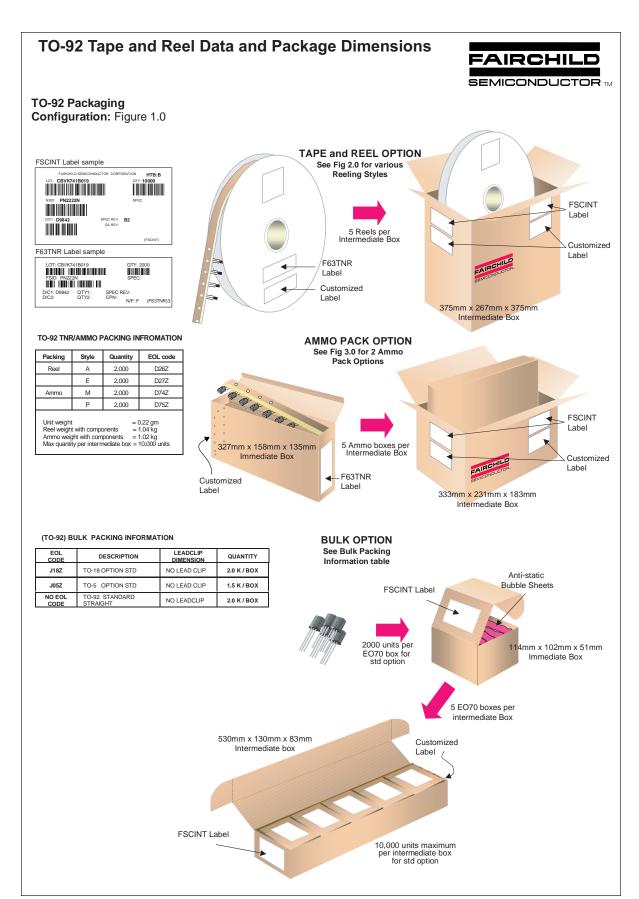


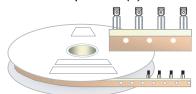
Figure 15. NDS0610 (SOT-23) Transient Thermal Response Curve.



TO-92 Tape and Reel Data and Package Dimensions, continued

TO-92 Reeling Style Configuration: Figure 2.0

Machine Option "A" (H)

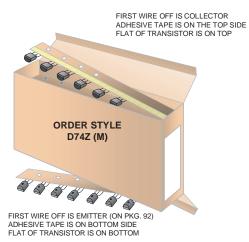


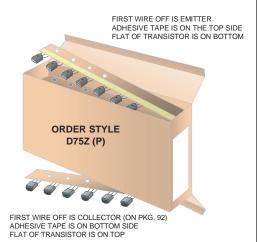
Style "A", D26Z, D70Z (s/h)

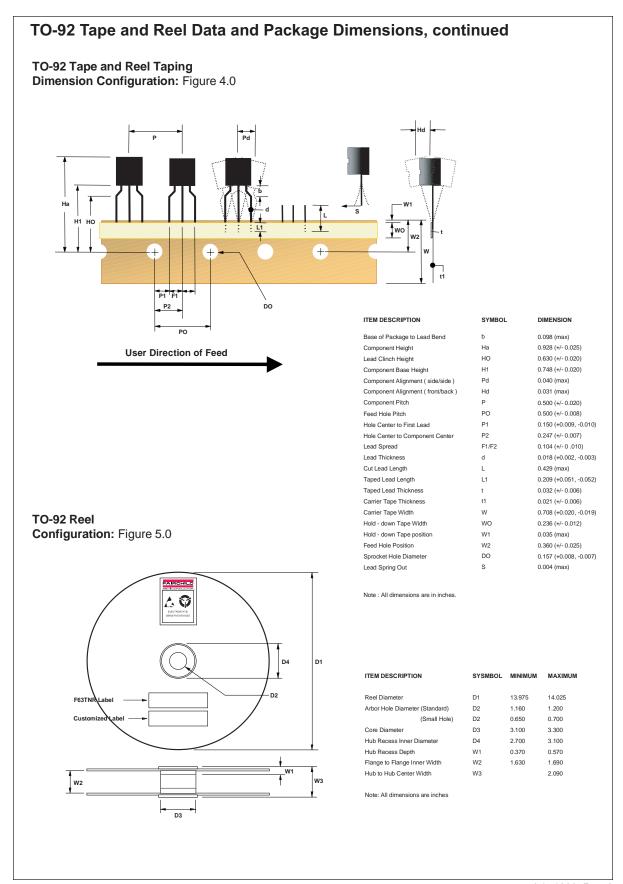
Machine Option "E" (J)

Style "E", D27Z, D71Z (s/h)

TO-92 Radial Ammo Packaging Configuration: Figure 3.0

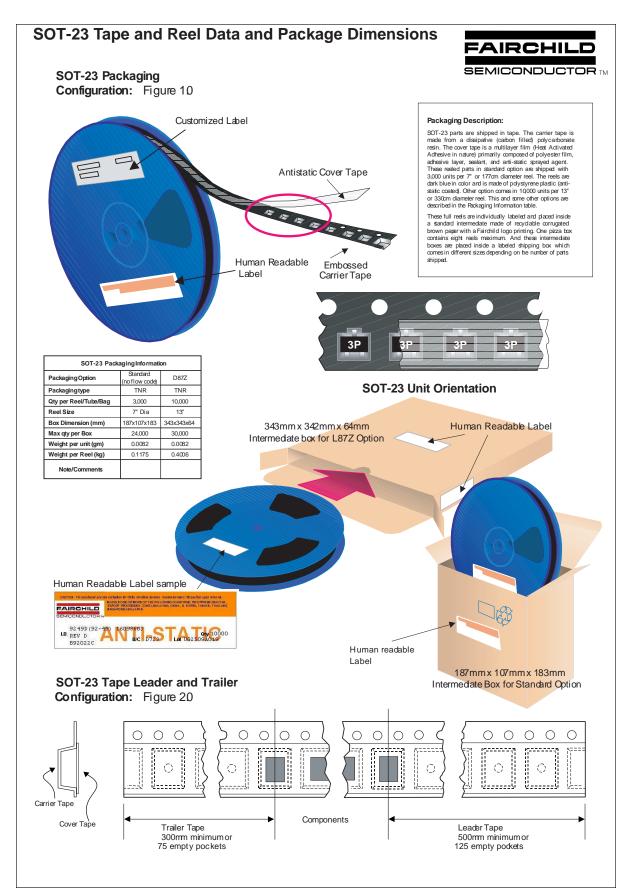






TO-92 Tape and Reel Data and Package Dimensions TO-92 (FS PKG Code 92, 94, 96) Scale 1:1 on letter size paper Dimensions shown below are in: inches [millimeters] Part Weight per unit (gram): 0.1977 0.185 4.70 0.170 4.32 TO-92 (92,94,96) 96 94 В В 0.76 В G Ε Ø0.060 [Ø1.52] 0.010 [0.254] DEEP В S С 0.615 0.570 5.0°TYP.

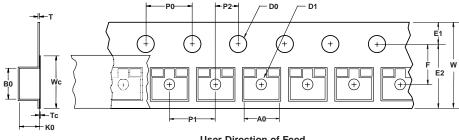
January 2000, Rev. B



SOT-23 Tape and Reel Data and Package Dimensions, continued

SOT-23 Embossed Carrier Tape

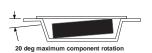
Configuration: Figure 3.0



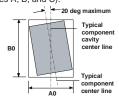
User Direction of Feed	

Dimensions are in millimeter														
Pkg type	Α0	В0	w	D0	D1	E1	E2	F	P1	P0	K0	т	Wc	Тс
SOT-23 (8mm)	3.15 +/-0.10	2.77 +/-0.10	8.0 +/-0.3	1.55 +/-0.05	1.125 +/-0.125	1.75 +/-0.10	6.25 min	3.50 +/-0.05	4.0 +/-0.1	4.0 +/-0.1	1.30 +/-0.10	0.228 +/-0.013	5.2 +/-0.3	0.06 +/-0.02

Notes: A0, B0, and K0 dimensions are determined with respect to the EIA/Jedec RS-481 rotational and lateral movement requirements (see sketches A, B, and C).



Sketch A (Side or Front Sectional View)
Component Rotation



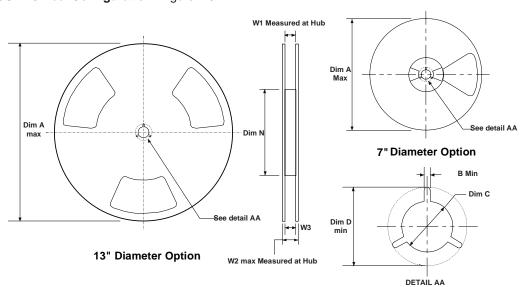
Sketch B (Top View)
Component Rotation



Sketch C (Top View)

Component lateral movement

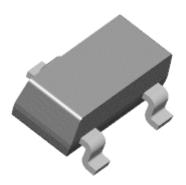
SOT-23 Reel Configuration: Figure 4.0

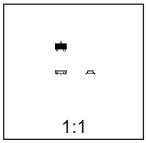


Dimensions are in inches and millimeters									
Tape Size	Reel Option	Dim A	Dim B	Dim C	Dim D	Dim N	Dim W1	Dim W2	Dim W3 (LSL-USL)
8mm	7" Dia	7.00 177.8	0.059 1.5	512 +0.020/-0.008 13 +0.5/-0.2	0.795 20.2	2.165 55	0.331 +0.059/-0.000 8.4 +1.5/0	0.567 14.4	0.311 - 0.429 7.9 - 10.9
8mm	13" Dia	13.00 330	0.059 1.5	512 +0.020/-0.008 13 +0.5/-0.2	0.795 20.2	4.00 100	0.331 +0.059/-0.000 8.4 +1.5/0	0.567 14.4	0.311 - 0.429 7.9 - 10.9

SOT-23 Tape and Reel Data and Package Dimensions, continued

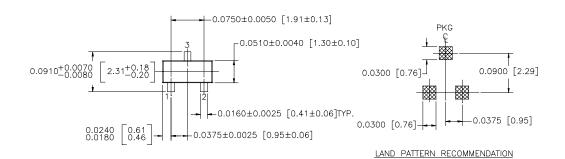
SOT-23 (FS PKG Code 49)

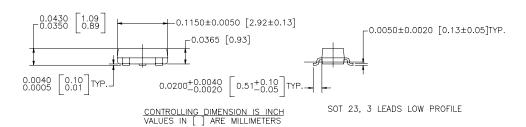




Scale 1:1 on letter size paper Dimensions shown below are in: inches [millimeters]

Part Weight per unit (gram): 0.0082





NOTE: UNLESS OTHERWISE SPECIFIED

- 1. STANDARD LEAD FINISH 150 MICROINCHES / 3.81 MICROMETERS MINIMUM TIN / LEAD (SOLDER) ON ALLOY 42
- 2. REFERENCE JEDEC REGISTRATION TO-236, VARIATION AB, ISSUE G, DATED JUL 1993

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PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition					
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.					
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.					
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