19-1634; Rev 0; 1/00

EVALUATION KIT AVAILABLE

2.125Gbps/1.063Gbps, 3.3V Fibre Channel Repeaters

General Description

The MAX3770 is a 2.125Gbps Fibre Channel repeater IC. The MAX3771 provides a pin-compatible solution for 1.063Gbps Fibre Channel. Both devices are optimized for use in Fibre Channel arbitrated-loop applications and operate from a 3.3V supply.

The MAX3770 is compatible with Fibre Channel jitter tolerance requirements and can recover data signals with up to 0.7 unit interval (UI) jitter. The circuit's fully integrated phase-locked loop (PLL) provides a frequency lock indication and does not need an external reference clock.

The MAX3770 provides low-jitter CML clock and data outputs. To reduce the external parts count, all signal inputs and outputs are internally terminated. The MAX3770/MAX3771 are available in 16-pin QSOP packages.

Applications

2.125Gbps Fibre Channel

1.063Gbps Fibre Channel

Fibre Channel Storage Systems

Storage Area Networks

Fibre Channel Hubs

Ordering Information

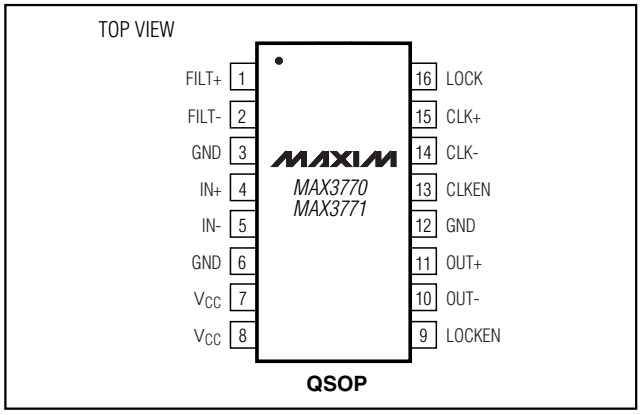
PART	TEMP. RANGE	PIN-PACKAGE
MAX3770CEE	0°C to +70°C	16 QSOP
MAX3771CEE*	0°C to +70°C	16 QSOP

**Future product—contact factory for availability.*

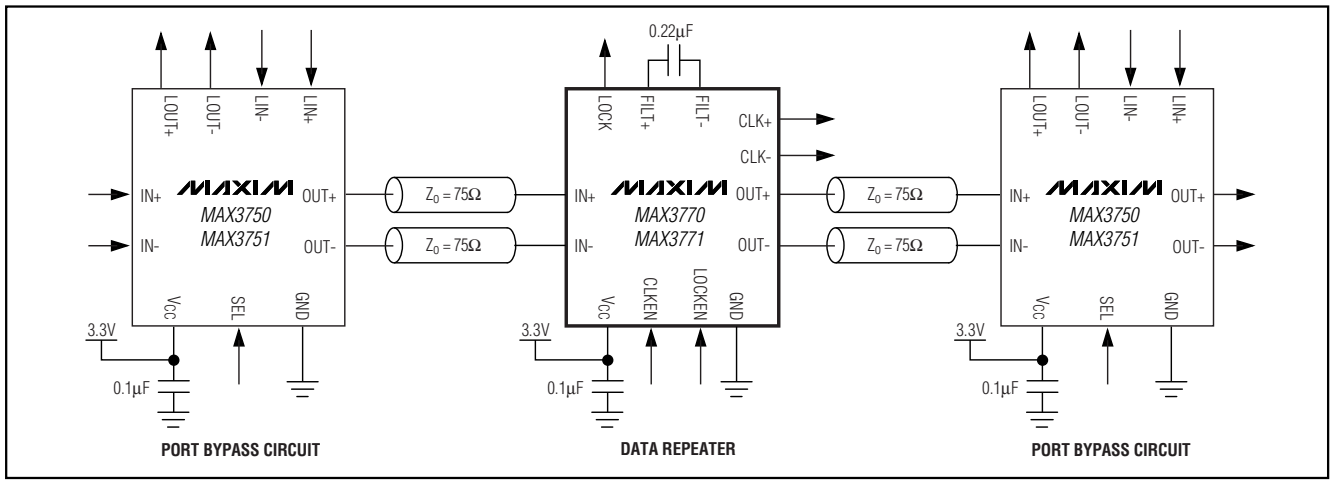
Features

- ♦ **Meet Fibre Channel Jitter Tolerance Requirements**
- ♦ **3.0V to 3.6V Operation**
- ♦ **Internally Terminated Data and Clock I/O**
- ♦ **Reference Clock Not Required**
- ♦ **Frequency Lock Indication**
- ♦ **Low Power Consumption**
  215mW at 3.3V (MAX3770)
  190mW at 3.3V (MAX3771)

Pin Configuration



Typical Application Circuit



2.125Gbps/1.063Gbps, 3.3V Fibre Channel Repeaters

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}.....-0.5V to +5.0V
Pin Voltage Levels (IN+, IN-, FILT+, FILT-, LOCKEN, CLKEN, LOCK).....-0.5V to (V_{CC} + 0.5V)
LOCK Output Current .....-1mA to +10mA
CML Output Currents OUT+, OUT-, CLK+, CLK-.....-22mA to +22mA
Continuous Power Dissipation (T_A = +70°C)
16-Pin TQFP (derate 6.7mW/°C above +70°C).....533mW
Operating Temperature Range.....0°C to +70°C
Storage Temperature Range .....-55°C to +150°C
Processing Temperature (die) .....+400°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +3.6V, T_A = 0°C to +70°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Current (Note 1)	CLKEN = V_{CC}	MAX3771		63		mA
		MAX3770		81	112	
	CLKEN = GND	MAX3771		57		
		MAX3770		67.5	91	
Differential Voltage Signal at OUT or CLOCK	R_{LOAD} = 150Ω, Figure 1		400	780	1000	mVp-p
Output Current at OUT or CLOCK	Sum of I_{OUT+} and I_{OUT-}			10.5		mA
LOCK Output Low	I_{OL} = +1mA				0.7	V
LOCK Output High	I_{OH} = -100µA		2.4			V
Differential Input Voltage Swing			200		2200	mVp-p
Input Common-Mode Voltage				V_{CC} - 0.45		V
Voltage at FILT+, FILT-				V_{CC} - 1.03		V
CLOCKEN and LOCKEN Input Current			-5		+5	µA
Differential Input Resistance			132	150	181	Ω
Differential Output Resistance	OUT+, OUT-, CLK+, CLK-		132	150	181	Ω

Note 1: Supply current includes output currents.

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +3.6V, T_A = 0°C to +70°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
OPERATION AT 2.125Gbps						
Edge Speed	20% to 80%			135	170	ps
Random Jitter Generation at Data Output	T_A = +25°C	Input = K28.7+ (Note 2)		3.4	5.3	ps_{RMS}
		Input = CRPAT (Note 3)		2.3	3.1	
		Input = CRPAT (Notes 3, 5)		3.9	7.3	
Deterministic Jitter Generation	T_A = +25°C	Input = K28.5± (Note 4)		15.6	22	ps_{p-p}
		Input = CRPAT (Notes 3, 5)		27	48	
Jitter Tolerance	T_A = +25°C (Note 5), input = CJTPAT (Note 6)	f = 85kHz (Note 7)	1.5	4.22		UI
		f = 1270kHz (Note 7)	0.1	0.89		
		f = 10MHz		0.36		
CDR Lock Time from Start	Input = CJTPAT (Note 6)			4.4		ms
Propagation Delay				1000	1500	ps
Clock to Q Delay			50	240	300	ps
OPERATION AT 1.063Gbps						
Random Jitter Generation at Data Output	T_A = +25°C	Input = K28.7+ (Note 2)		3.9		ps_{RMS}
		Input = CRPAT (Note 3)		2.3		
		Input = CRPAT (Notes 3, 5)		3.4		
Deterministic Jitter Generation	T_A = +25°C	Input = K28.5± (Note 4)		17		ps_{p-p}
		Input = CRPAT (Notes 3, 5)		36		ps_{p-p}
Jitter Tolerance	T_A = +25°C (Note 5), input = CJTPAT (Note 6), BER = IE-12	f = 42.5kHz		3.1		UI
		f = 635kHz		0.54		
		f = 5MHz		0.3		

Note 2: K28.7+ pattern: 0011111000

Note 3: Compliant random pattern (CRPAT) in hex:

Pattern	No. of Occurrences
3EAA2AAAAA	6
3EAAA6A5A9	1
86BA6C6475 D0E8DCA8B4 7949EAA665	16
72319A95AB	1
C16AAA9AA6	1

Note 4: K28.5± pattern: 0011111010110000010 1

Note 5: Random and deterministic jitter generation at 2.125Gbps is measured with 0.38UI deterministic jitter, and 0.22UI random jitter (BER = 1 x 10^{-12}) applied to the input. Random and deterministic jitter generation at 1.063Gbps is measured with 0.18UI deterministic jitter, and 0.08UI random jitter (BER = 1 x 10^{-12}) applied to the input.

Jitter tolerance at 2.125Gbps is measured with 0.38UI deterministic jitter and 0.22UI random jitter (BER = 1 x 10^{-12}) applied to the input. Jitter tolerance at 1.063Gbps is measured with 0.18UI deterministic jitter, and 0.08UI jitter (BER = 1 x 10^{-12}) applied to the input.

Note 6: Compliant jitter tolerance pattern in hex (CJTPAT):

Pattern	No. of Occurrences
3EAA2AAAAA	6
3EAAA6A5A9	1
871E3871E3	41
871E3870BC78F4AAAAAA	1
AAAAAAAAAA	12
AAA15555E3 871E3871E1	1
AB9C9686E6	1
C16AAA9AA6	1

Note 7: Jitter tolerance measurements at 85kHz and 1270kHz are limited by test equipment. Actual jitter tolerance > indicated.

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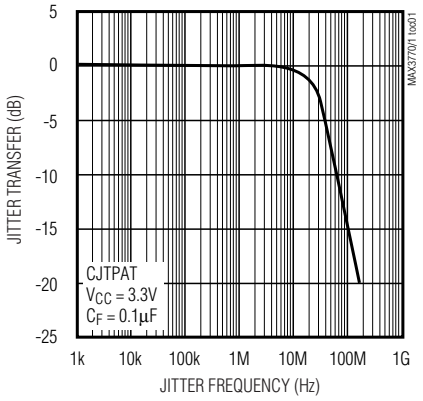
Pin Description

PIN	NAME	FUNCTION
1	FILT+	PLL Loop Filter Connection. Connect a 0.22µF capacitor between FILT+ and FILT-.
2	FILT-	PLL Loop Filter Connection. Connect a 0.22µF capacitor between FILT+ and FILT-.
3, 6, 12	GND	Ground
4	IN+	Positive CML Data Input (Figure 3)
5	IN-	Negative CML Data Input (Figure 3)
7, 8	V_{CC}	Supply Voltage
9	LOCKEN	When this input is forced high, the lock indicator is enabled. Ground for normal operation.
10	OUT-	Negative 75Ω CML Data Output (Figure 4)
11	OUT+	Positive 75Ω CML Data Output (Figure 4)
13	CLKEN	When this input is forced high, the clock output is enabled. Ground for normal operation.
14	CLK-	Negative 75Ω CML Clock Output (Figure 4). Enabled when CLKEN is forced high; disabled when CLKEN is forced low.
15	CLK+	Positive 75Ω CML Clock Output (Figure 4). Enabled when CLKEN is forced high; disabled when CLKEN is forced low.
16	LOCK	Frequency Lock Indicator. High level indicates the PLL is frequency-locked. Disabled when LOCKEN is forced low. The output of the LOCK pin may chatter when large jitter is applied to the input.

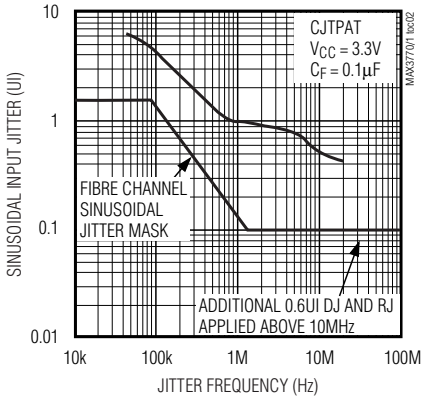
Typical Operating Characteristics

(V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.)

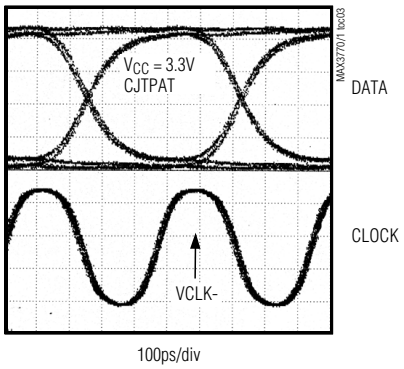
MAX3770
JITTER TRANSFER



MAX3770
JITTER TOLERANCE



MAX3770
RECOVERED DATA AND CLOCK SIGNALS



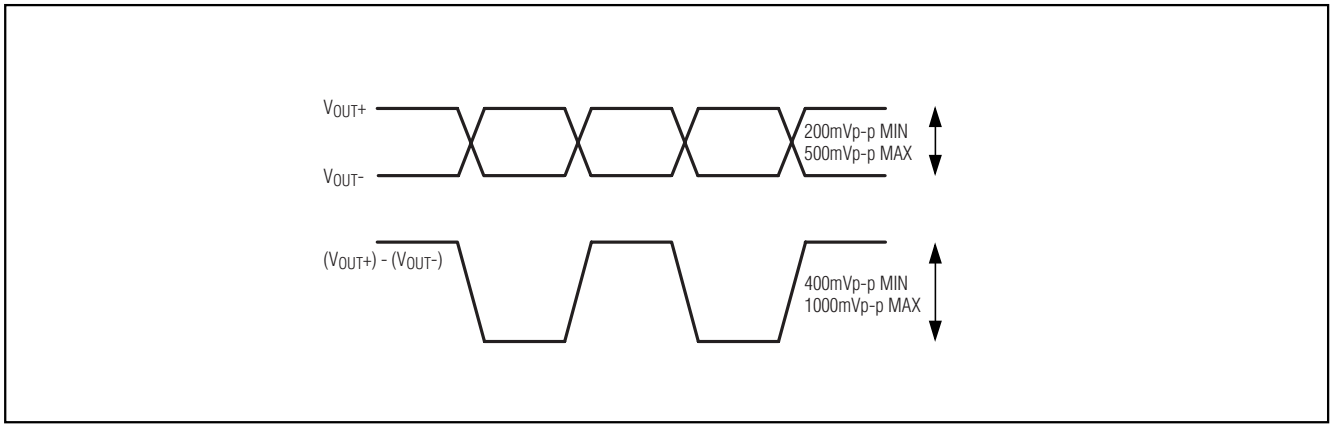


Figure 1. Example of Output Signal with R_{LOAD} = 150Ω

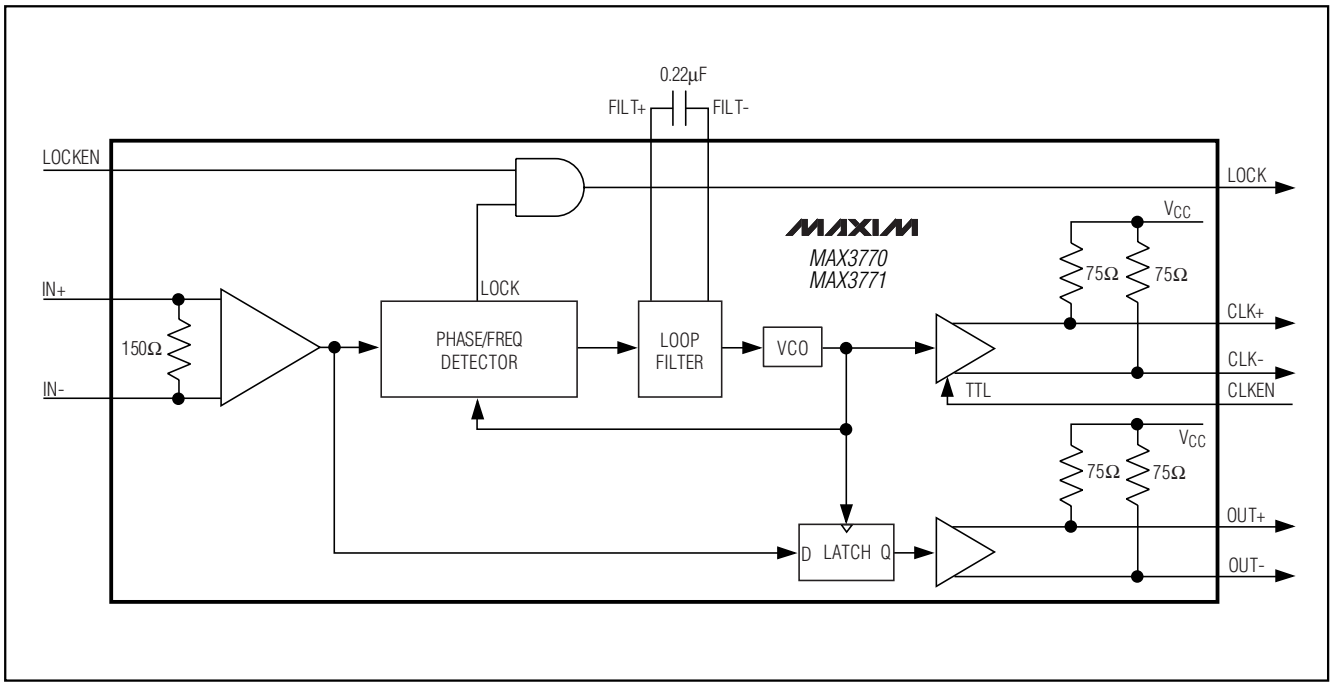


Figure 2. Functional Diagram

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Detailed Description

Figure 2 shows the functional diagram of the MAX3770 Fibre Channel repeater IC. The MAX3770 consists of a fully integrated phased-lock loop (PLL), CML input and output buffers, and a data latch. The PLL consists of a phase/frequency detector (PFD), a loop filter, and a voltage-controlled oscillator (VCO). The input and output signal buffers employ low-noise CML architecture and are terminated on-chip.

Phase and Frequency Detector

The phase/frequency detector generates an output signal that reflects the phase relationship between the incoming data and the internal clock generated by the VCO. Data recovery is accomplished by feedback in the PLL, which drives the error voltage to zero, aligning the falling edge of the recovered clock to the center of the data eye.

The phase frequency detector generates a frequency lock indication that can be monitored at the LOCK pin (Table 1). When the PLL is frequency-locked onto the incoming data, lock transitions high.

VCO and Latch

The fully integrated VCO contains an internal current reference and filter circuitry to minimize the influence of V_{CC} noise. The VCO is trimmed to 2.125GHz (MAX3770) and creates a clock output with frequency proportional to the control voltage applied by the loop filter. Data recovery is accomplished by using the recovered clock signal to latch the incoming data to the CML output buffers, significantly reducing the output jitter.

Applications Information

Figures 3 and 4 show models for the MAX3770/MAX3771 inputs and outputs, including package parasitics. Figure 5 shows typical 50Ω termination applications.

Design Procedure

The MAX3770's performance can be greatly affected by circuit board layout and design. Use good high-frequency design techniques, including minimizing ground inductance and using fixed-impedance transmission lines on the data and clock signals. All IN, OUT, and CLK pins can be connected with 0.1µF or 0.01µF coupling capacitors. If DC coupling is desired, pay particular attention to the DC voltage and current requirements at the pins of interest (see *DC Electrical Characteristics*). The MAX3750/MAX3751 port bypass circuit can be DC-coupled to the MAX3770/MAX3771 repeater. A 0.22µF capacitor should be used for the loop filter.

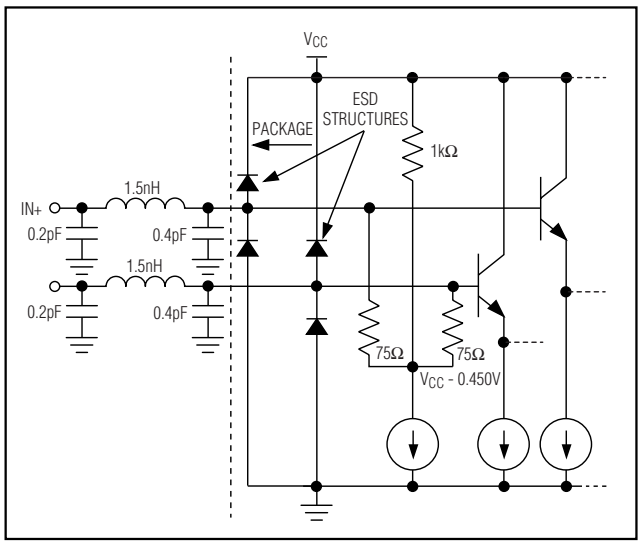


Figure 3. Input Structure

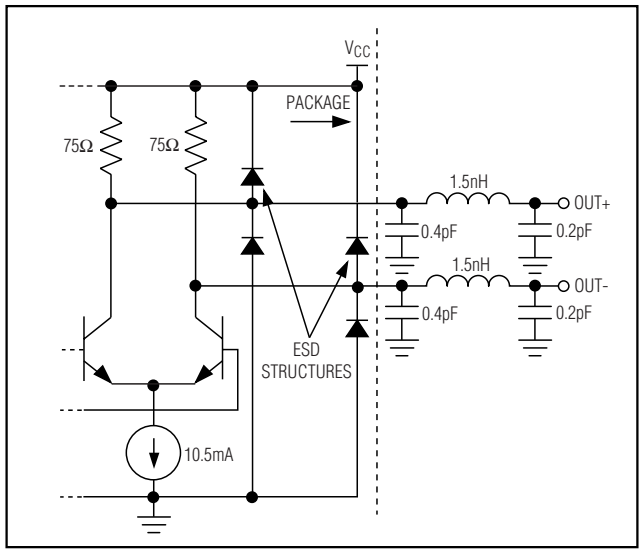


Figure 4. Output Structure

Control Functions

The lock enable (LOCKEN) and clock enable (CLKEN) pins can be configured to control the PLL's clock. Table 1 shows the operational modes available.

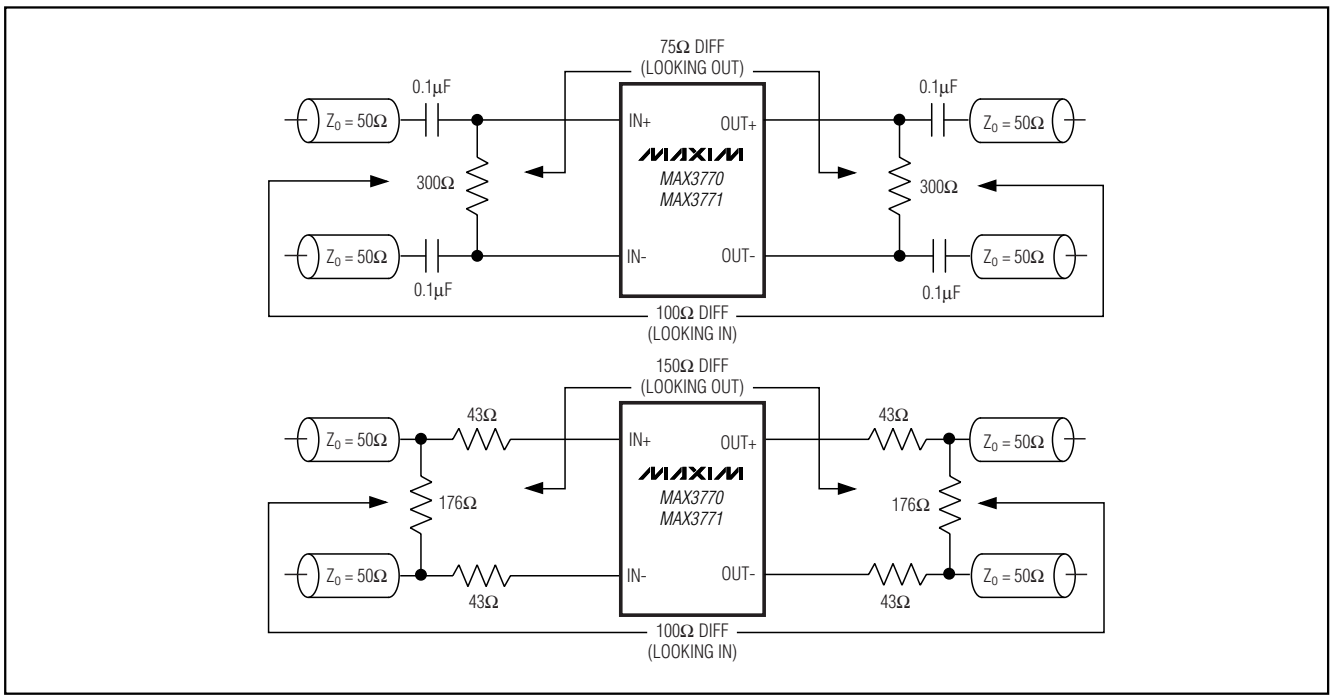
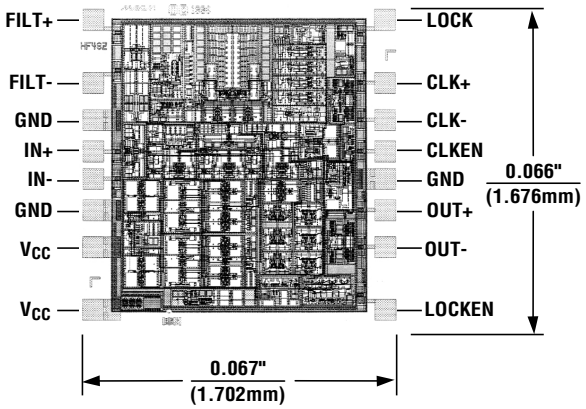


Figure 5. 50Ω Termination Applications

Table 1. Output States When Using Control Functions

INPUT PIN LEVEL		OUTPUT FUNCTION	
LOCKEN	**CLKEN**	**LOCK**	**CLOCK**
GND	GND	Disabled	Disabled
GND	V_{CC}	Disabled	Enabled
V_{CC}	GND	Enabled	Disabled
V_{CC}	V_{CC}	Enabled	Enabled

Chip Topography



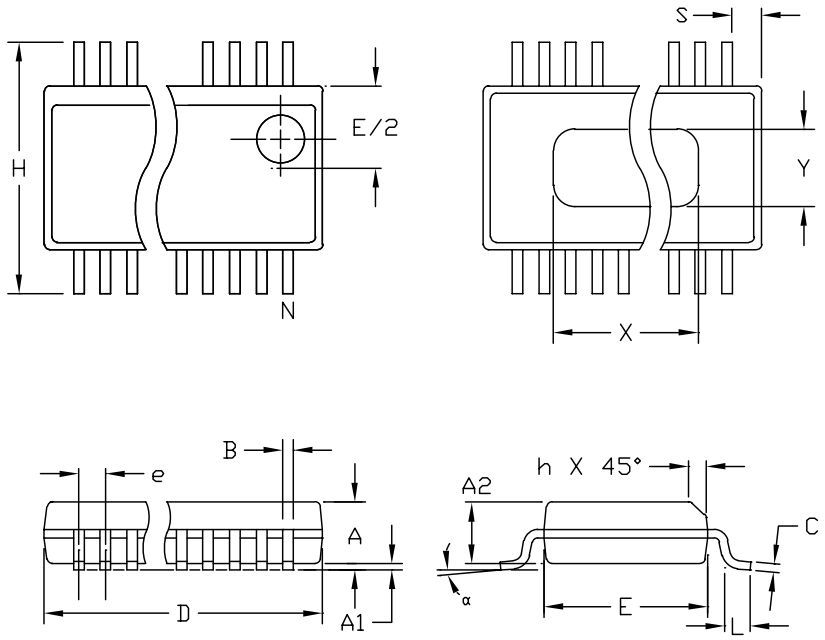
TRANSISTOR COUNT: 1217

SUBSTRATE CONNECTED to GND

2.125Gbps/1.063Gbps, 3.3V Fibre Channel Repeaters

Package Information

QSOP.EPS



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	.061	.068	1.55	1.73
A1	.004	.0098	0.102	0.249
A2	.055	.061	1.40	1.55
B	.008	.012	0.20	0.31
C	.0075	.0098	0.191	0.249
D	SEE VARIATIONS			
E	.150	.157	3.81	3.99
e	.025 BSC		0.635 BSC	
H	.230	.244	5.84	6.20
h	.010	.016	0.25	0.41
L	.016	.035	0.41	0.89
N	SEE VARIATIONS			
X	SEE VARIATIONS			
Y	.071	.087	1.803	2.209
α	0°	8°	0°	8°

VARIATIONS:

	INCHES		MILLIMETERS			
	MIN.	MAX.	MIN.	MAX.	N	
D	.189	.196	4.80	4.98	16	AA
S	.0020	.0070	0.05	0.18		
X	.107	.123	2.72	3.12		
D	.337	.344	8.56	8.74	20	AB
S	.0500	.0550	1.270	1.397		
D	.337	.344	8.56	8.74	24	AC
S	.0250	.0300	0.635	0.762		
D	.386	.393	9.80	9.98	28	AD
S	.0250	.0300	0.635	0.762		
X	.271	.287	6.88	7.29		

NOTES:
1. D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .006" PER SIDE.
3. HEAT SLUG DIMENSIONS X AND Y APPLY ONLY TO 16 AND 28 LEAD POWER-QSOP PACKAGES.
4. CONTROLLING DIMENSIONS: INCHES.

MAXIM
PROPRIETARY INFORMATION

TITLE:
PACKAGE OUTLINE, QSOP, .150", .025" LEAD PITCH

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0055	B	1/1