



LC7215, 7215F, 7215FM

MW/LW PLL Frequency Synthesizers

Overview

The LC7215, LC7215F and LC7215FM are phase-locked-loop frequency synthesizer LSIs that provide accurate reference frequencies over the MW and LW bands, making them ideally suited for AM tuners.

Features

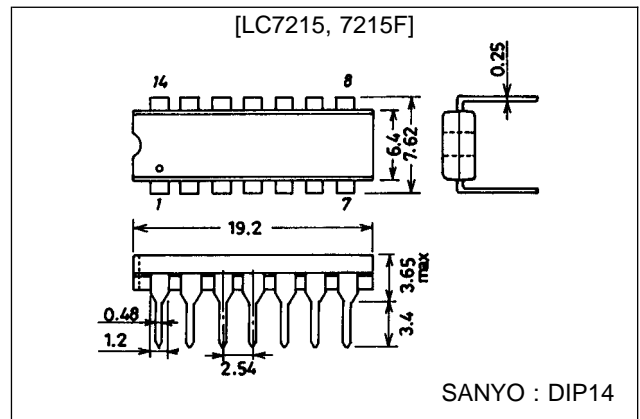
- PLL frequency synthesizer LSIs for MW and LW bands.
- Reference frequencies of 1, 5, 9 and 10 kHz.
- On-chip transistor for the low-pass filter amplifier.
- Single output pin (CMOS output)
- Controller clock output pin.
- Time-base output pin.
- All devices can be used for double conversion demodulation.
- The LC7215F and 7215FM have expanded input frequency ranges.

| | |
|------------|--------------------------------|
| LC7215 | 0.5 to 13 MHz : (DIP14) |
| LC7215F/FM | 0.5 to 20 MHz : (DIP14/MFP14S) |

Package Dimensions

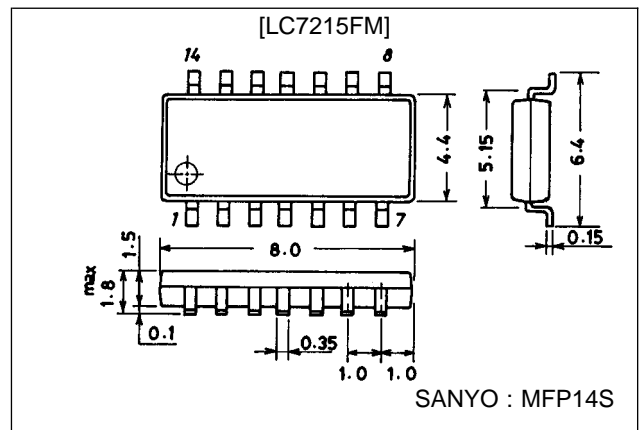
unit : mm

3003A-DIP14



unit : mm

3111-MFP14S



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Specifications

Absolute Maximum Ratings at $T_a = 25^\circ\text{C}$, $V_{SS} = 0\text{ V}$

Values in parentheses are for the LC7215F and LC7215FM.

| Parameter | Symbol | Conditions | Ratings | Unit |
|-----------------------------|---------------------|--|------------------------|------------------|
| Maximum supply voltage | $V_{DD\text{ max}}$ | V_{DD} | -0.3 to +6.5 | V |
| Input voltage | V_{IN1} | All input pins | -0.3 to $V_{DD} + 0.3$ | V |
| | V_{IN2} | CE, CL, DATA | (Note) -0.3 to +6.5 | V |
| Output current | I_{OUT} | AOUT | 0 to 5 | mA |
| Output voltage | V_{OUT1} | AOUT | -0.3 to +15 | V |
| | V_{OUT2} | \overline{SYC} , \overline{TB} | -0.3 to +6.5 | V |
| | V_{OUT3} | All output pins except V_{OUT1} and V_{OUT2} | -0.3 to $V_{DD} + 0.3$ | V |
| Allowable power dissipation | $P_d\text{ max}$ | $T_a \leq 85^\circ\text{C}$ | 150 | mW |
| Operating temperature | T_{opr} | | -40 to +85 | $^\circ\text{C}$ |
| Storage temperature | T_{stg} | | -55 to +125 | $^\circ\text{C}$ |

Note: Voltage that is applied to the resistors when resistors totaling at least 10 k Ω are connected to a pin in series.

Allowable Operating Conditions at $V_{SS} = 0\text{ V}$

Values in parentheses are for the LC7215F and LC7215FM.

| Parameter | Symbol | Conditions | min | typ | max | Unit |
|---|------------|---|----------|-------|-----------|-------|
| Supply voltage | V_{DD1} | V_{DD} | (4.5)3.0 | | (5.5)5.5 | V |
| | V_{DD2} | V_{DD} (Crystal OSC oscillation guaranteed) | 3.0 | | 5.5 | V |
| High-level input voltage | V_{IH} | CE, CL, DATA | 2.0 | | V_{DD1} | V |
| Low-level input voltage | V_{IL} | CE, CL, DATA | 0 | | 0.5 | V |
| Output voltage | V_{OUT1} | AOUT | | | 13 | V |
| | V_{OUT2} | \overline{SYC} , \overline{TB} | | | 5.5 | V |
| Input frequency | f_{IN1} | PIN: Sine wave, capacitive coupling V_{DD1} , *S = 1 | (2.3)2.3 | | (20)13 | MHz |
| | f_{IN2} | PIN: Sine wave, capacitive coupling V_{DD1} , *S = 0 | 0.5 | | 2.5 | MHz |
| Oscillation guaranteed crystal oscillator | X'tal | XIN, XOUT: $C_I \leq 30\ \Omega$ | 8.00 | 11.16 | 12.00 | MHz |
| Input amplitude | V_{IN1} | PIN: Square wave, capacity connection V_{DD1} , *S = 1 | 100 | | 1000 | mVrms |
| | V_{IN2} | PIN: Square wave, capacity connection V_{DD1} , *S = 0 | 100 | | 1000 | mVrms |
| Power supply | — | V_{DD} , V_{SS} : A capacitor of at least 1000 pF must be inserted. | 1000 | | | pF |

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Electrical Characteristics within the allowable operating ranges

Values in parentheses are for LC7215F and LC7215FM.

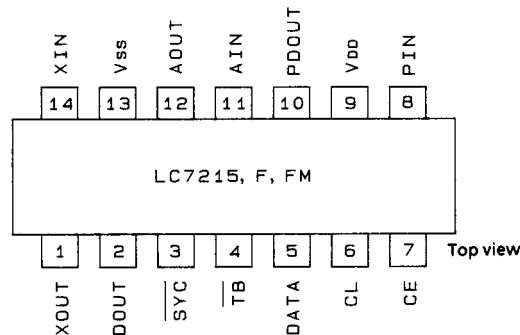
| Parameter | Symbol | Conditions | min | typ | max | Unit |
|---|-------------------|--|-------------------------|------|------|------|
| High-level input currents | I _{IH1} | XIN: V _I = V _{DD} | | | 20 | μA |
| | I _{IH2} | PIN: V _I = V _{DD} | | | 40 | μA |
| | I _{IH3} | CE, CL, DATA: V _I = V _{DD} | | | 3.0 | μA |
| | I _{IH4} | AIN: V _I = V _{DD} | | 0.01 | 1.0 | μA |
| Low-level input currents | I _{IL1} | XIN: V _I = V _{SS} | | | 20 | μA |
| | I _{IL2} | PIN: V _I = V _{SS} | | | 40 | μA |
| | I _{IL3} | CE, CL, DATA: V _I = V _{SS} | | | 3.0 | μA |
| | I _{IL4} | AIN: V _I = V _{SS} | | 0.01 | 1.0 | μA |
| High-level output voltages | V _{OH1} | DOUT: I _O = 1 mA | V _{DD} -1.0 | | | V |
| | V _{OH2} | PDOUT: I _O = 0.5 mA | V _{DD} -1.0 | | | V |
| Low-level output voltages | V _{OL1} | DOUT: I _O = -1 mA | | | 1.0 | V |
| | V _{OL2} | PDOUT: I _O = -0.5 mA | | | 1.0 | V |
| | V _{OL4} | SYC, TB: I _O = 0.5 mA | | | 1.0 | V |
| | V _{OL5} | AOUT: I _O = 1 mA | | | 1.0 | V |
| Output off-state leakage currents | I _{OFF1} | SYC, TB: V _O = V _{DD} | | | 3.0 | μA |
| | I _{OFF2} | AOUT: V _O = 13 V | | | 5.0 | μA |
| Tristate output High-level off-state leakage current | I _{OFFH} | PDOUT: V _O = V _{DD} | | 0.01 | 1.0 | nA |
| Tristate output Low-level off-state leakage current | I _{OFFL} | PDOUT: V _O = V _{SS} | | 0.01 | 1.0 | nA |
| High-level output voltage | V _{OH3} | XOUT: I _O = -0.1 mA | V _{DD} -1.0 | | | V |
| Low-level output voltage | V _{OL3} | XOUT: I _O = 0.1 mA | | | 1.0 | V |
| Supply current | I _{DD1} | V _{DD} : f _{IN1} = 13 MHz, *S = 1 (High speed) (Note 1) | | | 10 | mA |
| | | f _{IN1} = 20 MHz, *S = 1 (High speed) (Note 1) | | | (12) | mA |
| | I _{DD2} | V _{DD} : f _{IN1} = 2.5 MHz, *S = 0 (Low speed) (Note 1) | | | 5 | mA |
| | I _{DD3} | V _{DD} : V _{DD} = 5.5 V, *O = 0, P = 1 (Note 2) | | 1.2 | 2.0 | mA |
| | | V _{DD} : V _{DD} = 4.5 V, *O = 0, P = 1 (Note 2) | | 0.7 | 1.5 | mA |
| V _{DD} : V _{DD} = 3.0 V, *O = 0, P = 1 (Note 2) | | | 0.4 | 1.0 | mA | |

* S, O and P are serial control bits.

Note 1. V_{IN1} = V_{IN2} = 100 mVms. The 11.16 MHz crystal is connected to XIN and XOUT. All other inputs are connected to V_{SS} and all other outputs are open.

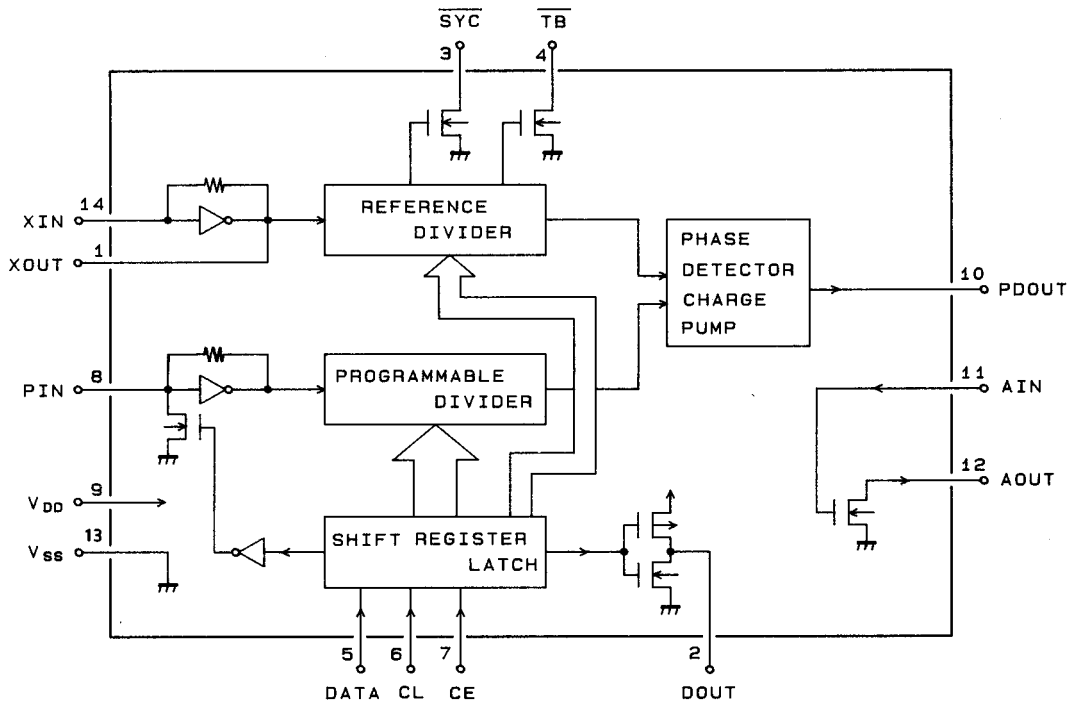
2. The 11.16 MHz crystal is connected to XIN and XOUT. All other inputs are connected to V_{DD} and all other outputs are open. (Backup mode when PLL is halted.)

Pin Assignment



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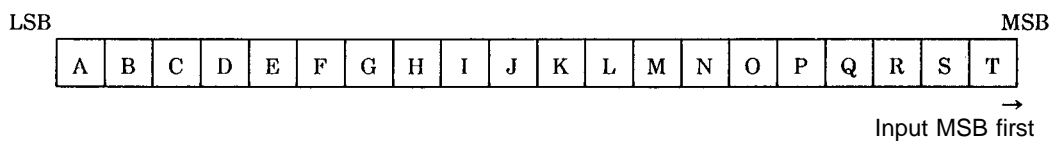
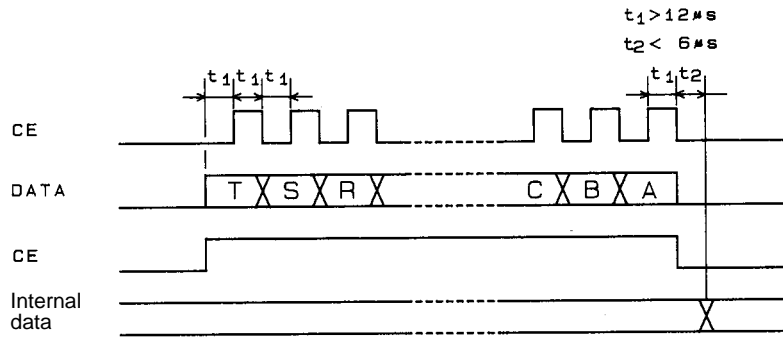
Block Diagram



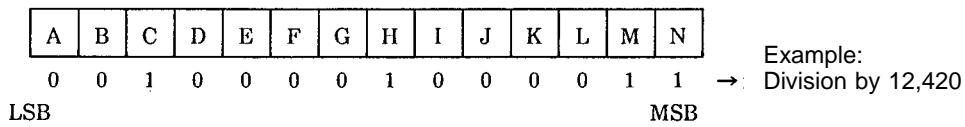
Pin Description

| Name | Description |
|-----------------------------------|---|
| XIN, XOUT | 11.16 MHz crystal oscillator connection, feedback resistance built-in |
| PIN | Local oscillator signal input |
| V _{DD} , V _{SS} | Power supply |
| DATA, CL, CE | Data input |
| DOUT | Single bit data output |
| AIN, AOUT | Low-pass filter amplifier |
| PDOUT | Charge pump output |
| TB | 8 Hz time-base output |
| SYC | 60 kHz controller clock output |

Data Input



(1) A to N: Divider data



(2) O, P: Mode selection

| Mode | O | P | DOUT | TB | Operation |
|-------|---|---|------|------|--|
| NOR1 | 0 | 0 | T | 8 Hz | Normal operation (with PLL operating) |
| NOR2 | 0 | 1 | T | 8 Hz | Normal operation (backup when PLL is halted) |
| TEST1 | 1 | 0 | | | (Device test mode) |
| TEST2 | 1 | 1 | | | (Device test mode) |

(3) Q, R: Reference frequency selection

| Q | R | Reference frequency |
|---|---|---------------------|
| 0 | 0 | 9 kHz |
| 0 | 1 | 10 kHz |
| 1 | 0 | 1 kHz |
| 1 | 1 | 5 kHz |

(4) S: Programmable divider input sensitivity switch

S = 1: for High speed
S = 0: for Low speed

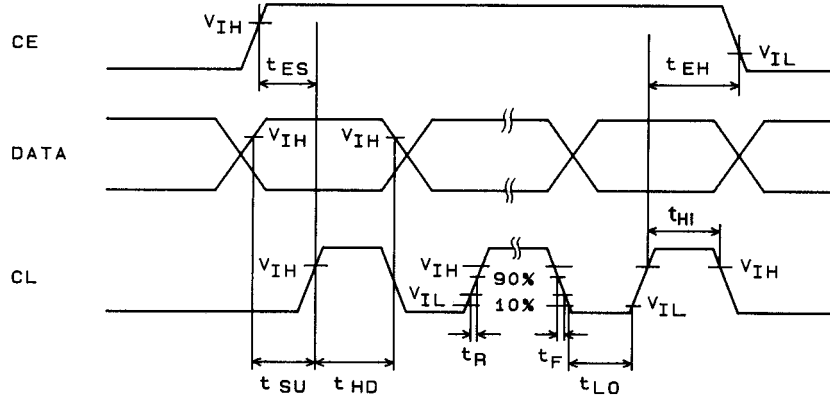
(5) T: Output to DOUT

T = 1: DOUT = 1
T = 0: DOUT = 0

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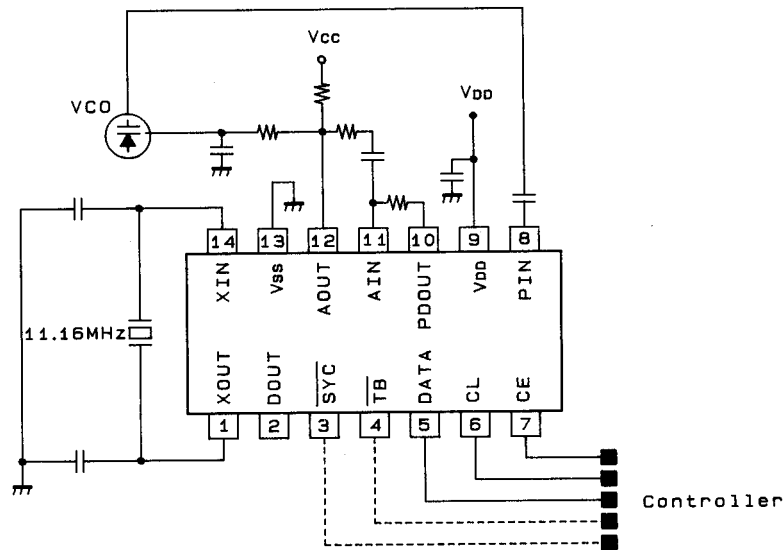
Data Input Timing

$V_{IH} = 2.0$ to V_{DD} , $V_{IL} = 0$ to 0.5 V
 $X'tal = 8.00$ to 11.16 (typ) to 12.00 MHz
 Data latch: Rising edge of CL

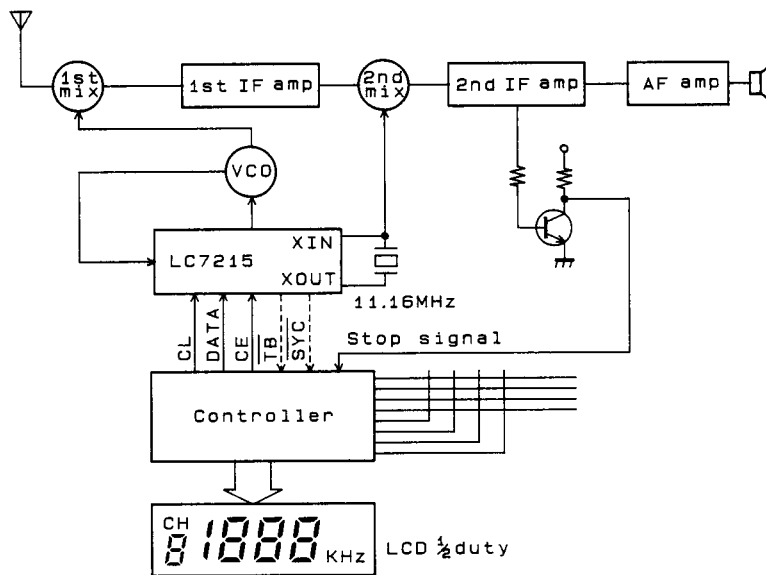


| Item | Symbol | 11.16 MHz crystal | Other crystal frequencies | Effective value |
|-----------------------|----------|---------------------|--|--------------------------------|
| Enable setup time | t_{ES} | At least 12 μ s | At least $2 \times (1/f_{Xtal} \times 62)$ | 1/2 of the value shown at left |
| Enable hold time | t_{EH} | ↑ | ↑ | |
| Data setup time | t_{SU} | ↑ | ↑ | |
| Data hold time | t_{HD} | ↑ | ↑ | |
| Clock Low-level time | t_{LO} | ↑ | ↑ | |
| Clock High-level time | t_{HI} | ↑ | ↑ | |
| Rise time | t_R | 1 μ s or less | 1 μ s or less | |
| Fall time | t_F | ↑ | ↑ | |

(1) Sample Application Circuit



(2) Double-conversion Receiver



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