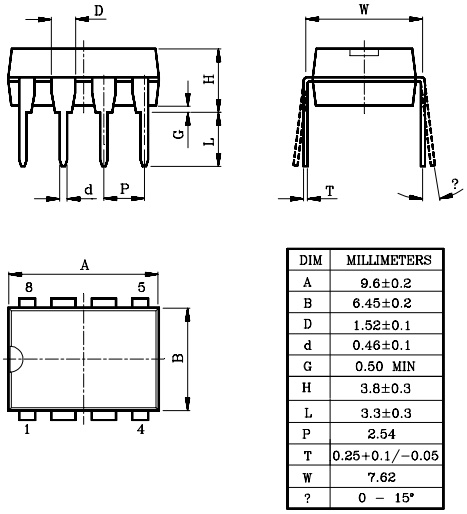
LOW POWER AUDIO AMPLIFIER

The KIA6419P/F is a low power audio amplifier integrated circuit intended (primarily) for telephone applications, such as in speakerphones. It provides differential speaker outputs to maximize output swing at low supply voltages (2.0 volts minimum). Coupling capacitors to the speaker are not required. Open loop gain is 80dB, and the closed loop gain is set with two external resistors. A chip disable pin permits powering down and/ or muting the input signal. The KIA6419 is available in a standard 8-pin DIP or a surface mount package.



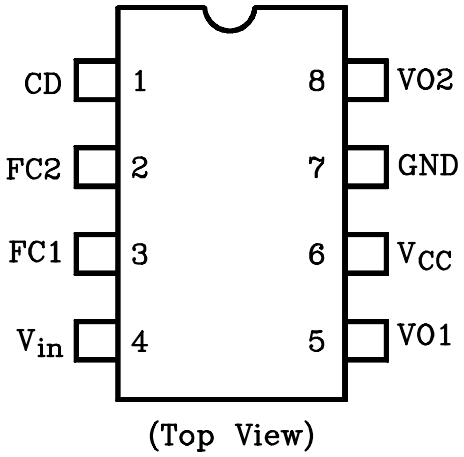
DIM	MILLIMETERS
A	9.6±0.2
B	6.45±0.2
D	1.52±0.1
d	0.46±0.1
G	0.50 MIN
H	3.8±0.3
L	3.3±0.3
P	2.54
T	0.25+0.1/−0.05
W	7.62
?	0 ~ 15°

DIP-8

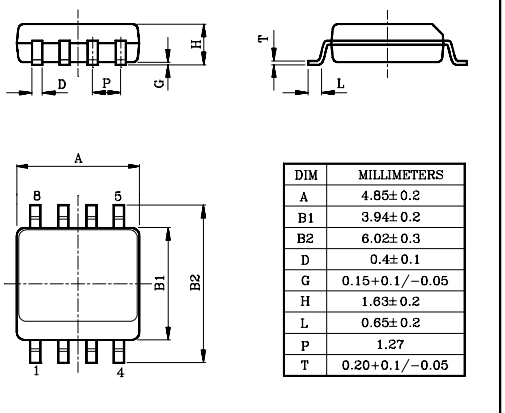
FEATURES

- Wide Operating Supply Voltage Range (2-16 volts)-Allows Telephone Line Powered Applications.
- Low Quiescent Supply Current 2.0mA Typical) for Battery Powered Applications.
- Chip Disable Input to Power Down the IC.
- Low Power-Down Quiescent Current (65μA Typical)
- Drives a Wide Range of Speaker Loads (8 Ohms and Up)
- Output Power Exceeds 250mW with 32 Ohm Speaker
- Low Total Harmonic Distortion (0.5% Typical)
- Gain Adjustable from <0 dB to> 46dB for Voice Band
- Requires Few External Components

PIN CONNECTION



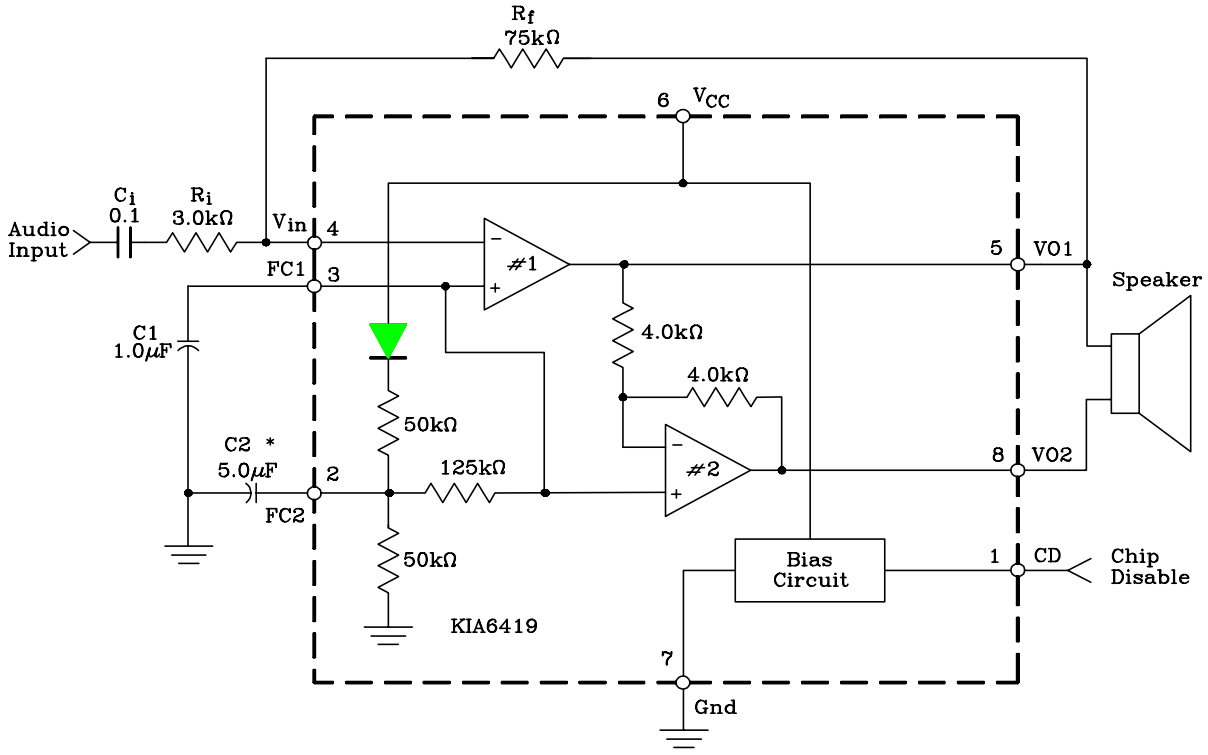
(Top View)



DIM	MILLIMETERS
A	4.85±0.2
B1	3.94±0.2
B2	6.02±0.3
D	0.4±0.1
G	0.15+0.1/−0.05
H	1.63±0.2
L	0.65±0.2
P	1.27
T	0.20+0.1/−0.05

FLP-8

BLOCK DIAGRAM AND TYPICAL APPLICATION CIRCUIT



* =Optional
Differential Gain = $2\times\frac{R_f}{R_i}$

MAXIMUM RATINGS (Ta=25℃)

PARAMETER	VALUE	UNITS
Supply Voltage	-1.0 to 18	Vdc
Maximum Output Current at VO1, VO2	±250	mA
Maximum Voltage @Vin, FC1, FC2, CD	-1.0 V_{CC}+1.0	Vdc
Applied Output Voltage to VO1, VO2 when disabled	-1.0 V_{CC}+1.0	Vdc
Operating Temperature	-20~70	℃
Junction Temperature	-55~140	℃

Devices should not be operated at these values. The "Recommended Operating Limits" provide for actual device operation.

RECOMMENDED OPERATING LIMITS

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS
Supply Voltage	V_{CC}	+2.0	-	+16	Vdc
Load Impedance	R_L	8.0	-	100	Ω
Peak Load Current	I_L	-	-	±200	mA
Differential Gain (5.0kHz bandwidth)	AVD	0	-	46	dB
Voltage @ CD (Pin 1)	VCD	0	-	V_{CC}	Vdc
Ambient Temperature	T_A	-20	-	+70	℃

ELECTRICAL CHARACTERISTICS (Ta=25℃)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
AMPLIFIERS (AC CHARACTERISTCIS)					
AC Input Resistance (@V_{IN})	r_i	-	>30	-	MΩ
Open Loop Gain (Amplifier #1, f<100Hz)	A_{VOL1}	80	-	-	dB
Closed Loop Gain (Amplifier #2) (V_{CC}=6.0V, f=1.0kHz, R_L=32Ω)	A_{V2}	-0.35	0	+0.35	dB
Gain Bandwidth Product	GBW	-	1.5	-	MHz
Output Power, V_{CC}=3.0V, R_L=16Ω, THD≤10% V_{CC}=6.0V, R_L=32Ω, THD≤10% V_{CC}=12V, R_L=100Ω, THD≤10%	Pout3 Pout6 Pout12	55 250 400	- - -	- - -	mW
Total Harmonic Distortion (f=1.0kHz) (V_{CC}=6.0V, R_L=32Ω, Pout=125mW) (V_{CC}≥3.0V, R_L=8.0Ω, Pout=20mW) (V_{CC}≥12V, R_L=32Ω, Pout=200mW)	THD	- - -	0.5 0.5 0.6	1.0 - -	%
Power Supply Rejection (V_{CC}=6.0V, ΔV_{CC}=3.0V) (C1=∞, C2=0.01μF) (C1=0.1μF, C2=0, f=1.0kHz) (C1=1.0μF, C2=5.0μF, f=1.0kHz)	PSRR	50 - -	- 12 52	- - -	dB
Muting (V_{CC}=6.0V, 1.0kHz≤f≤20kHz, CD=2.0V)	GMT	-	>70	-	dB
AMPLIFIERS (DC CHARACTERISTCIS)					
Output DC Level @VO1, VO2, V_{CC}=3.0V, R_L=16Ω (Rf=75k) V_{CC}=6.0V V_{CC}=12V	VO(3) VO(6) VO(12)	1.0 - -	1.15 2.65 5.65	1.25 - -	Vdc
Output High Level (I_{OUT}=-75mA, 2.0V≤V_{CC}≤16V)	V_{OH}	-	V_{CC}-1.0	-	Vdc
Output Low Level (I_{OUT}=75mA, 2.0V≤V_{CC}≤16V)	V_{OL}	-	0.16	-	Vdc
Output DC Offset Voltage (VO1-VO2) (V_{CC}=6.0V, Rf=75kΩ, R_L=32Ω)	ΔV_O	-30	0	+30	mV
Input Bias Current @V_{IN} (V_{CC}=6.0V)	I_{IB}	-	-100	-200	nA
Equivalent Resistance @FC1 (V_{CC}=6.0V)	R_{FC1}	100	150	220	kΩ
Equivalent Resistance @FC2 (V_{CC}=6.0V)	R_{FC2}	18	25	40	kΩ
CHIP DISABEL (Pin 1)					
Input Voltage-Low	V_{IL}	-	-	0.8	Vdc
Input Voltage-High	V_{IH}	2.0	-	-	Vdc
Input Resistance (V_{CC}=V_{CD}=16V)	R_{CD}	50	90	175	kΩ
Power Supply					
Power Supply Current (V_{CC}=3.0V, R_L=∞, CD=0.8V) (V_{CC}=16V, R_L=∞, CD=0.8V) (V_{CC}=3.0V, R_L=∞, CD=2.0V)	I_{CC3} I_{CC16} I_{CCD}	- - -	2.0 3.0 65	3.0 4.0 100	mA μA

Note : Currents into a pin are positive, currents out of a pin are negative.

PIN DESCRIPTION

SYMBOL	PIN.	DESCRIPTION
CD	1	Chip Disable-Digital Input. A logic "0"(<0.8V) sets normal operation. A Logic "1" (≥2.0V) sets the power down mode. Input impedance is nominally 90kΩ.
FC2	2	A capacitor at this pin increases power supply rejection, and affects turn-on time. This pin can be left open if the capacitor at FC1 is sufficient.
FC1	3	Analog Ground for the amplifiers. A 1.0μF capacitor at this pin (with a 5.0μF capacitor at Pin 2) provides (typically) 52dB of power supply rejection. Turn-on time of the circuit is affected by the capacitor on this pin. This pin can be used as an alternate input.
V_{IN}	4	Amplifier Input. The input capacitor and resistor set low frequency rolloff and input impedance. The feedback resistor is connected to this pin and VO1.
VO1	5	Amplifier Output #1. The dc level is ≈ (V_{CC}-0.7V)/2.
V_{CC}	6	DC supply voltage (+2.0 to +16volts) is applied to this pin.
GND	7	Ground pin for the entire circuit.
VO2	8	Amplifier Output #2. This signal is equal in amplitude, but 180° out of phase with that at VO1. The dc level is ≈ (V_{CC}-0.7V)/2.

TYPICAL TEMPERATURE PERFORMANCE (-20° <T_A<+70℃)

SYMBOL	Typical Change	Units
Input Bias Current (@V_{IN})	±40	pA/℃
Total Harmonic Distortion (V_{CC}=6.0V, R_L=32Ω, Pout=125mW, f=1.0kHz)	+0.003	%/℃
Power Supply Current (V_{CC}=3.0V, R_L=∞, CD=0V) (V_{CC}=3.0V, R_L=∞, CD=2.0V)	-2.5 -0.03	μA/℃

DESIGN GUIDELINES

GENERAL

The KIA6451P is a low power audio amplifier capable of low voltage operation (V_{CC}=2.0V minimum) such as that encountered in line-powered speakerphones. The circuit provides a differential output (VO1=VO2) to the speaker to maximize the available voltage swing at low voltages. The differential gain is set by two external resistors. Pins FC1 and FC2 allow controlling the amount of power supply and noise rejection, as well as providing alternate inputs tothe amplifiers. The CD pin permits powering down the IC for muting purposes and to conserve power.

AMPLIFIERS

Referring to the block diagram. The internal configuration consists of two identical operational amplifiers. Amplifier #1 has an open loop gain of ≥ 80 dB (at f≤100Hz), and the closed loop gain is set by external resistors Rf and Ri. The amplifier is unity gain stable, and has a unity gain frequency of approximately 1.5MHz. In order to adequately cover the telephone voice band (300-3400Hz). a maximum closed leep gain of 46dB is recommended. Amplifier #2 is internally set to a gain of -1.0 (0dB). The outputs of both amplifiers are capable of sourcing and sinking a peak current of 200mA. The outputs can typically swing to within≈0.4 volts above ground and to within ≈1.3 volts below V_{CC}. at the maximum current. See Figures 18 and 19 for V_{OH} and V_{OL} curves. The output dc offset voltage (VO1-VO2) is primarily a function of the feedback resistor(Rf), and secondarily due to the amplifiers' input offset voltages. The input offset voltage of the two amplifiers will generally be similar for a particular Ic, and therefore nearly cancel each other at the outputs.

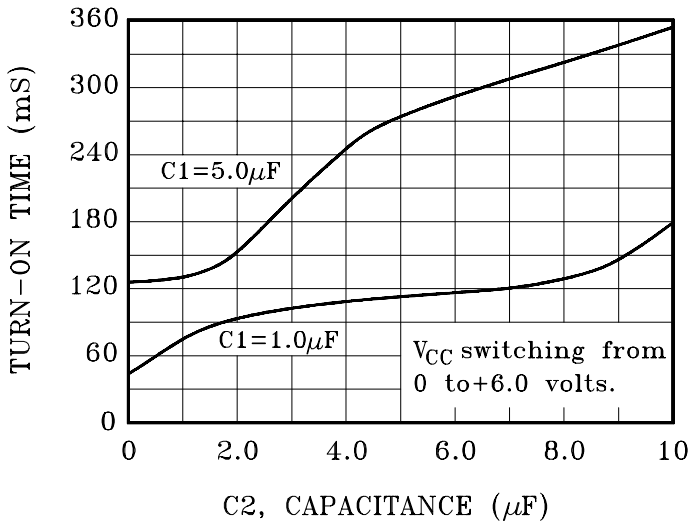
Amplifier #1's bias current, however, flows out of V_{IN} (Pin4) and through Rf, forcing VO1 to shift negative by an amount equal to ($R_f \times 1_{IB}$). VO2 is shifted positive an equal amount. The output offset voltage specified in the Electrical characteristics is measured with the feedback resistor shown in the typical application circuit, and therefore takes into account the bias current as well as internal offset voltages of the amplifiers. The bias current is constant with respect to V_{CC}.

FC1 and FC2

Power supply rejection is provided by the capacitors (C1 and C2 in the Typical Application Circuit) at FC1 and FC2, C2 is somewhat dominant at low frequencies, while C1 is dominant at high frequencies, as shown in the graphs of Figures 4-7. The required values of C1 and C2 depend on the conditions of each application. A line powered speakerphone, for example, will require more filtering than a circuit powered by a well regulated power supply. The amount of rejection is a function of the capacitors, and the equivalent impedance looking into FC1 and FC2 (listed in the Electrical Characteristics as R_{FC1} and R_{FC2}).

In addition to providing filtering, C1 and C2 also affect the turn-on time of the circuit at power-up, since the two capacitors must charge up through the internal 50k and 125kΩ resistors. The graph of Figure 1 indicates the turn-on time upon application of V_{CC} of +6.0 volts. The turn-on time is ≈60% longer for V_{CC}=3.0 volts, and ≈20% less for V_{CC}=9.0 volts. Turn-off time is <10μS upon removal of V_{CC}.

FIGURE 1-TURN-ON TIME versus C1,C2 AT POWER-ON



CHIP DISABLE

The chip disable (pin 1) can be used to power down the IC to conserve power, or for muting or both when at a logic "0" (0 to 0.8 volts), the KIA6419 is enabled for normal operation. When Pin 1 is at a logic "1" (2.0 to V_{CC} volts), the IC is disabled. If pin 1 is open, that is equivalent to a logic "0", although good design practice dictates that an input should never be left open. Input impedance at pin 1 is a nominal 90kΩ. The power supply current (when disabled) is shown in Figure 15.

Muting, defined as the change in differential gain from normal operation to muted operation, is in excess of 70dB. The turn-off time of the audio output, from the application of the CD signal, is <2.0μS, and turn on-time is 12-15 ms. Both times are independent of C1, C2 and V_{CC}.

When the KIA6419 is disabled, the voltages at FC1 and FC2 do not changes as they are powered from V_{CC} The outputs, VO1, and VO2 change to a high impedance condition, removing the signal from the speaker. If signals from other sources are to be applied to the outputs (while disabled), they must be within the range of V_{CC} and ground.

POWER DISSIPATION

Figures 8-10 indicate the device dissipation (within the IC) for various combinations of V_{CC}, R_L and load power. The maximum power which can safely be dissipated within the KIA6419 is found from the following equation : $P_D=(140℃-T_A)/\theta JA$

where T_A is the ambient temperature ; and θJA is the package thermal resistance (100℃/W for the standard DIP package, and 180℃/W for the surface mount package.)

The power dissipated within the KIA6419 in a given application, is found from the following equation : $P_D=(V_{CC}\times I_{CC})+(I_{RMS}\times V_{CC})-(R_L\times I_{RMS}^2)$ where I_{CC} is obtained from Figrue 15 ; and I_{RMS} is the RMS current at the load ; and R_L is the load resistance.

Figures 8-10, along with Figures 11-13 (distortion curves), and a peak working load current of ±200mA, define the operating range for the KIA6419. The operating range is further defined in terms of allowable load power in Figure 14 for loads of 8.0Ω, 16Ω, and 32Ω. The left (ascending) portion of each of the three curves is defined by the power level at which 10% distortion occurs. The center flat portion of each curve is defined by the maximum output current capability of the KIA6419. The right (descending) portion of each curve is defined by the maxiumum internal power dissipation of the IC at 25℃. At higher ambient temperatures, the maximum load power must be reduced according to the above equations. Operating the device beyond the current and junction temperature limits will degrade long term reliability.

LAYOUT CONSIDERATIONS

Normally a snubber is not needed at the output of the KIA6419 unlike many other audio amplifiers. However, the PC board layout, stray capacitances, and the manner in which the speaker wires are configured, may dictate otherwise. Generally the speaker wires should be twisted tightly, and be not more than a few inches in length.

FIGURE2-AMPLIFIER #1 OPEN LOOP GAIN AND PHASE

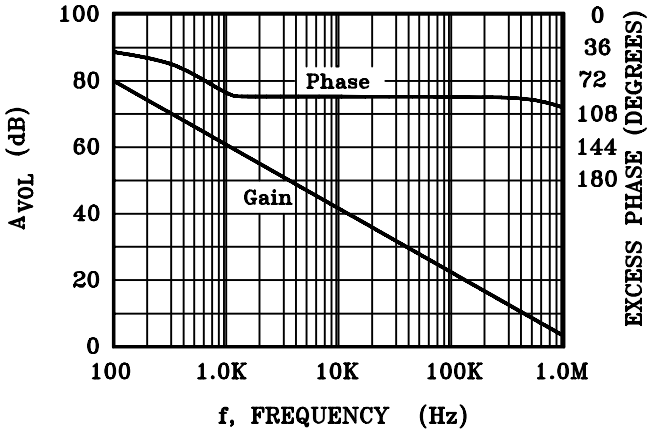
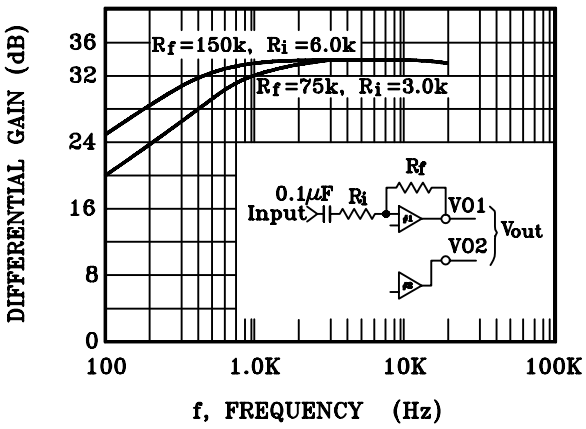


FIGURE3-DIFFERENTIAL GAIN versus FREQUENCY



POWER SUPPLY REJECTION versus FREQUENCY

FIGURE4-C2=10μF

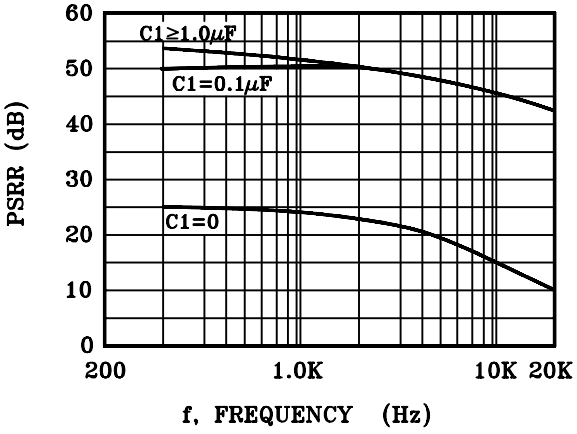


FIGURE5-C2=5.0μF

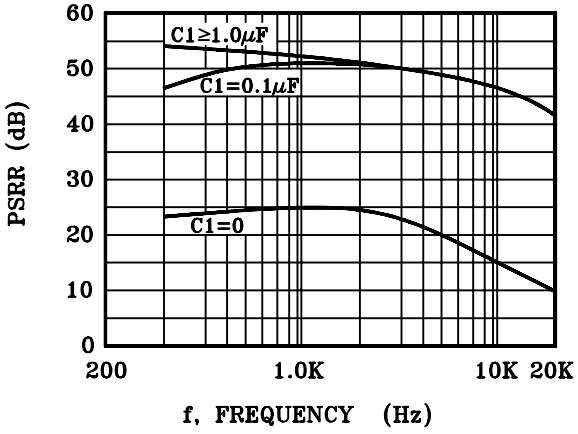


FIGURE6-C2=1.0μF

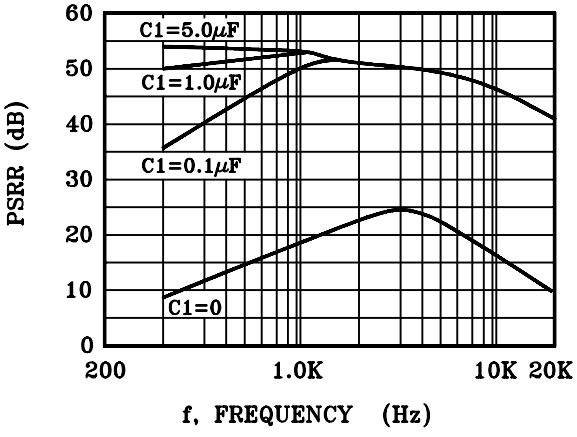


FIGURE7-C2=0

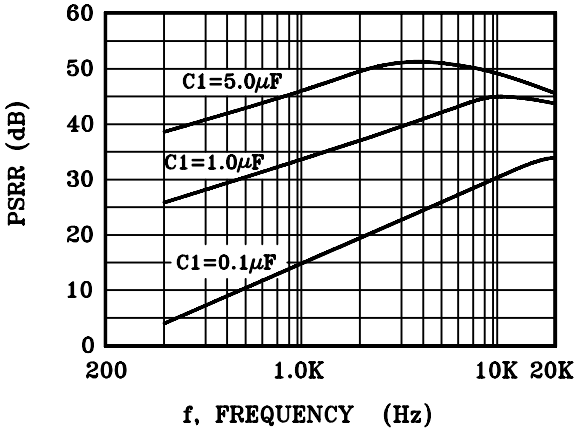


FIGURE8-DEVICE DISSIPATION
8.0Ω LOAD

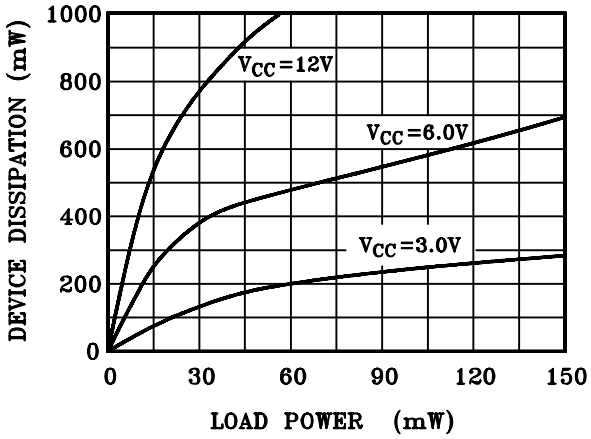


FIGURE9-DEVICE DISSIPATION
16Ω LOAD

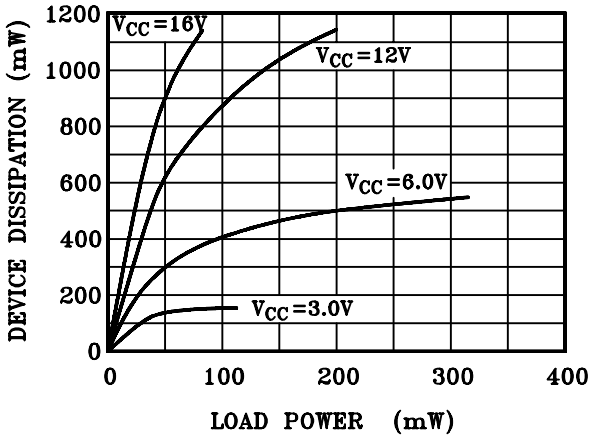


FIGURE10-DEVICE DISSIPATION
32Ω LOAD

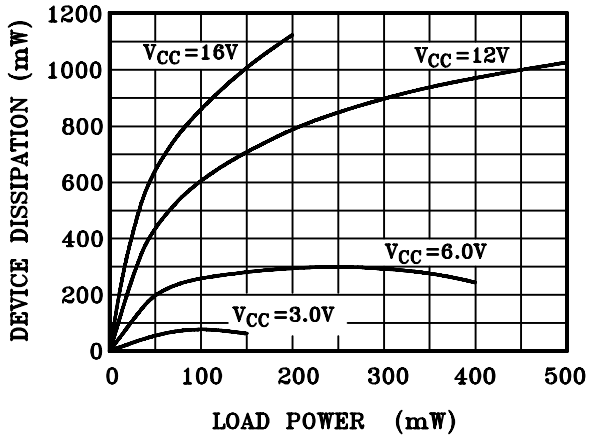


FIGURE11-DISTORTION versus POWER
f=1.0kHz,AVD=34dB

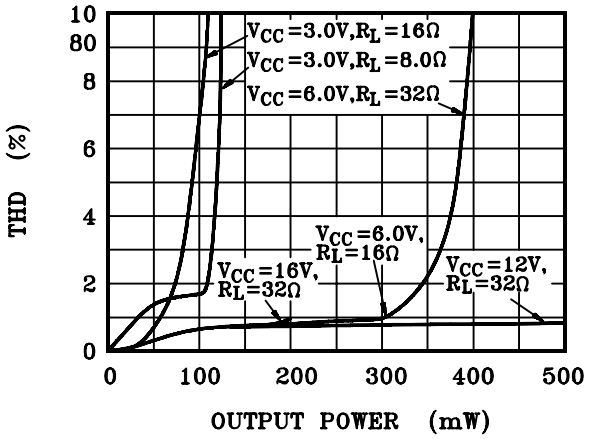


FIGURE12-DISTORTION versus POWER
f=3.0kHz,AVD=34dB

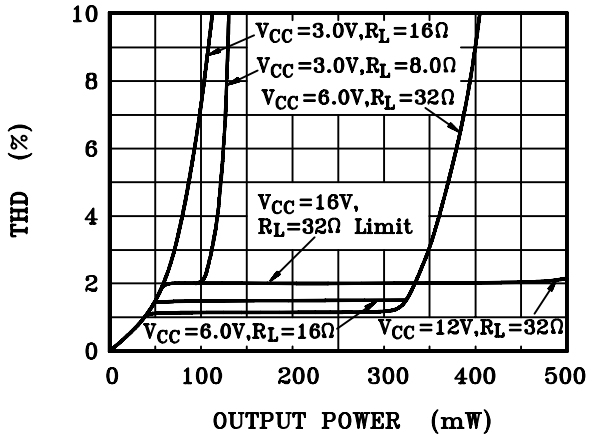


FIGURE13-DISTORTION versus POWER
f=1,3.0kHz,AVD=12dB

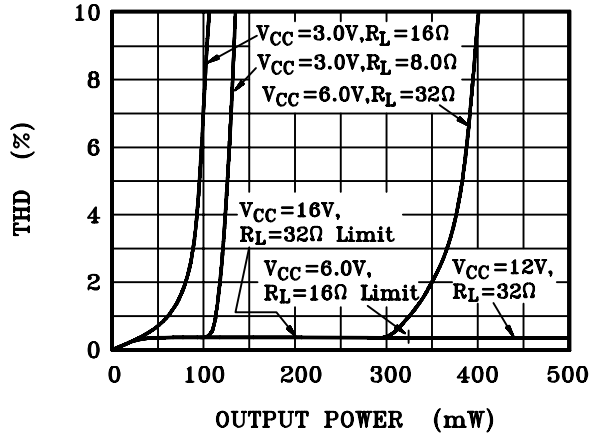


FIGURE14-MAXIMUM ALLOWABLE LOAD POWER

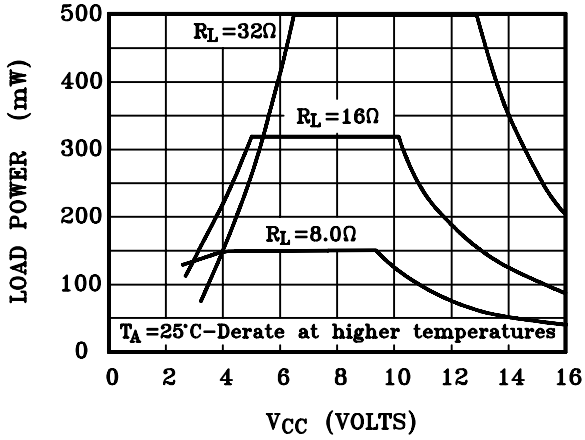


FIGURE15-POWER SUPPLY CURRENT

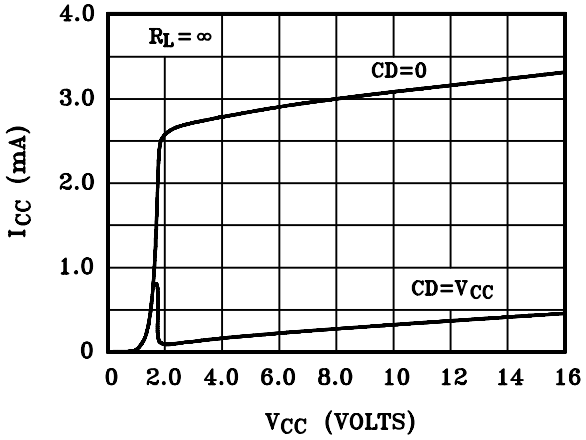


FIGURE16-SMALL SIGNAL RESPONSE

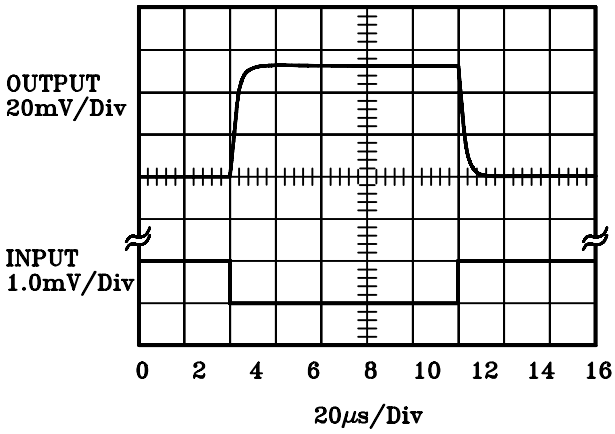


FIGURE17-LARGE SIGNAL RESPONSE

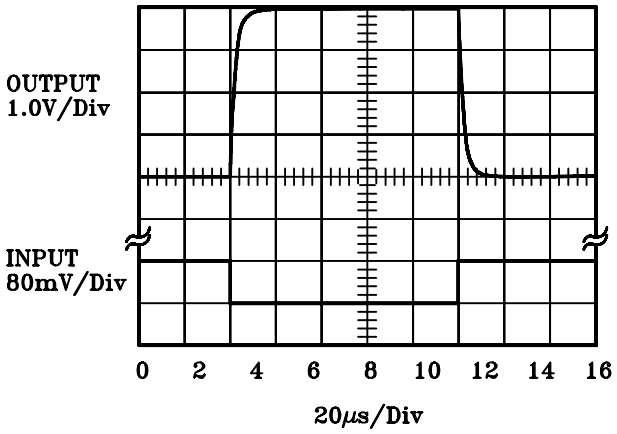


FIGURE18-V_{CC} -V_{OH} @V01,V02 versus LOAD CURRENT

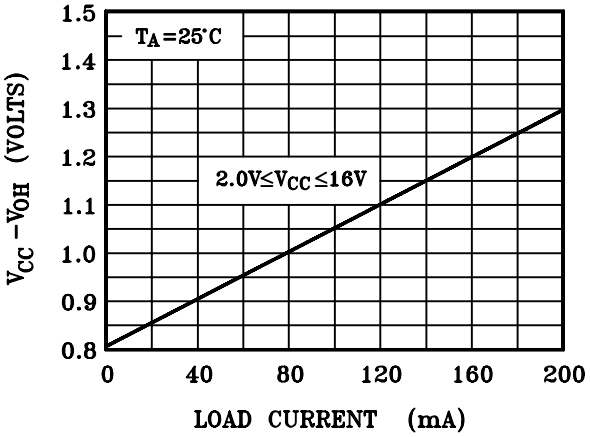


FIGURE19-V_{OL} @V01,V02 versus LOAD CURRENT

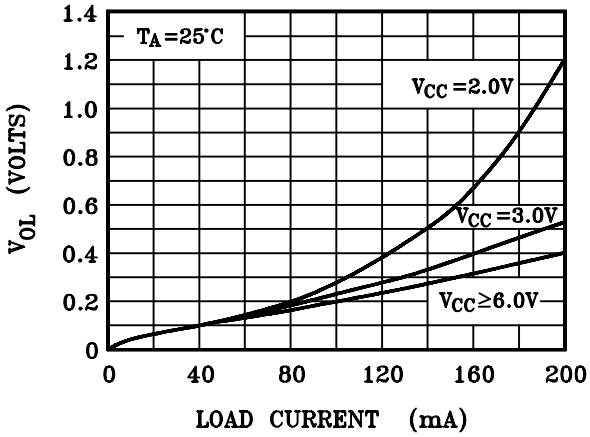


FIGURE20-INPUT CHARACTERISTICS @ CD (PIN 1)

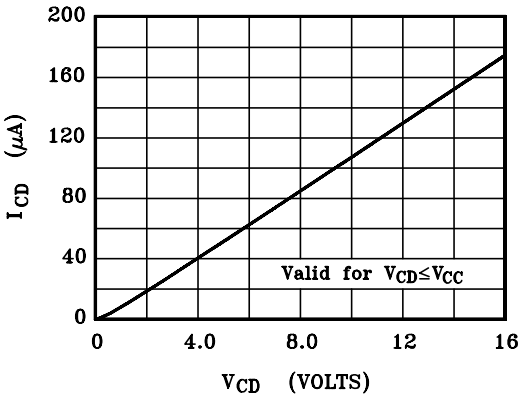
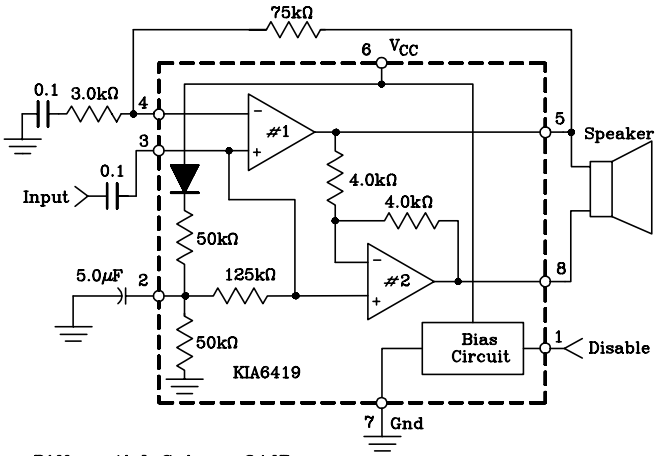


FIGURE21-AUDIO AMPLIFIER WITH HIGH INPUT IMPEDANCE



Differential Gain = 34dB
Frequency Response : See Figure 3
Input Impedance = 125kΩ
PSRR = 50dB

FIGURE22-AUDIO AMPLIFIER WITH BASS SUPPRESSION

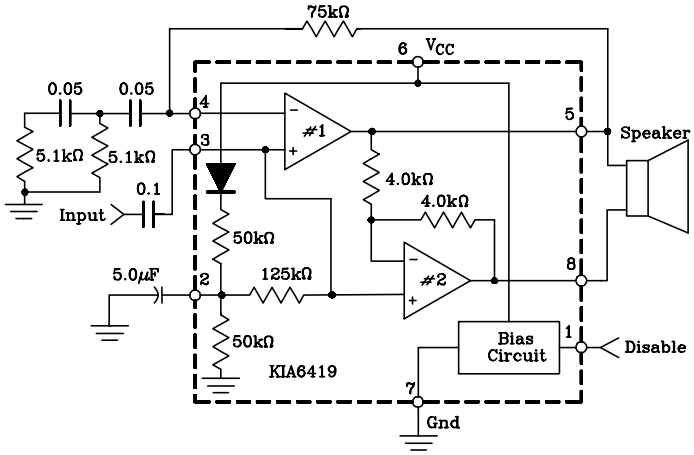


FIGURE23-FREQUENCY RESPONSE OF FUGURE22

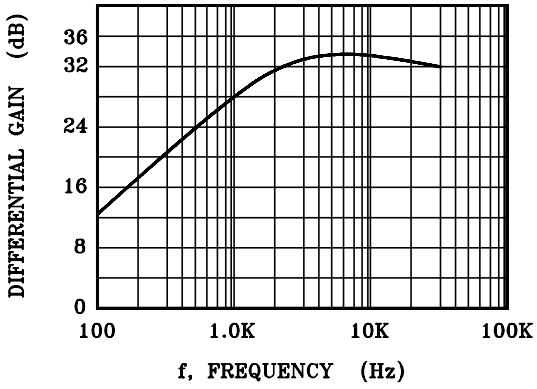


FIGURE24-AUDIO AMPLIFIER WITH BANDPASS

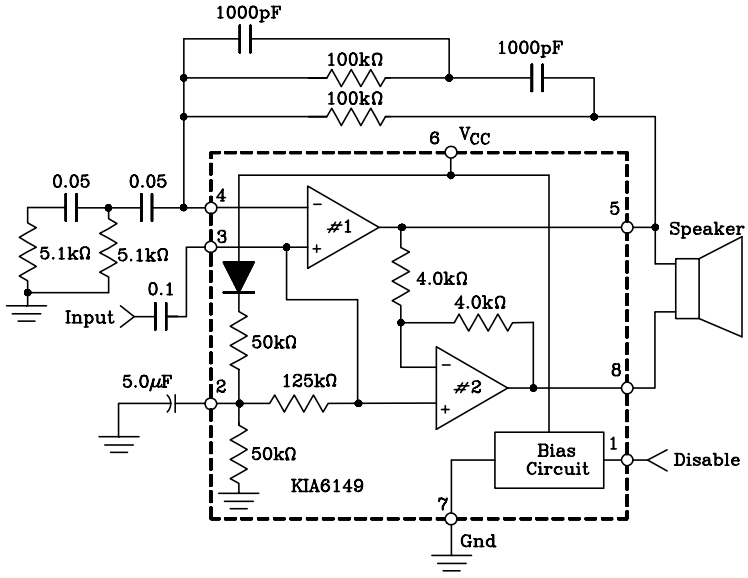


FIGURE25-FREQUENCY RESPONSE OF FIGURE24

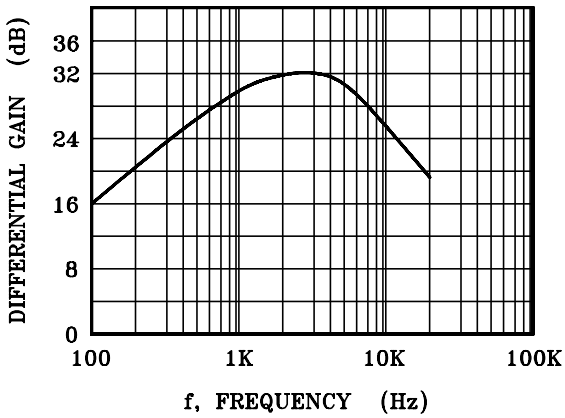
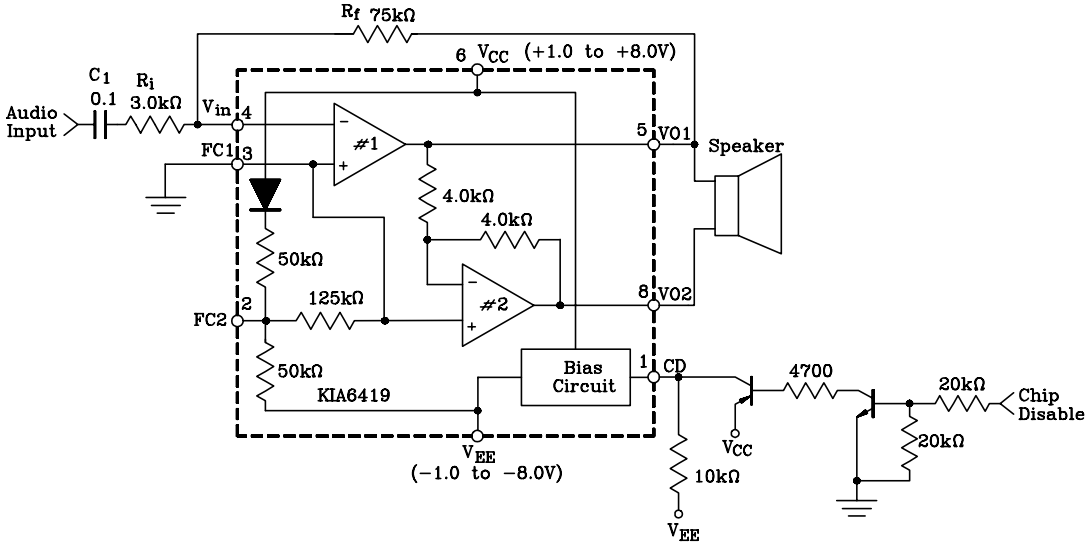


FIGURE26-SPLIT SUPPLY OPERATION



NOTE : If V_{CC} and V_{EE} are not symmertrical about ground then FC1 must be connected through a capacitor to ground as shown on the front page.