

# N-channel enhancement mode TrenchMOS™ transistor

IRFZ44NS

## GENERAL DESCRIPTION

N-channel enhancement mode standard level field-effect power transistor in a surface mounting plastic envelope using 'trench' technology. The device features very low on-state resistance and has integral zener diodes giving ESD protection up to 2kV. It is intended for use in switched mode power supplies and general purpose switching applications.

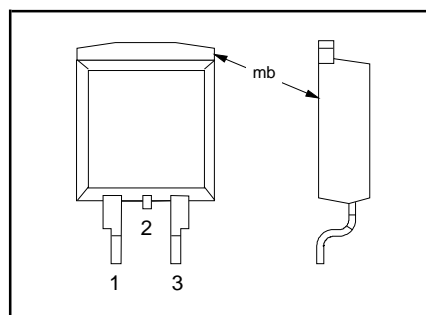
## QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
$V_{DS}$	Drain-source voltage	55	V
$I_D$	Drain current (DC)	49	A
$P_{tot}$	Total power dissipation	110	W
$T_j$	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance $V_{GS} = 10\text{ V}$	22	mΩ

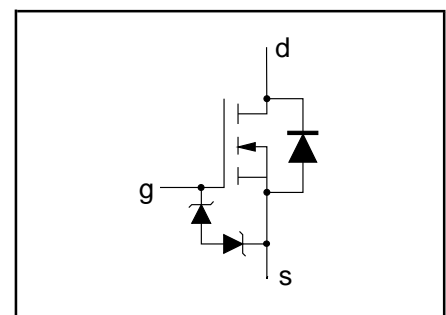
## PINNING - SOT404 (D<sup>2</sup>PAK)

PIN	DESCRIPTION
1	gate
2	drain
3	source
mb	drain

## PIN CONFIGURATION



## SYMBOL



## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{DS}$	Drain-source voltage	-	-	55	V
$V_{DGR}$	Drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$	-	55	V
$\pm V_{GS}$	Gate-source voltage	-	-	20	V
$I_D$	Drain current (DC)	$T_{mb} = 25\text{ }^\circ\text{C}$	-	49	A
$I_D$	Drain current (DC)	$T_{mb} = 100\text{ }^\circ\text{C}$	-	35	A
$I_{DM}$	Drain current (pulse peak value)	$T_{mb} = 25\text{ }^\circ\text{C}$	-	160	A
$P_{tot}$	Total power dissipation	$T_{mb} = 25\text{ }^\circ\text{C}$	-	110	W
$T_{stg}, T_j$	Storage & operating temperature	-	- 55	175	°C

## ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_C$	Electrostatic discharge capacitor voltage, all pins	Human body model (100 pF, 1.5 kΩ)	-	2	kV

## THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j-mb}$	Thermal resistance junction to mounting base	-	-	1.4	K/W
$R_{th\ j-a}$	Thermal resistance junction to ambient	Minimum footprint, FR4 board	50	-	K/W

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### STATIC CHARACTERISTICS

T<sub>j</sub> = 25°C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V <sub>(BR)DSS</sub>	Drain-source breakdown voltage	V <sub>GS</sub> = 0 V; I <sub>D</sub> = 0.25 mA; T <sub>j</sub> = -55°C	55 50	- -	- -	V V
V <sub>GS(TO)</sub>	Gate threshold voltage	V <sub>DS</sub> = V <sub>GS</sub> ; I <sub>D</sub> = 1 mA T <sub>j</sub> = 175°C T <sub>j</sub> = -55°C	2.0 1.0 -	3.0 -	4.0 -	V V V
I <sub>DSS</sub>	Zero gate voltage drain current	V <sub>DS</sub> = 55 V; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 175°C	-	0.05	10	μA
I <sub>GSS</sub>	Gate source leakage current	V <sub>GS</sub> = ±10 V; V <sub>DS</sub> = 0 V T <sub>j</sub> = 175°C	-	0.04	1	μA
±V <sub>(BR)GSS</sub>	Gate source breakdown voltage	I <sub>G</sub> = ±1 mA; T <sub>j</sub> = 175°C	16	-	-	V
R <sub>DS(ON)</sub>	Drain-source on-state resistance	V <sub>GS</sub> = 10 V; I <sub>D</sub> = 25 A T <sub>j</sub> = 175°C	-	15	22	mΩ
			-	-	42	mΩ

### DYNAMIC CHARACTERISTICS

T<sub>mb</sub> = 25°C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g <sub>fs</sub>	Forward transconductance	V <sub>DS</sub> = 25 V; I <sub>D</sub> = 25 A	6	-	-	S
C <sub>iss</sub>	Input capacitance	V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 25 V; f = 1 MHz	-	1350	1800	pF
C <sub>oss</sub>	Output capacitance		-	330	400	pF
C <sub>rss</sub>	Feedback capacitance		-	155	215	pF
Q <sub>g</sub>	Total gate charge	V <sub>DD</sub> = 44 V; I <sub>D</sub> = 50 A; V <sub>GS</sub> = 10 V	-	-	62	nC
Q <sub>gs</sub>	Gate-source charge		-	-	15	nC
Q <sub>gd</sub>	Gate-drain (miller) charge		-	-	26	nC
t <sub>d on</sub>	Turn-on delay time	V <sub>DD</sub> = 30 V; I <sub>D</sub> = 25 A;	-	18	26	ns
t <sub>r</sub>	Turn-on rise time	V <sub>GS</sub> = 10 V; R <sub>G</sub> = 10 Ω	-	50	75	ns
t <sub>d off</sub>	Turn-off delay time	Resistive load	-	40	50	ns
t <sub>f</sub>	Turn-off fall time		-	30	40	ns
L <sub>d</sub>	Internal drain inductance	Measured from upper edge of drain tab to centre of die	-	2.5	-	nH
L <sub>s</sub>	Internal source inductance	Measured from source lead soldering point to source bond pad	-	7.5	-	nH

### REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T<sub>j</sub> = 25°C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I <sub>DR</sub>	Continuous reverse drain current		-	-	49	A
I <sub>DRM</sub>	Pulsed reverse drain current		-	-	160	A
V <sub>SD</sub>	Diode forward voltage	I <sub>F</sub> = 25 A; V <sub>GS</sub> = 0 V I <sub>F</sub> = 40 A; V <sub>GS</sub> = 0 V	-	0.95 1.0	1.2 -	V
t <sub>rr</sub>	Reverse recovery time	I <sub>F</sub> = 40 A; -di <sub>F</sub> /dt = 100 A/μs; V <sub>GS</sub> = -10 V; V <sub>R</sub> = 30 V	-	47	-	ns
Q <sub>rr</sub>	Reverse recovery charge		-	0.15	-	μC

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**AVALANCHE LIMITING VALUE**

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$W_{DSS}$	Drain-source non-repetitive unclamped inductive turn-off energy	$I_D = 45\text{ A}; V_{DD} \leq 25\text{ V}; V_{GS} = 10\text{ V}; R_{GS} = 50\ \Omega; T_{mb} = 25\text{ }^\circ\text{C}$	-	-	110	mJ



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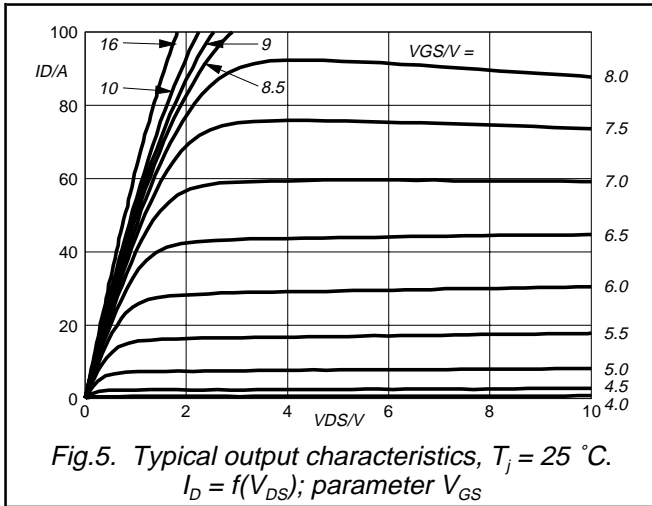


Fig.5. Typical output characteristics,  $T_j = 25\text{ }^\circ\text{C}$ .  
 $I_D = f(V_{DS})$ ; parameter  $V_{GS}$

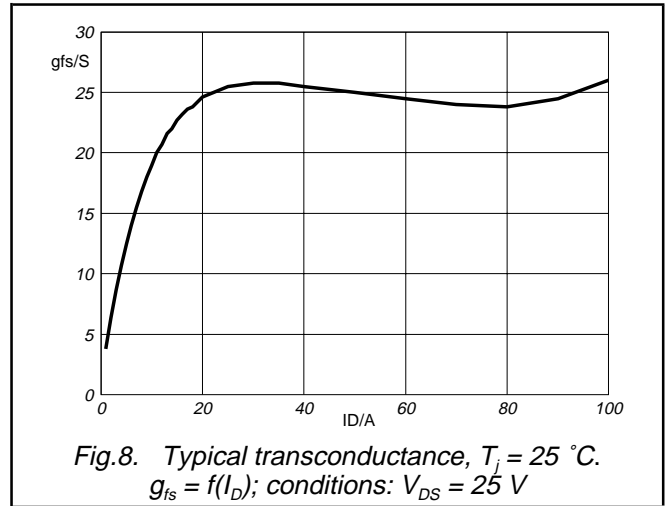


Fig.8. Typical transconductance,  $T_j = 25\text{ }^\circ\text{C}$ .  
 $g_{fs} = f(I_D)$ ; conditions:  $V_{DS} = 25\text{ V}$

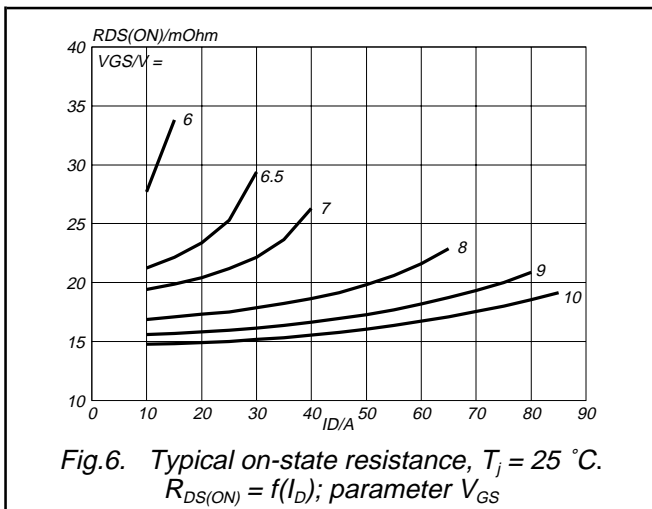


Fig.6. Typical on-state resistance,  $T_j = 25\text{ }^\circ\text{C}$ .  
 $R_{DS(ON)} = f(I_D)$ ; parameter  $V_{GS}$

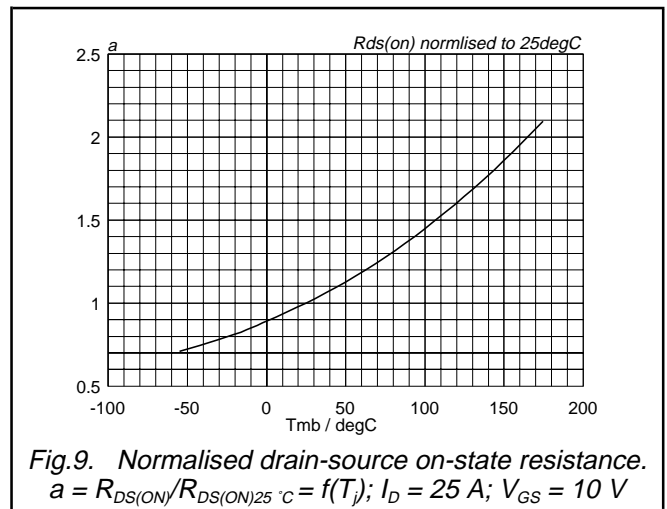


Fig.9. Normalised drain-source on-state resistance.  
 $a = R_{DS(ON)}/R_{DS(ON)25\text{ }^\circ\text{C}} = f(T_j)$ ;  $I_D = 25\text{ A}$ ;  $V_{GS} = 10\text{ V}$

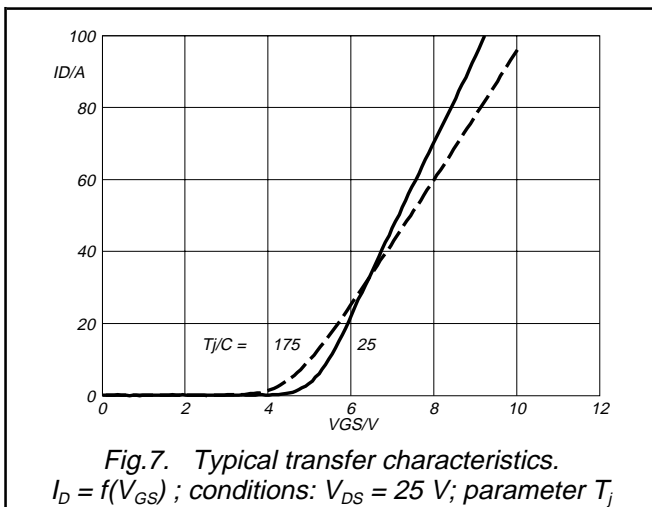


Fig.7. Typical transfer characteristics.  
 $I_D = f(V_{GS})$ ; conditions:  $V_{DS} = 25\text{ V}$ ; parameter  $T_j$

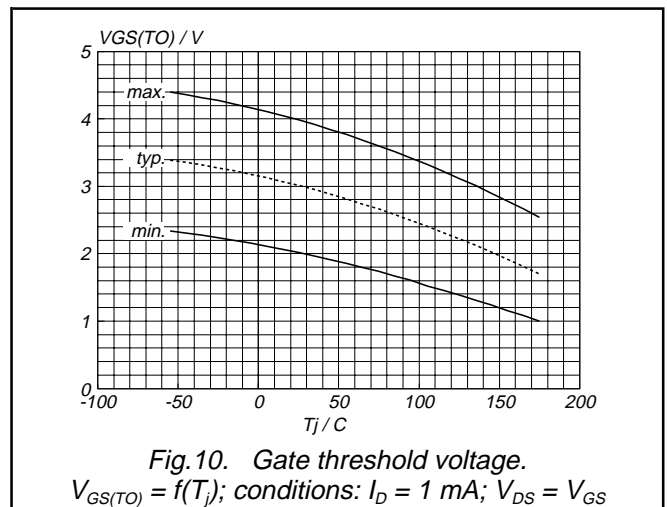
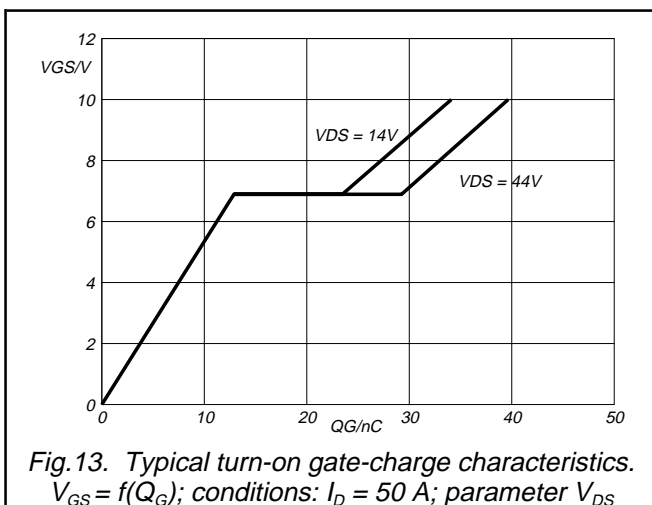
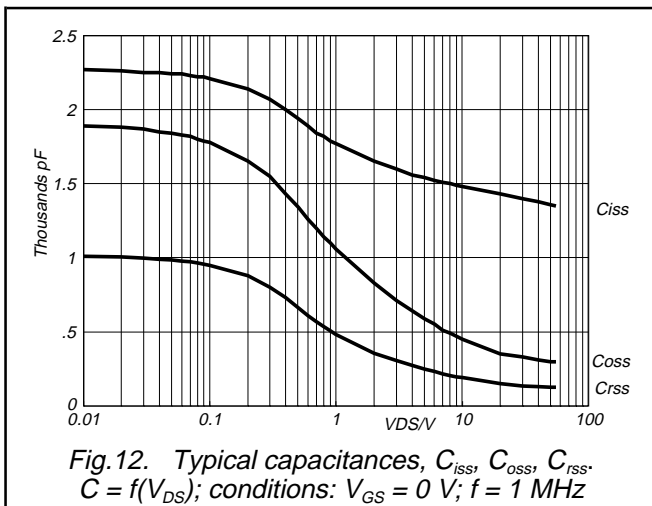


Fig.10. Gate threshold voltage.  
 $V_{GS(TO)} = f(T_j)$ ; conditions:  $I_D = 1\text{ mA}$ ;  $V_{DS} = V_{GS}$

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Fig.17. Switching test circuit.

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MECHANICAL DATA

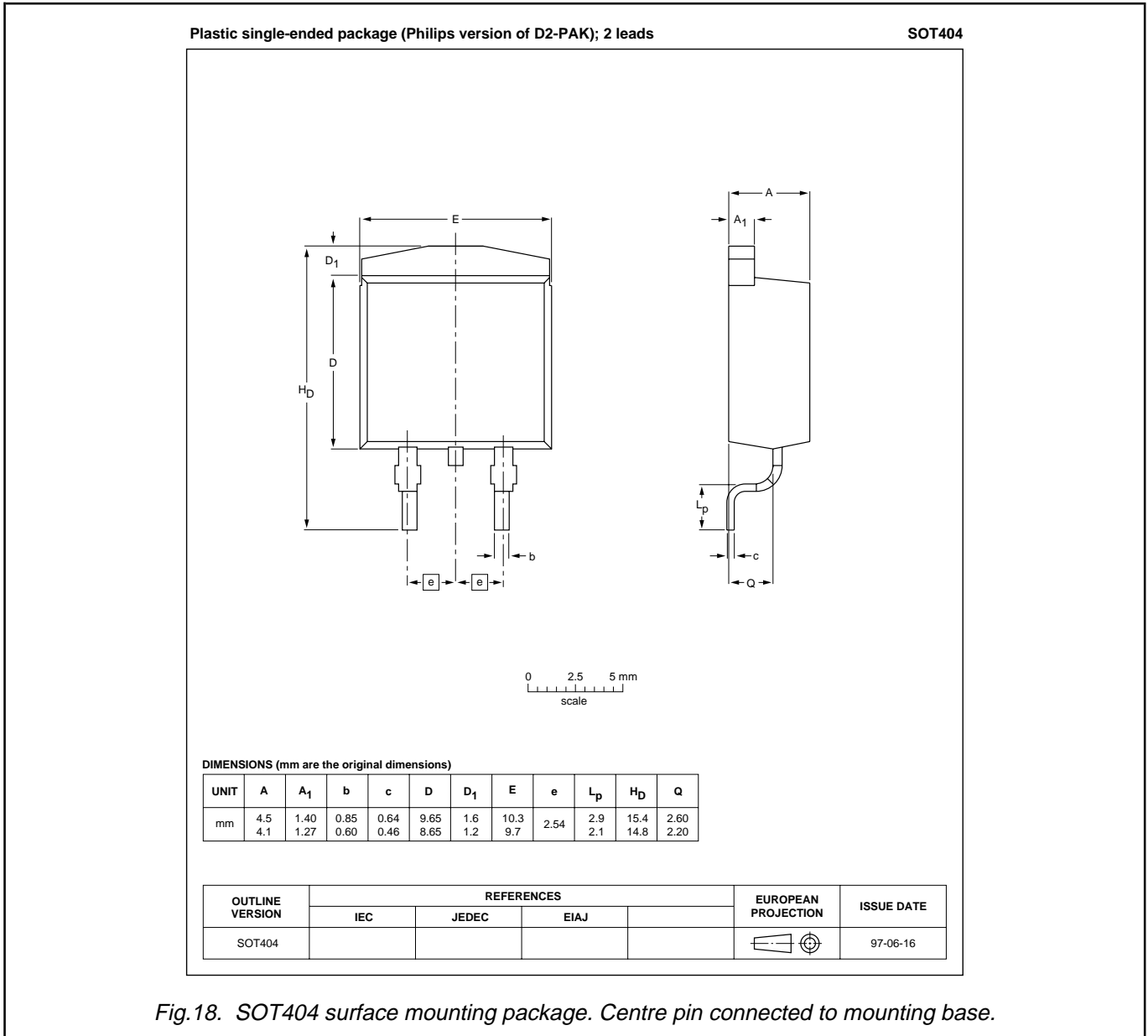


Fig.18. SOT404 surface mounting package. Centre pin connected to mounting base.

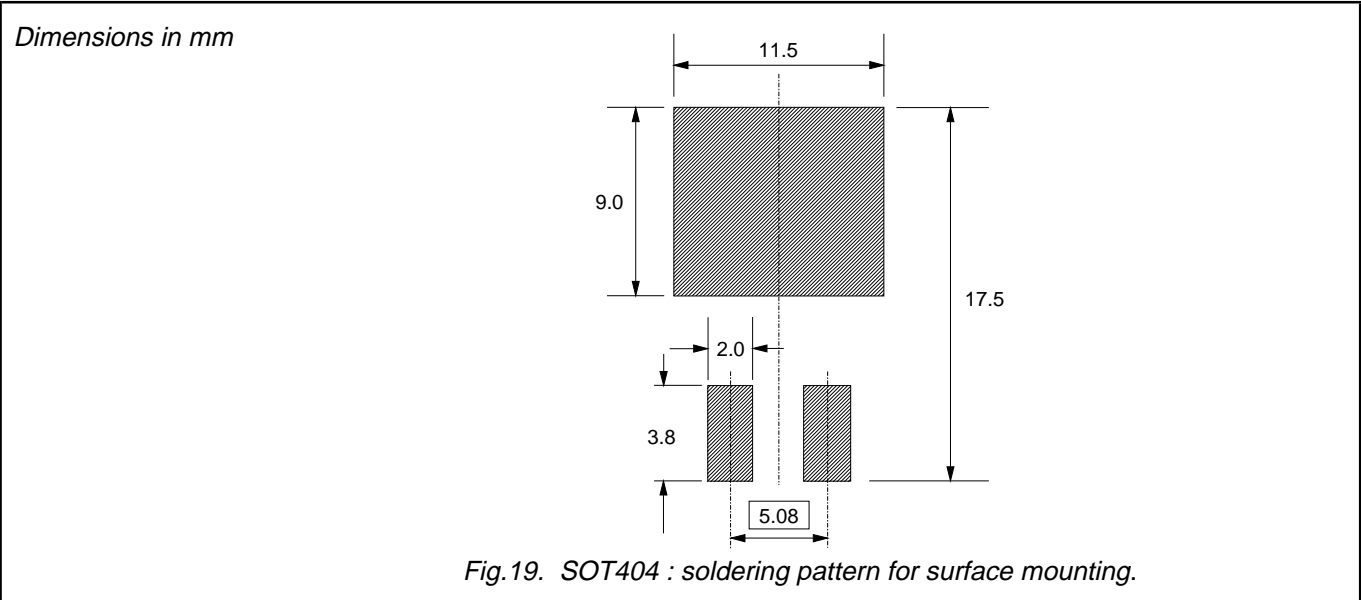
Notes

1. This product is supplied in anti-static packaging. The gate-source input must be protected against static discharge during transport or handling.
2. Refer to SMD Footprint Design and Soldering Guidelines, Data Handbook SC18.
3. Epoxy meets UL94 V0 at 1/8".

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**MOUNTING INSTRUCTIONS**



**DEFINITIONS**

<b>Data sheet status</b>	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
<b>Limiting values</b>	
Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
<b>Application information</b>	
Where application information is given, it is advisory and does not form part of the specification.	
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