

April 1997

## 70A, 600V, UFS Series N-Channel IGBT

### Features

- 70A, 600V,  $T_C = 25^\circ\text{C}$
- 600V Switching SOA Capability
- Typical Fall Time . . . . . 100ns at  $T_J = 150^\circ\text{C}$
- Short Circuit Rating
- Low Conduction Loss

### Ordering Information

PART NUMBER	PACKAGE	BRAND
HGTG40N60B3	TO-247	G40N60B3

NOTE: When ordering, use the entire part number.

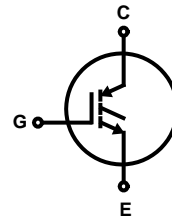
### Description

The HGTG40N60B3 is a MOS gated high voltage switching device combining the best features of MOSFETs and bipolar transistors. The device has the high input impedance of a MOSFET and the low on-state conduction loss of a bipolar transistor. The much lower on-state voltage drop varies only moderately between  $25^\circ\text{C}$  and  $150^\circ\text{C}$ .

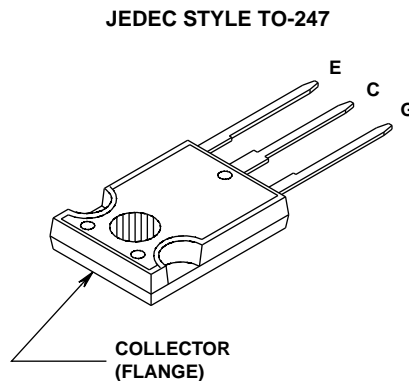
The IGBT is ideal for many high voltage switching applications operating at moderate frequencies where low conduction losses are essential, such as: AC and DC motor controls, power supplies and drivers for solenoids, relays and contactors.

Formerly Developmental Type TA49052.

### Symbol



### Packaging



#### HARRIS SEMICONDUCTOR IGBT PRODUCT IS COVERED BY ONE OR MORE OF THE FOLLOWING U.S. PATENTS

4,364,073	4,417,385	4,430,792	4,443,931	4,466,176	4,516,143	4,532,534	4,567,641
4,587,713	4,598,461	4,605,948	4,618,872	4,620,211	4,631,564	4,639,754	4,639,762
4,641,162	4,644,637	4,682,195	4,684,413	4,694,313	4,717,679	4,743,952	4,783,690
4,794,432	4,801,986	4,803,533	4,809,045	4,809,047	4,810,665	4,823,176	4,837,606
4,860,080	4,883,767	4,888,627	4,890,143	4,901,127	4,904,609	4,933,740	4,963,951
4,969,027							

## HGTG40N60B3

### Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ , Unless Otherwise Specified

	HGTG40N60B3	UNITS
Collector to Emitter Voltage . . . . .	600	V
Collector Current Continuous		
At $T_C = 25^\circ\text{C}$ . . . . .	70	A
At $T_C = 110^\circ\text{C}$ . . . . .	40	A
Collector Current Pulsed (Note 1) . . . . .	330	A
Gate to Emitter Voltage Continuous . . . . .	$\pm 20$	V
Gate to Emitter Voltage Pulsed . . . . .	$\pm 30$	V
Switching Safe Operating Area at $T_J = 150^\circ\text{C}$ , Figure 2 . . . . .	100A at 600V	
Power Dissipation Total at $T_C = 25^\circ\text{C}$ . . . . .	290	W
Power Dissipation Derating $T_C > 25^\circ\text{C}$ . . . . .	2.33	$\text{W}/^\circ\text{C}$
Reverse Voltage Avalanche Energy . . . . .	100	mJ
Operating and Storage Junction Temperature Range . . . . .	-55 to 150	$^\circ\text{C}$
Maximum Lead Temperature for Soldering . . . . .	260	$^\circ\text{C}$
Short Circuit Withstand Time (Note 2) at $V_{GE} = 15\text{V}$ . . . . .	2	$\mu\text{s}$
Short Circuit Withstand Time (Note 2) at $V_{GE} = 10\text{V}$ . . . . .	10	$\mu\text{s}$

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

**NOTES:**

1. Pulse width limited by maximum junction temperature.
2.  $V_{CE(PK)} = 360\text{V}$ ,  $T_J = 125^\circ\text{C}$ ,  $R_{GE} = 3\Omega$ .

### Electrical Specifications $T_C = 25^\circ\text{C}$ , Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Collector to Emitter Breakdown Voltage	$BV_{CES}$	$I_C = 250\mu\text{A}$ , $V_{GE} = 0\text{V}$		600	-	-	V
Emitter to Collector Breakdown Voltage	$BV_{ECS}$	$I_C = 10\text{mA}$ , $V_{GE} = 0\text{V}$		15	25	-	V
Collector to Emitter Leakage Current	$I_{CES}$	$V_{CE} = BV_{CES}$	$T_C = 25^\circ\text{C}$	-	-	100	$\mu\text{A}$
		$V_{CE} = BV_{CES}$	$T_C = 150^\circ\text{C}$	-	-	6.0	mA
Collector to Emitter Saturation Voltage	$V_{CE(SAT)}$	$I_C = I_{C110}$ , $V_{GE} = 15\text{V}$	$T_C = 25^\circ\text{C}$	-	1.4	2.0	V
			$T_C = 150^\circ\text{C}$	-	1.5	2.3	V
Gate to Emitter Threshold Voltage	$V_{GE(TH)}$	$I_C = 250\mu\text{A}$ , $V_{CE} = V_{GE}$		3.0	4.8	6.0	V
Gate to Emitter Leakage Current	$I_{GES}$	$V_{GE} = \pm 20\text{V}$		-	-	$\pm 100$	nA
Switching SOA	SSOA	$T_J = 150^\circ\text{C}$ $R_G = 3\Omega$ $V_{GE} = 15\text{V}$ $L = 100\mu\text{H}$	$V_{CE} = 480\text{V}$	200	-	-	A
			$V_{CE} = 600\text{V}$	100	-	-	A
Gate to Emitter Plateau Voltage	$V_{GEP}$	$I_C = I_{C110}$ , $V_{CE} = 0.5 BV_{CES}$		-	7.5	-	V
On-State Gate Charge	$Q_{g(ON)}$	$I_C = I_{C110}$ , $V_{CE} = 0.5 BV_{CES}$	$V_{GE} = 15\text{V}$	-	250	330	nC
			$V_{GE} = 20\text{V}$	-	335	435	nC

# HGTG40N60B3

## Electrical Specifications $T_C = 25^\circ\text{C}$ , Unless Otherwise Specified (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Current Turn-On Delay Time	$t_{d(ON)I}$	IGBT and Diode Both at $T_J = 25^\circ\text{C}$ $I_{CE} = I_{C110}$ $V_{CE} = 0.8 V_{CES}$ $V_{GE} = 15\text{V}$ $R_G = 3\Omega$ $L = 100\mu\text{H}$ Test Circuit - Figure 17	-	47	-	ns
Current Rise Time	$t_{rI}$		-	35	-	ns
Current Turn-Off Delay Time	$t_{d(OFF)I}$		-	170	200	ns
Current Fall Time	$t_{fI}$		-	50	100	ns
Turn-On Energy	$E_{ON}$		-	1050	1200	$\mu\text{J}$
Turn-Off Energy (Note 1)	$E_{OFF}$		-	800	1400	$\mu\text{J}$
Current Turn-On Delay Time	$t_{d(ON)I}$	IGBT and Diode Both at $T_J = 150^\circ\text{C}$ $I_{CE} = I_{C110}$ $V_{CE} = 0.8 V_{CES}$ $V_{GE} = 15\text{V}$ $R_G = 3\Omega$ $L = 100\mu\text{H}$ Test Circuit (Figure 17)	-	47	-	ns
Current Rise Time	$t_{rI}$		-	35	-	ns
Current Turn-Off Delay Time	$t_{d(OFF)I}$		-	285	375	ns
Current Fall Time	$t_{fI}$		-	100	200	ns
Turn-On Energy	$E_{ON}$		-	1850	-	$\mu\text{J}$
Turn-Off Energy (Note 1)	$E_{OFF}$		-	2000	-	$\mu\text{J}$
Thermal Resistance Junction To Case	$R_{\theta JC}$		-	-	0.43	$^\circ\text{C/W}$

### NOTE:

- Turn-Off Energy Loss ( $E_{OFF}$ ) is defined as the integral of the instantaneous power loss starting at the trailing edge of the input pulse and ending at the point where the collector current equals zero ( $I_{CE} = 0\text{A}$ ). All devices were tested per JEDEC Standard No. 24-1 Method for Measurement of Power Device Turn-Off Switching Loss. This test method produces the true total Turn-Off Energy Loss. Turn-On losses include losses due to diode recovery.

## Typical Performance Curves (Unless Otherwise Specified)

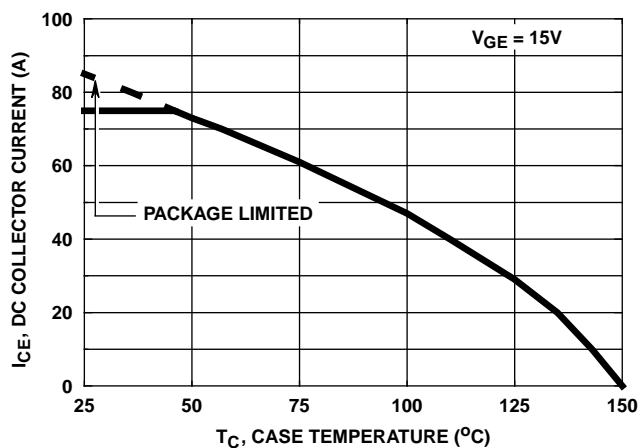


FIGURE 1. DC COLLECTOR CURRENT AS A FUNCTION OF CASE TEMPERATURE

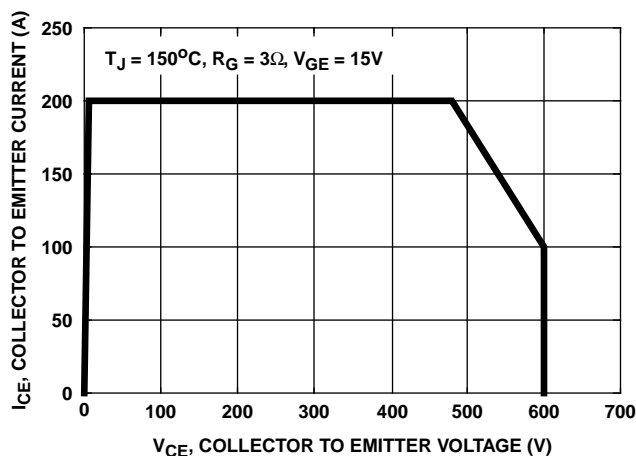


FIGURE 2. MINIMUM SWITCHING SAFE OPERATING AREA

Typical Performance Curves (Unless Otherwise Specified) (Continued)

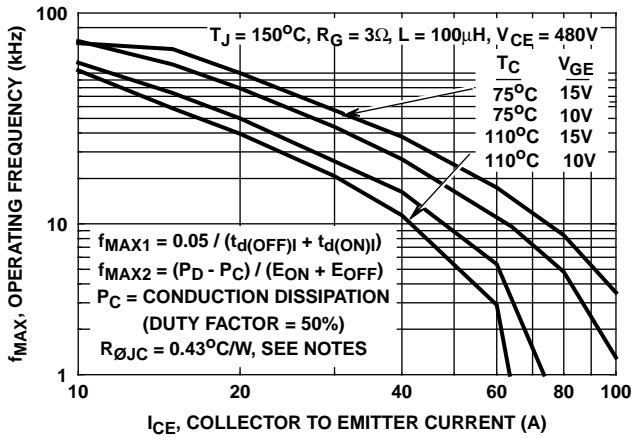


FIGURE 3. OPERATING FREQUENCY AS A FUNCTION OF COLLECTOR TO EMITTER CURRENT

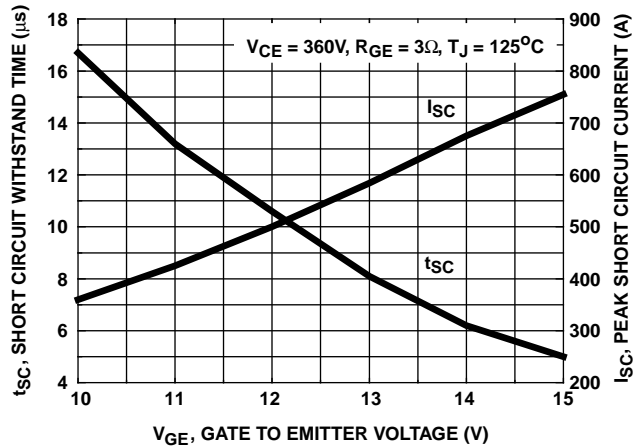


FIGURE 4. SHORT CIRCUIT WITHSTAND TIME

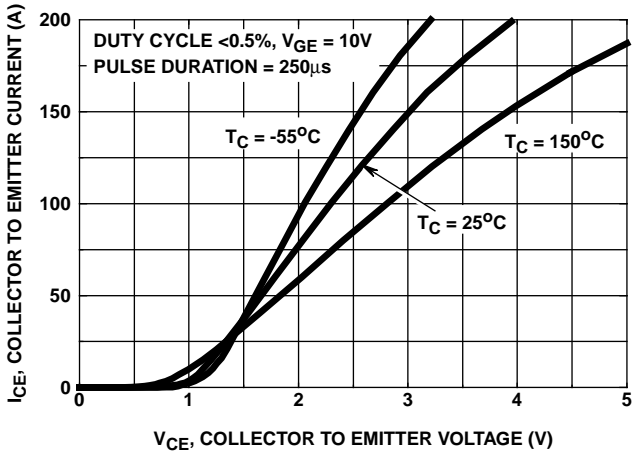


FIGURE 5. COLLECTOR TO EMITTER ON STATE VOLTAGE

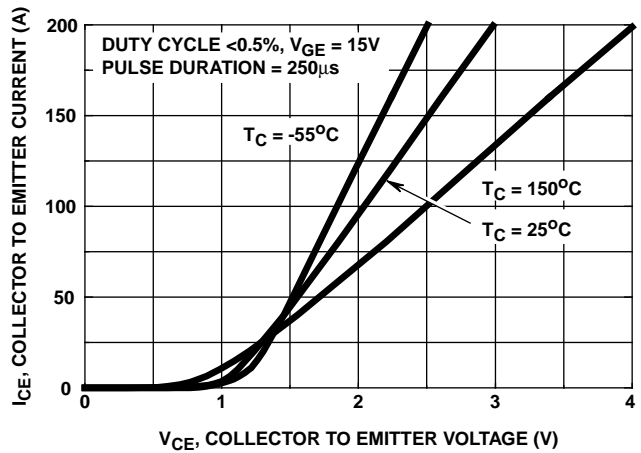


FIGURE 6. COLLECTOR TO EMITTER ON STATE VOLTAGE

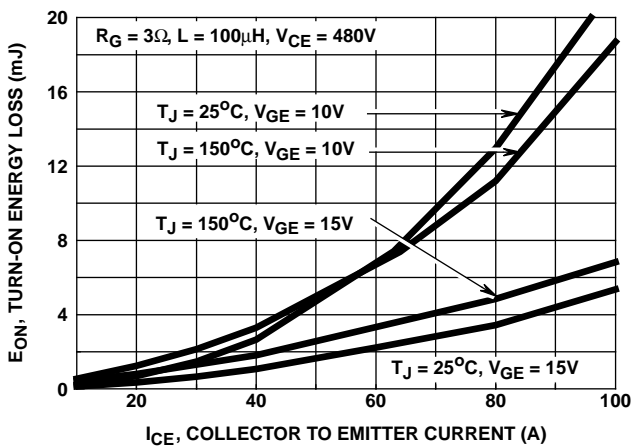


FIGURE 7. TURN-ON ENERGY LOSS AS A FUNCTION OF COLLECTOR TO EMITTER CURRENT

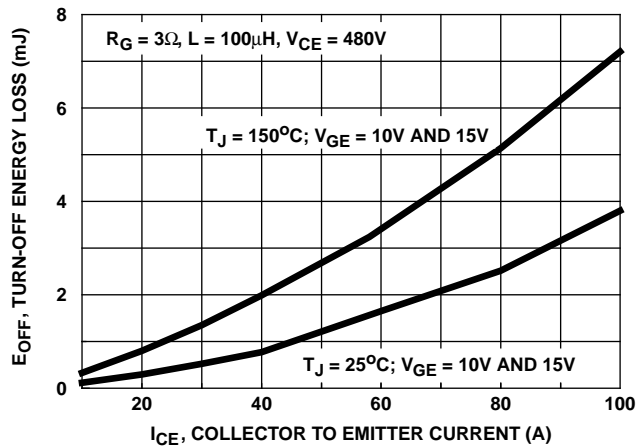


FIGURE 8. TURN-OFF ENERGY LOSS AS A FUNCTION OF COLLECTOR TO EMITTER CURRENT

Typical Performance Curves (Unless Otherwise Specified) (Continued)

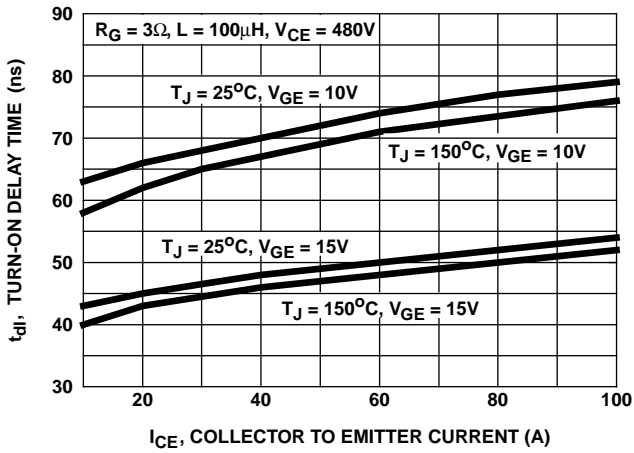


FIGURE 9. TURN-ON DELAY TIME AS A FUNCTION OF COLLECTOR TO EMITTER CURRENT

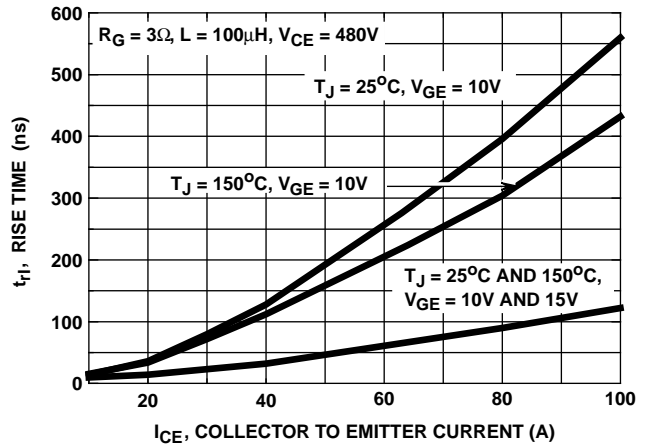


FIGURE 10. TURN-ON RISE TIME AS A FUNCTION OF COLLECTOR TO EMITTER CURRENT

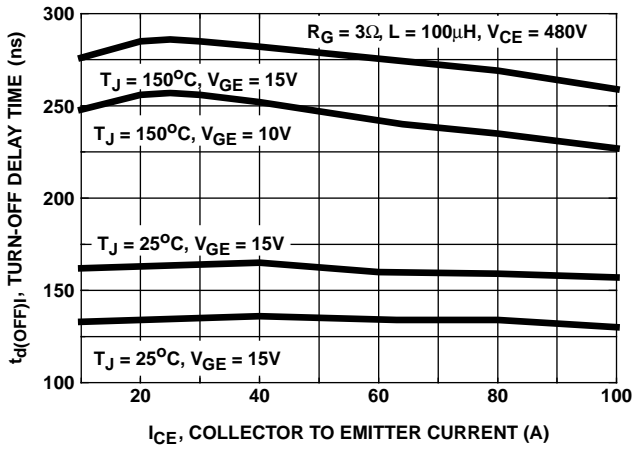


FIGURE 11. TURN-OFF DELAY TIME AS A FUNCTION OF COLLECTOR TO EMITTER CURRENT

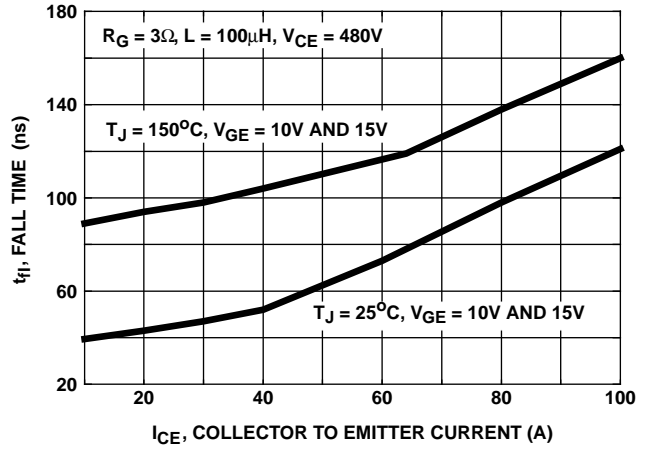


FIGURE 12. FALL TIME AS A FUNCTION OF COLLECTOR TO EMITTER CURRENT

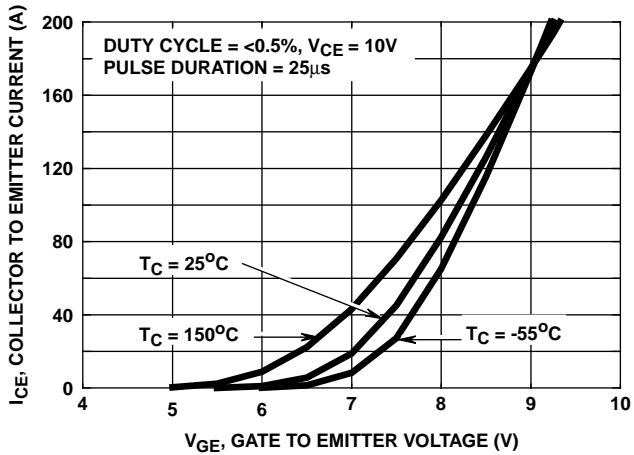


FIGURE 13. TRANSFER CHARACTERISTIC

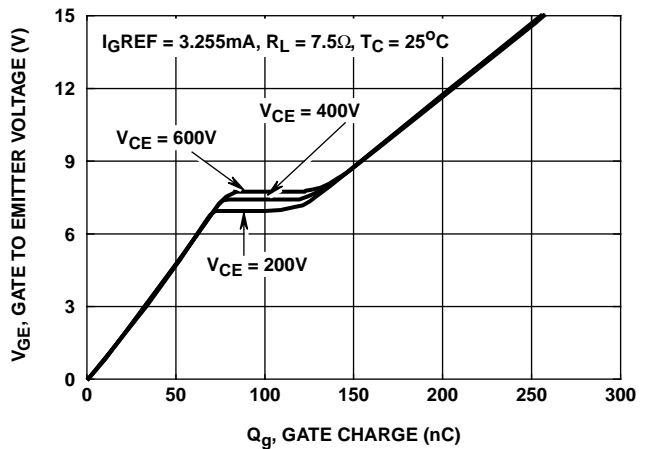


FIGURE 14. GATE CHARGE WAVEFORMS

Typical Performance Curves (Unless Otherwise Specified) (Continued)

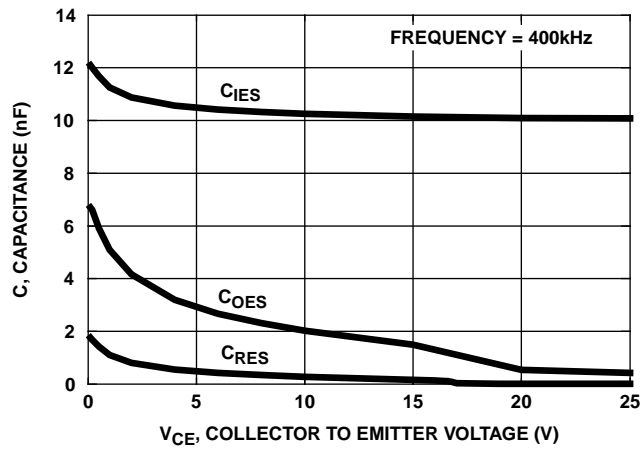


FIGURE 15. CAPACITANCE AS A FUNCTION OF COLLECTOR TO EMITTER VOLTAGE

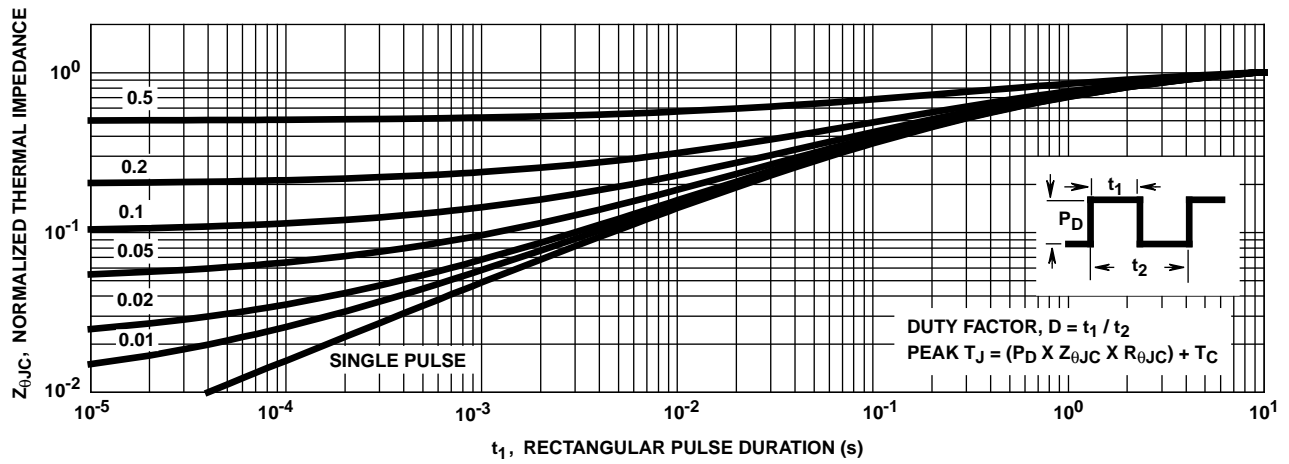


FIGURE 16. NORMALIZED TRANSIENT THERMAL RESPONSE, JUNCTION TO CASE

Test Circuit and Waveforms

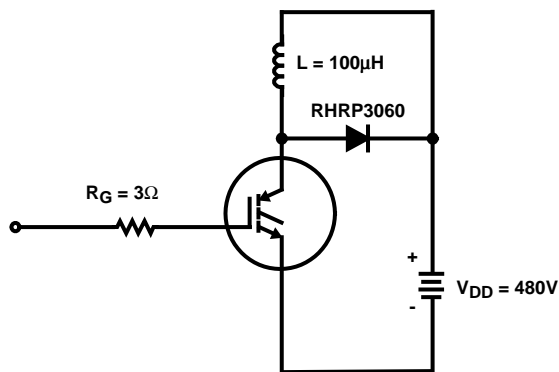


FIGURE 17. INDUCTIVE SWITCHING TEST CIRCUIT

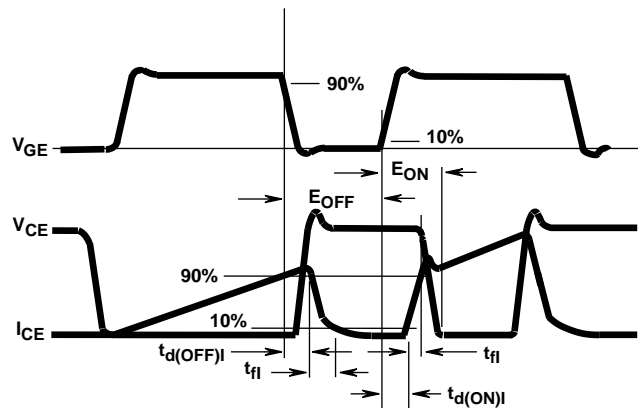


FIGURE 18. SWITCHING TEST WAVEFORMS

### Handling Precautions for IGBT's

Insulated Gate Bipolar Transistors are susceptible to gate-insulation damage by the electrostatic discharge of energy through the devices. When handling these devices, care should be exercised to assure that the static charge built in the handler's body capacitance is not discharged through the device. With proper handling and application procedures, however, IGBT's are currently being extensively used in production by numerous equipment manufacturers in military, industrial and consumer applications, with virtually no damage problems due to electrostatic discharge. IGBT's can be handled safely if the following basic precautions are taken:

1. Prior to assembly into a circuit, all leads should be kept shorted together either by the use of metal shorting springs or by the insertion into conductive material such as "ECCOSORBD LD26™" or equivalent.
2. When devices are removed by hand from their carriers, the hand being used should be grounded by any suitable means - for example, with a metallic wristband.
3. Tips of soldering irons should be grounded.
4. Devices should never be inserted into or removed from circuits with power on.
5. **Gate Voltage Rating** - Never exceed the gate-voltage rating of  $V_{GEM}$ . Exceeding the rated  $V_{GE}$  can result in permanent damage to the oxide layer in the gate region.
6. **Gate Termination** - The gates of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the device due to voltage buildup on the input capacitor due to leakage currents or pickup.
7. **Gate Protection** - These devices do not have an internal monolithic Zener diode from gate to emitter. If gate protection is required an external Zener is recommended.

ECCOSORBD™ is a Trademark of Emerson and Cumming, Inc.

### Operating Frequency Information

Operating frequency information for a typical device (Figure 3) is presented as a guide for estimating device performance for a specific application. Other typical frequency vs collector current ( $I_{CE}$ ) plots are possible using the information shown for a typical unit in Figures 5, 6, 7, 8, 9 and 10. The operating frequency plot (Figure 3) of a typical device shows  $f_{MAX1}$  or  $f_{MAX2}$ ; whichever is smaller at each point. The information is based on measurements of a typical device and is bounded by the maximum rated junction temperature.

$f_{MAX1}$  is defined by  $f_{MAX1} = 0.05 / (t_{d(OFF)I} + t_{d(ON)I})$ . Dead-time (the denominator) has been arbitrarily held to 10% of the on-state time for a 50% duty factor. Other definitions are possible.  $t_{d(OFF)I}$  and  $t_{d(ON)I}$  are defined in Figure 18. Device turn-off delay can establish an additional frequency limiting condition for an application other than  $T_{JMAX}$ .  $t_{d(OFF)I}$  is important when controlling output ripple under a lightly loaded condition.

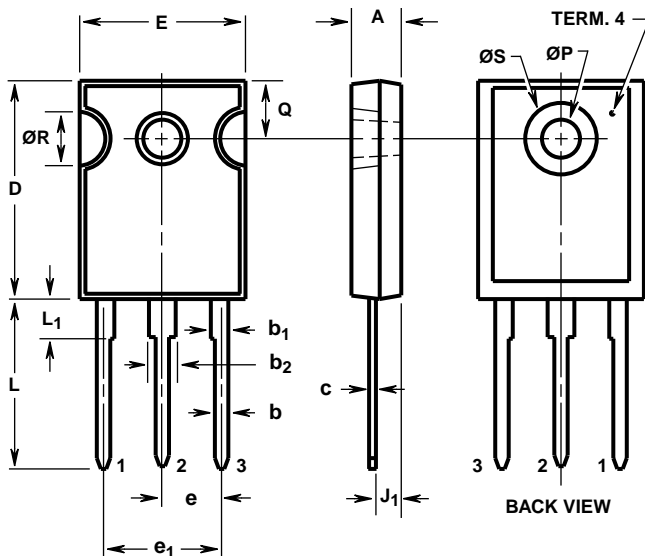
$f_{MAX2}$  is defined by  $f_{MAX2} = (P_D - P_C) / (E_{OFF} + E_{ON})$ . The allowable dissipation ( $P_D$ ) is defined by  $P_D = (T_{JMAX} - T_C) / R_{\theta JC}$ . The sum of device switching and conduction losses must not exceed  $P_D$ . A 50% duty factor was used (Figure 3) and the conduction losses ( $P_C$ ) are approximated by  $P_C = (V_{CE} \times I_{CE}) / 2$ .

$E_{ON}$  and  $E_{OFF}$  are defined in the switching waveforms shown in Figure 18.  $E_{ON}$  is the integral of the instantaneous power loss ( $I_{CE} \times V_{CE}$ ) during turn-on and  $E_{OFF}$  is the integral of the instantaneous power loss ( $I_{CE} \times V_{CE}$ ) during turn-off. All tail losses are included in the calculation for  $E_{OFF}$ ; i.e., the collector current equals zero ( $I_{CE} = 0$ ).

# HGTG40N60B3

## TO-247

### 3 LEAD JEDEC STYLE TO-247 PLASTIC PACKAGE



- LEAD 1 - GATE
- LEAD 2 - COLLECTOR
- LEAD 3 - EMITTER
- TERM. 4 - COLLECTOR

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.180	0.190	4.58	4.82	-
b	0.046	0.051	1.17	1.29	2, 3
b <sub>1</sub>	0.060	0.070	1.53	1.77	1, 2
b <sub>2</sub>	0.095	0.105	2.42	2.66	1, 2
c	0.020	0.026	0.51	0.66	1, 2, 3
D	0.800	0.820	20.32	20.82	-
E	0.605	0.625	15.37	15.87	-
e	0.219 TYP		5.56 TYP		4
e <sub>1</sub>	0.438 BSC		11.12 BSC		4
J <sub>1</sub>	0.090	0.105	2.29	2.66	5
L	0.620	0.640	15.75	16.25	-
L <sub>1</sub>	0.145	0.155	3.69	3.93	1
ØP	0.138	0.144	3.51	3.65	-
Q	0.210	0.220	5.34	5.58	-
ØR	0.195	0.205	4.96	5.20	-
ØS	0.260	0.270	6.61	6.85	-

#### NOTES:

1. Lead dimension and finish uncontrolled in L<sub>1</sub>.
2. Lead dimension (without solder).
3. Add typically 0.002 inches (0.05mm) for solder coating.
4. Position of lead to be measured 0.250 inches (6.35mm) from bottom of dimension D.
5. Position of lead to be measured 0.100 inches (2.54mm) from bottom of dimension D.
6. Controlling dimension: Inch.
7. Revision 1 dated 1-93.

All Harris Semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.

*Harris Semiconductor products are sold by description only. Harris Semiconductor reserves the right to make changes in circuit design and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Harris is believed to be accurate and reliable. However, no responsibility is assumed by Harris or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Harris or its subsidiaries.*

## Sales Office Headquarters

For general information regarding Harris Semiconductor and its products, call **1-800-4-HARRIS**

**NORTH AMERICA**  
Harris Semiconductor  
P. O. Box 883, Mail Stop 53-210  
Melbourne, FL 32902  
TEL: 1-800-442-7747  
(407) 729-4984  
FAX: (407) 729-5321

**EUROPE**  
Harris Semiconductor  
Mercure Center  
100, Rue de la Fusee  
1130 Brussels, Belgium  
TEL: (32) 2.724.2111  
FAX: (32) 2.724.22.05

**ASIA**  
Harris Semiconductor PTE Ltd.  
No. 1 Tannery Road  
Cencon 1, #09-01  
Singapore 1334  
TEL: (65) 748-4200  
FAX: (65) 748-0400

