450MHz, Low Power, Video Operational Amplifier with Programmable Output Disable

The HFA1149 is a high speed, low power, current feedback amplifier built with Intersil's proprietary complementary bipolar UHF-1 process. This amplifier features a unique combination of power and performance specifically tailored for video applications.

The HFA1149 incorporates an output disable pin which is TTL/CMOS compatible, and user programmable for polarity (active high or low). This feature eliminates the inverter required between amplifiers in multiplexer configurations. The ultra-fast (12ns/20ns) disable/enable times make the HFA1149 the obvious choice for pixel switching and other high speed multiplexing applications. The HFA1149 is a high performance, pin compatible upgrade for the popular HA-5020 and HFA1145, as well as the CLC410**.**

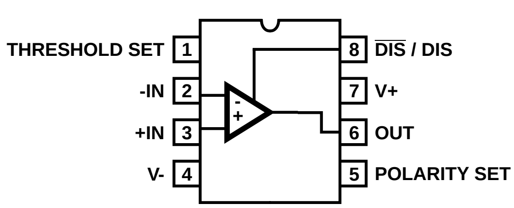
For a comparably performing op amp without an output disable, please refer to the HFA1109 data sheet.

Ordering Information

PART NUMBER (BRAND)	TEMP. RANGE (^oC)	PACKAGE	PKG. NO.
HFA1149IB (H1149)	-40 to 85	8 Ld SOIC	M8.15
HFA11XXEVAL	DIP Evaluation Board for High Speed Op Amps		

Pinout

HFA1149
(SOIC)
TOP VIEW



Features

- Wide - 3dB Bandwidth (A_V = +2) 450MHz
- Gain Flatness (To 250MHz) 0.8dB
- Very Fast Slew Rate (A_V = +2) 1100V/µs
- High Input Impedance 1.7MΩ
- Differential Gain/Phase. . . . . 0.02%/0.02 Degrees
- Low Supply Current 10mA
- Fast Output Disable/Enable 12ns/20ns

Applications

- Professional Video Processing
- Video Switchers and Routers
- Medical Imaging
- PC Multimedia Systems
- Video Pixel Switching
- Video Distribution Amplifiers
- Flash Converter Drivers
- Radar/IF Processing

HFA1149 PIN DESCRIPTIONS

PIN NAME	DESCRIPTION
Threshold Set	Optional Logic Threshold Set. Maintains disable pin TTL compatibility with asymmetrical supplies (e.g., +10V, 0V).
Polarity Set	Defines Polarity of Disable Input. High or floating selects active low disable (i.e., $\overline{DIS}$).
$\overline{DIS}$/DIS	TTL Compatible Disable Input. Output is driven to a true Hi-Z state when active. Polarity depends on state of Polarity Set Pin.

HFA1149 DISABLE FUNCTIONALITY

POLARITY SET (PIN 5)	DISABLE (PIN 8)	OUTPUT (PIN 6)
High or Float	High or Float	Enabled
High or Float	Low	Disabled
Low	High or Float	Disabled
Low	Low	Enabled

Absolute Maximum Ratings

Voltage Between V+ and V- 12V
DC Analog Input Voltage . . . . V_{SUPPLY}
Digital Input Voltage . . . . V_{SUPPLY} ±1V
Differential Input Voltage 8V
Output Current (Note 2) . . . . Short Circuit Protected
30mA Continuous
60mA ≤ 50% Duty Cycle

ESD Rating
Human Body Model (Per MIL-STD-883 Method 3015.7) . . 1000V
Charged Device Model (Per EOS/ESD DS5.3, 4/14/93) . . 1000V
Machine Model (Per EIAJ ED-4701 Method C-111). 50V

Operating Conditions

Temperature Range . . . . -40^oC to 85^oC

Thermal Information

Thermal Resistance (Typical, Note 1) θ_{JA} ($^oC/W$)
SOIC Package 160
Maximum Junction Temperature (Die) . . . . 175^oC
Maximum Junction Temperature (Plastic Package) . . . . 150^oC
Maximum Storage Temperature Range . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . 300^oC
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.
2. Output is short circuit protected to ground. Brief short circuits to ground will not degrade reliability, however, continuous (100% duty cycle) output current must not exceed 30mA for maximum reliability.

Electrical Specifications

V_{SUPPLY} = ±5V, A_V = +2, R_F = 250Ω, R_L = 100Ω, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	(NOTE 3) TEST LEVEL	TEMP. (^oC)	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS							
Input Offset Voltage		A	25	-	1	5	mV
		A	Full	-	2	8	mV
Average Input Offset Voltage Drift		B	Full	-	10	-	µV/^oC
Input Offset Voltage Common-Mode Rejection Ratio	ΔV_{CM} = ±2V	A	25	47	50	-	dB
	ΔV_{CM} = ±2V	A	Full	45	48	-	dB
Input Offset Voltage Power Supply Rejection Ratio	ΔV_{PS} = ±1.25V	A	25	50	53	-	dB
	ΔV_{PS} = ±1.25V	A	Full	47	51	-	dB
Non-Inverting Input Bias Current		A	25	-	4	10	µA
		A	Full	-	5	15	µA
Non-Inverting Input Bias Current Drift		B	Full	-	30	-	nA/^oC
Non-Inverting Input Bias Current Power Supply Sensitivity	ΔV_{PS} = ±1.25V	A	25	-	0.5	1	µA/V
	ΔV_{PS} = ±1.25V	A	Full	-	0.5	3	µA/V
Inverting Input Bias Current		A	25	-	2	10	µA
		A	Full	-	3	15	µA
Inverting Input Bias Current Drift		B	Full	-	40	-	nA/^oC
Inverting Input Bias Current Common-Mode Sensitivity	ΔV_{CM} = ±2V	A	25	-	3	6	µA/V
	ΔV_{CM} = ±2V	A	Full	-	3	8	µA/V
Inverting Input Bias Current Power Supply Sensitivity	ΔV_{PS} = ±1.25V	A	25	-	1.6	5	µA/V
	ΔV_{PS} = ±1.25V	A	Full	-	1.6	8	µA/V
Non-Inverting Input Resistance	ΔV_{CM} = ±2V	A	25, 85	0.8	1.7	-	MΩ
	ΔV_{CM} = ±2V	A	-40	0.5	1.4	-	MΩ
Inverting Input Resistance		B	25	-	60	-	Ω
Input Capacitance		B	25	-	1.6	-	pF
Input Voltage Common Mode Range (Implied by V_{IO} CMRR, $+R_{IN}$, and $-I_{BIAS}$ CMS tests)		A	Full	±2	±2.5	-	V

Electrical Specifications V_{SUPPLY} = ±5V, A_V = +2, R_F = 250Ω, R_L = 100Ω, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	(NOTE 3) TEST LEVEL	TEMP. (°C)	MIN	TYP	MAX	UNITS
Input Noise Voltage Density (Note 5)	f = 100kHz	B	25	-	4	-	nV/√Hz
Non-Inverting Input Noise Current Density (Note 5)	f = 100kHz	B	25	-	2.4	-	pA/√Hz
Inverting Input Noise Current Density (Note 5)	f = 100kHz	B	25	-	40	-	pA/√Hz
TRANSFER CHARACTERISTICS							
Open Loop Transimpedance Gain (Note 5)		B	25	-	500	-	kΩ
Minimum Stable Gain		B	Full	-	1	-	V/V
AC CHARACTERISTICS							
-3dB Bandwidth (V_{OUT} = 0.2V_{P-P}, Note 5)	A_V = -1, R_F = 200Ω	B	25	300	375	-	MHz
		B	Full	290	360	-	MHz
	A_V = +1, +R_S = 700Ω	B	25	280	330	-	MHz
		B	Full	260	320	-	MHz
	A_V = +2	B	25	390	450	-	MHz
		B	Full	350	410	-	MHz
Gain Peaking	A_V = +2, V_{OUT} = 0.2V_{P-P}	B	25	-	0	0.2	dB
		B	Full	-	0	0.5	dB
Gain Flatness (A_V = +2, V_{OUT} = 0.2V_{P-P}, Note 5)	To 125MHz	B	25	-1.0	-0.45	-	dB
		B	Full	-1.1	-0.45	-	dB
	To 200MHz	B	25	-1.6	-0.75	-	dB
		B	Full	-1.7	-0.75	-	dB
	To 250MHz	B	25	-1.9	-0.85	-	dB
		B	Full	-2.2	-0.85	-	dB
Gain Flatness A_V = +1, +R_S = 700Ω, V_{OUT} = 0.2V_{P-P} (Note 5)	To 125MHz	B	25	±0.3	±0.1	-	dB
		B	Full	±0.4	±0.1	-	dB
	To 200MHz	B	25	±0.8	±0.35	-	dB
		B	Full	±0.9	±0.35	-	dB
	To 250MHz	B	25	±1.3	±0.6	-	dB
		B	Full	±1.4	±0.6	-	dB
OUTPUT CHARACTERISTICS							
Output Voltage Swing, Unloaded (Note 5)	A_V = -1, R_L = ∞	A	25	±3	±3.2	-	V
		A	Full	±2.8	±3	-	V
Output Current (Note 5)	A_V = -1, R_L = 75Ω	A	25, 85	±33	±36	-	mA
		A	-40	±30	±33	-	mA
Output Short Circuit Current	A_V = -1	B	25	-	120	-	mA
Closed Loop Output Resistance (Note 5)	DC, A_V = +1, Enabled	B	25	-	0.05	-	Ω
Second Harmonic Distortion (V_{OUT} = 2V_{P-P}, Note 5)	20MHz	B	25	-	-55	-	dBc
	60MHz	B	25	-	-57	-	dBc
Third Harmonic Distortion (V_{OUT} = 2V_{P-P}, Note 5)	20MHz	B	25	-	-68	-	dBc
	60MHz	B	25	-	-60	-	dBc
Reverse Isolation (S_{12})	30MHz	B	25	-	-65	-	dB
TRANSIENT CHARACTERISTICS							
Rise and Fall Times	V_{OUT} = 0.5V_{P-P}	B	25	-	1.1	1.3	ns
		B	Full	-	1.1	1.4	ns

Electrical Specifications V_{SUPPLY} = ±5V, A_V = +2, R_F = 250Ω, R_L = 100Ω, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	(NOTE 3) TEST LEVEL	TEMP. (°C)	MIN	TYP	MAX	UNITS
Overshoot	V_{OUT} = 0.5V_{P-P}	B	25	-	0	2	%
		B	Full	-	0.5	5	%
Slew Rate	A_V = -1, R_F = 200Ω V_{OUT} = 5V_{P-P}	B	25	2300	2600	-	V/μs
		B	Full	2200	2500	-	V/μs
	A_V = +1, V_{OUT} = 4V_{P-P}, +R_S = 700Ω	B	25	475	550	-	V/μs
		B	Full	430	500	-	V/μs
	A_V = +2, V_{OUT} = 5V_{P-P}	B	25	940	1100	-	V/μs
		B	Full	800	950	-	V/μs
Settling Time (V_{OUT} = +2V to 0V step, Note 5)	To 0.1%	B	25	-	19	-	ns
	To 0.05%	B	25	-	23	-	ns
	To 0.01%	B	25	-	36	-	ns
Overdrive Recovery Time	V_{IN} = ±2V	B	25	-	5	-	ns
VIDEO CHARACTERISTICS							
Differential Gain (f = 3.58MHz)	R_L = 150Ω	B	25	-	0.02	0.06	%
		B	Full	-	0.03	0.09	%
	R_L = 75Ω	B	25	-	0.04	0.09	%
		B	Full	-	0.05	0.12	%
Differential Phase (f = 3.58MHz)	R_L = 150Ω	B	25	-	0.02	0.06	Degrees
		B	Full	-	0.02	0.06	Degrees
	R_L = 75Ω	B	25	-	0.05	0.09	Degrees
		B	Full	-	0.06	0.13	Degrees
POWER SUPPLY CHARACTERISTICS							
Power Supply Range		C	25	±4.5	-	±5.5	V
Power Supply Current (Note 4)		A	25	-	9.6	10	mA
		A	Full	-	10	11	mA
HFA1149 DISABLE CHARACTERISTICS Polarity Set = Floating, Threshold Set = Floating, Unless Otherwise Specified							
Disabled Supply Current	$V_{\overline{DIS}}$ = 0V	A	Full	-	2.8	3.5	mA
Digital Input Logic Low (Note 4)		A	Full	-	-	0.8	V
Digital Input Logic High (Note 4)		A	25	2.0	-	-	V
		A	Full	2.2	-	-	V
Digital Input Logic Low Current (Note 4)	$V_{DIGITAL}$ = 0V	A	Full	-	100	200	μA
Digital Input Logic High Current (Note 4)	$V_{DIGITAL}$ = 5V	A	Full	-	1	15	μA
Output Disable Time (Note 5)	V_{IN} = ±0.5V, $V_{\overline{DIS}}$ = 2.4V to 0V	B	25	-	12	-	ns
Output Enable Time (Note 5)	V_{IN} = ±0.5V, $V_{\overline{DIS}}$ = 0V to 2.4V	B	25	-	20	-	ns
Disabled Output Capacitance	$V_{\overline{DIS}}$ = 0V	B	25	-	2.5	-	pF
Disabled Output Leakage	$V_{\overline{DIS}}$ = 0V, V_{IN} = ∓2V, V_{OUT} = ±3V	A	Full	-	3	10	μA
Off Isolation ($V_{\overline{DIS}}$ = 0V, V_{IN} = 1V_{P-P}, Note 5)	At 10MHz	B	25	-	-64	-	dB
	At 30MHz	B	25	-	-54	-	dB

NOTES:

3. Test Level: A. Production tested; B. Typical or guaranteed limit based on characterization; C. Design Typical for information only.
4. Digital inputs are Polarity Set and $\overline{DIS}$ / DIS.
5. See Typical Performance Curves for more information.

Application Information

Optimum Feedback Resistor

Although a current feedback amplifier's bandwidth dependency on closed loop gain isn't as severe as that of a voltage feedback amplifier, there can be an appreciable decrease in bandwidth at higher gains. This decrease may be minimized by taking advantage of the current feedback amplifier's unique relationship between bandwidth and R_F. All current feedback amplifiers require a feedback resistor, even for unity gain applications, and R_F, in conjunction with the internal compensation capacitor, sets the dominant pole of the frequency response. Thus, the amplifier's bandwidth is inversely proportional to R_F. The HFA1149 design is optimized for a 250Ω R_F at a gain of +2. Decreasing R_F decreases stability, resulting in excessive peaking and overshoot (Note: Capacitive feedback will cause the same problems due to the feedback impedance decrease at higher frequencies). At higher gains the amplifier is more stable, so R_F can be decreased in a trade-off of stability for bandwidth.

TABLE 1. OPTIMUM FEEDBACK RESISTOR

GAIN (A_{CL})	R_F (Ω)	BANDWIDTH (MHz)
-1	200	375
+1	250 (+R_S = 700Ω)	330
+2	250	450
+5	100	160
+10	90	70

Table 1 lists recommended R_F values, and the expected bandwidth, for various closed loop gains. For a gain of +1, a resistor (+R_S) in series with +IN is required to reduce gain peaking and increase stability

Output Disable Function

The HFA1149 incorporates an output disable function that is useful for reducing power dissipation or for multiplexing signals onto a common analog bus. When disabled, the inverting input and the output become high impedances (however, the feedback network for gains other than +1 still present a load to ground from the output), the supply current reduces by 68%, and the input to output isolation becomes greater than 60dB. The amplifier is disabled by driving the $\overline{DIS}$ / DIS input to its active state.

The active state of the $\overline{DIS}$ / DIS input is user programmable via the HFA1149's Polarity Set input (see next paragraph). If the Polarity Set input is left floating, or is tied to a logic high (e.g., V+), then the disable function is activated by a logic low on the $\overline{DIS}$ / DIS input (typical of most output disable op amps). If the Polarity Set input is connected to a logic low (e.g., GND), then a logic high on the $\overline{DIS}$ / DIS input disables the amplifier.

The $\overline{DIS}$ / DIS input is TTL compatible, and unlike most competitive devices, the TTL compatibility can be maintained when the HFA1149 is operated at supplies other than ±5V (see the "Threshold Set input" section below).

An internal resistive bias network ensures that the $\overline{DIS}$ / DIS pin is pulled high if it is undriven on the PCB.

Polarity Set Input

A novel feature of the HFA1149 is the polarity programmability of the disable control pin ($\overline{DIS}$ / DIS). Depending on the state of the Polarity Set input (pin 5), the designer can define the active state to be high or low for the $\overline{DIS}$ / DIS input (see the "HFA1149 Disable Functionality" table on the front page). With this feature, a 2:1 multiplexer can be created by defining one amplifier's disable control as active low (Polarity Set = High or floating), and the other amplifier's control as active high (Polarity Set = Low). Note that if the Polarity Set pin is left floating, an internal pull-up resistor pulls the pin high, and the HFA1149 becomes a drop-in replacement for any standard ±5V supply op amp with output disable (e.g., CLC410, CLC411, CLC430, HA-5020, HFA1145, AD810). Likewise, if the disable and polarity set pins are both floated, the HFA1149 works just like a standard op amp (i.e., the output is always enabled).

Threshold Set Input for TTL Compatibility

The HFA1149 derives an internal threshold reference for the digital circuitry as long as the power supplies are nominally ±5V. This reference is used to ensure the TTL compatibility of the $\overline{DIS}$ / DIS and Polarity Set inputs. With symmetrical ±5V supplies the Threshold Set pin (Pin 1) must be floated to guarantee TTL compatibility. If asymmetrical supplies (e.g., +10V, 0V) are utilized, and TTL compatibility is desired, the Threshold Set pin must be connected to an external voltage (e.g., GND for +10V, 0V operation). The following equation should be used to determine the voltage (V_{THSET}) to be applied to the Threshold Set pin:

$$V_{THSET} = 1.58(V_{DIGTH} + 1.6V) - \frac{V-}{8} - 0.46(V+),$$

where V_{DIGTH} is the desired switching point (typically 1.4V for TTL compatibility) of the Polarity Set and $\overline{DIS}$ / DIS inputs.

Figure 1 illustrates the input impedance of the Threshold Set pin for calculating the input current at a given V_{THSET}.

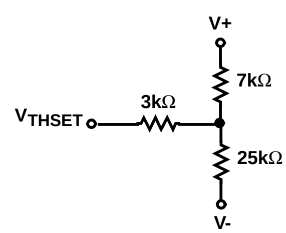


FIGURE 1. THRESHOLD SET INPUT IMPEDANCE

PC Board Layout

The frequency response of this amplifier depends greatly on the care taken in designing the PC board. **The use of low inductance components such as chip resistors and chip capacitors is strongly recommended, while a solid ground plane is a must!** Attention should be given to decoupling the power supplies. A large value (10µF) tantalum in parallel with a small value (0.1µF) chip capacitor works well in most cases.

Terminated microstrip signal lines are recommended at the input and output of the device. Capacitance directly on the output must be minimized, or isolated as discussed in the next section.

Care must also be taken to minimize the capacitance to ground seen by the amplifier's inverting input (-IN). The larger this capacitance, the worse the gain peaking, resulting in pulse overshoot and possible instability. Thus, it is recommended that the ground plane be removed under traces connected to -IN, and connections to -IN should be kept as short as possible.

Driving Capacitive Loads

Capacitive loads, such as an A/D input, or an improperly terminated transmission line will degrade the amplifier's phase margin resulting in frequency response peaking and possible oscillations. In most cases, the oscillation can be avoided by placing a resistor (R_S) in series with the output prior to the capacitance.

R_S and C_L form a low pass network at the output, thus limiting system bandwidth well below the amplifier bandwidth. By decreasing R_S as C_L increases, the maximum bandwidth is obtained without sacrificing stability. In spite of this, bandwidth still decreases as the load capacitance increases.

Evaluation Board

The performance of the HFA1149 may be evaluated using the HFA11XX Evaluation Board (part number HFA11XXEVAL). Please contact your local sales office for information. When evaluating this amplifier, the two 510Ω gain setting resistors on the evaluation board should be changed to 250Ω.

The layout and schematic of the board are shown in Figure 2.

NOTE: The SOIC version may be evaluated in the DIP board by using a SOIC-to-DIP adapter such as Aries Electronics Part Number 08-350000-10.

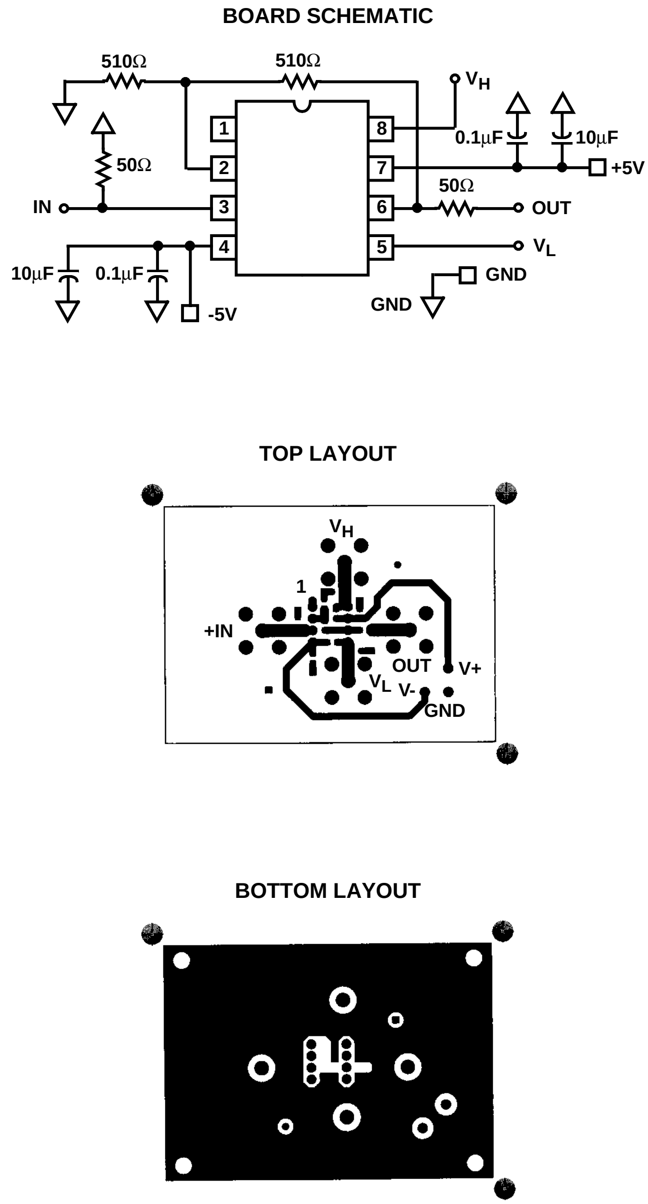


FIGURE 2. EVALUATION BOARD SCHEMATIC AND LAYOUT

Typical Performance Curves

V_{SUPPLY} = ±5V, T_A = 25^{o}C, R_F = Value From the Optimum Feedback Resistor Table, R_L = 100Ω, Unless Otherwise Specified

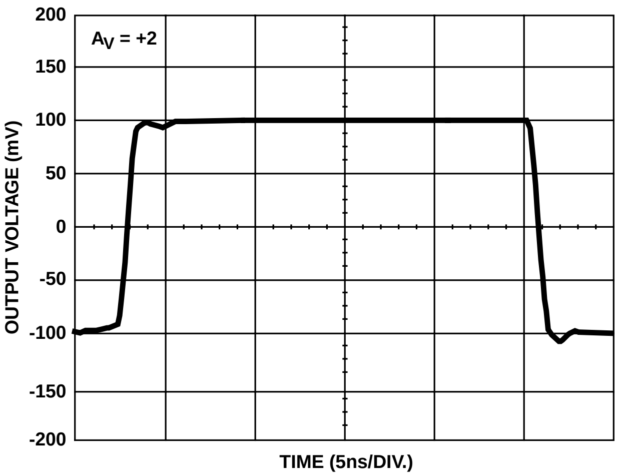


FIGURE 3. SMALL SIGNAL PULSE RESPONSE

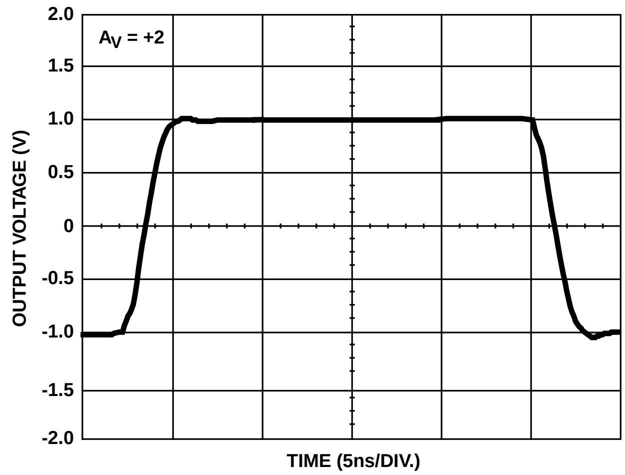


FIGURE 4. LARGE SIGNAL PULSE RESPONSE

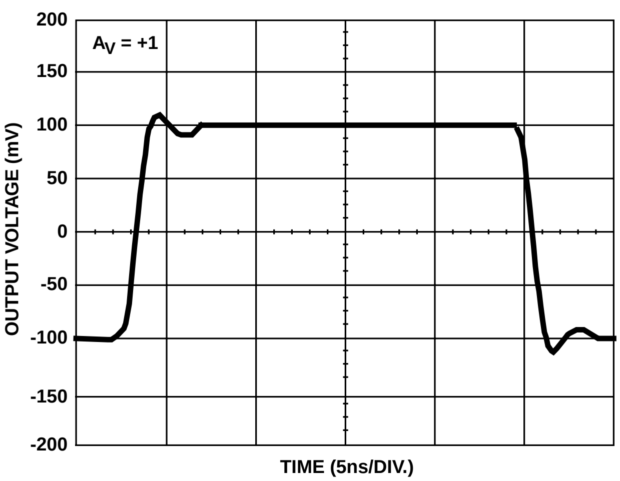


FIGURE 5. SMALL SIGNAL PULSE RESPONSE

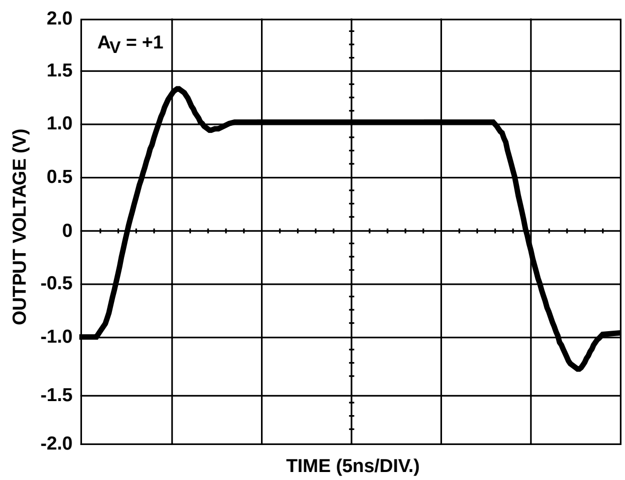


FIGURE 6. LARGE SIGNAL PULSE RESPONSE

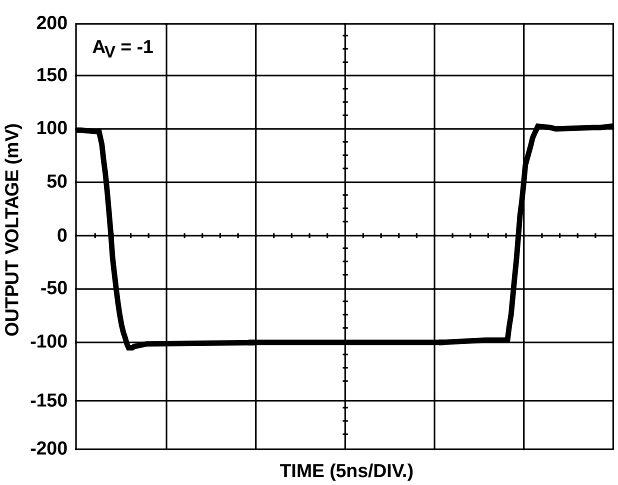


FIGURE 7. SMALL SIGNAL PULSE RESPONSE

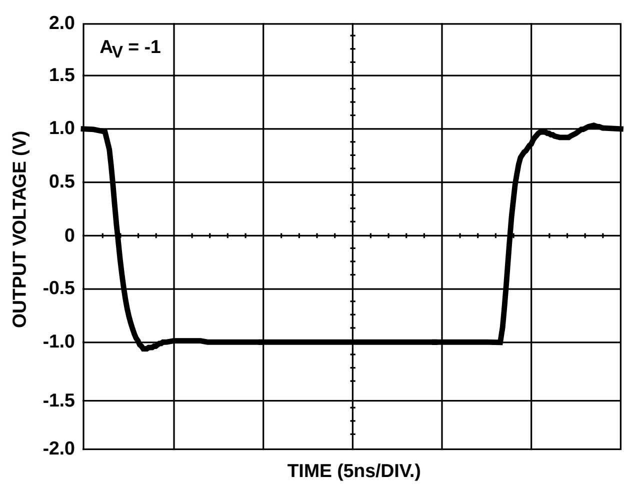


FIGURE 8. LARGE SIGNAL PULSE RESPONSE

Typical Performance Curves

V_{SUPPLY} = ±5V, T_A = 25°C, R_F = Value From the Optimum Feedback Resistor Table, R_L = 100Ω, Unless Otherwise Specified **(Continued)**

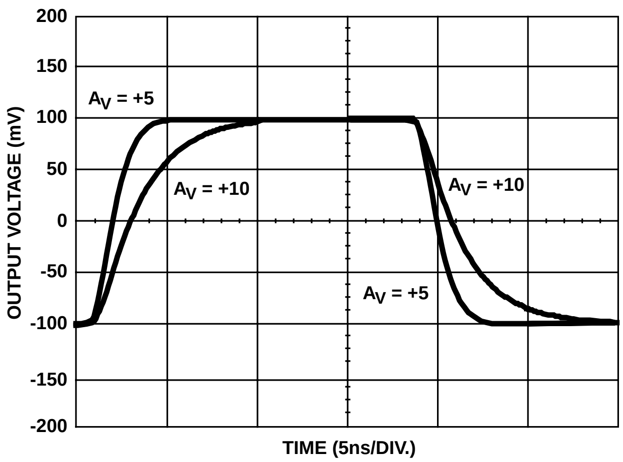


FIGURE 9. SMALL SIGNAL PULSE RESPONSE

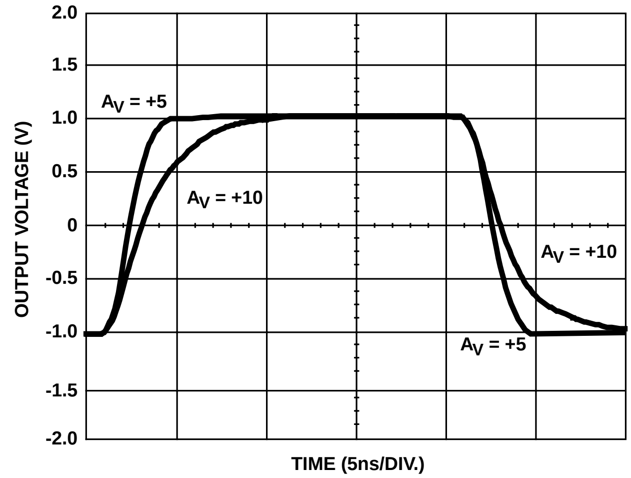


FIGURE 10. LARGE SIGNAL PULSE RESPONSE

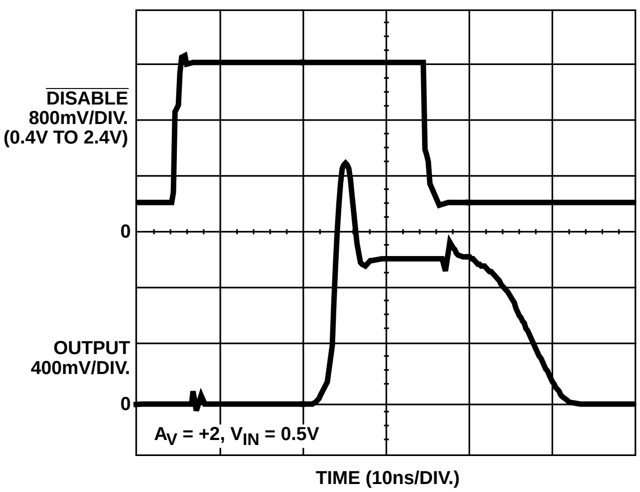


FIGURE 11. OUTPUT ENABLE AND DISABLE RESPONSE

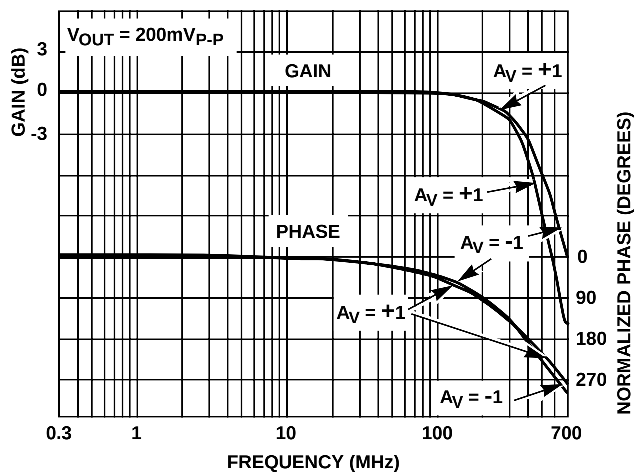


FIGURE 12. FREQUENCY RESPONSE

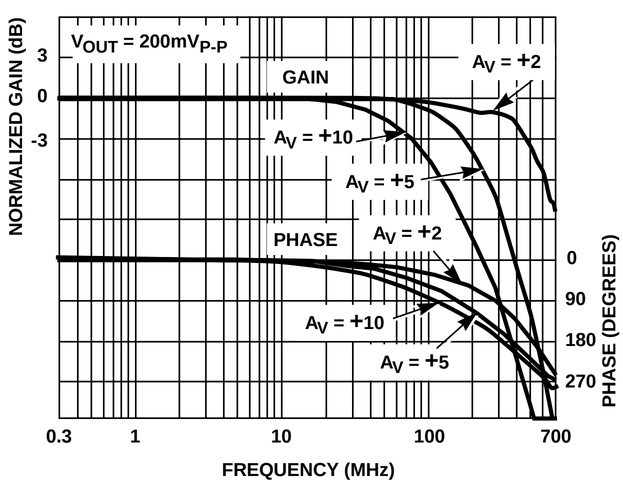


FIGURE 13. FREQUENCY RESPONSE

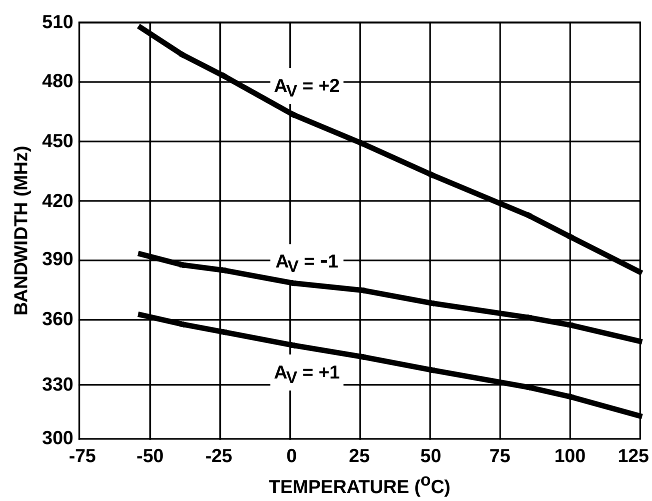


FIGURE 14. -3dB BANDWIDTH vs TEMPERATURE

Typical Performance Curves

V_{SUPPLY} = ±5V, T_A = 25°C, R_F = Value From the Optimum Feedback Resistor Table, R_L = 100Ω, Unless Otherwise Specified **(Continued)**

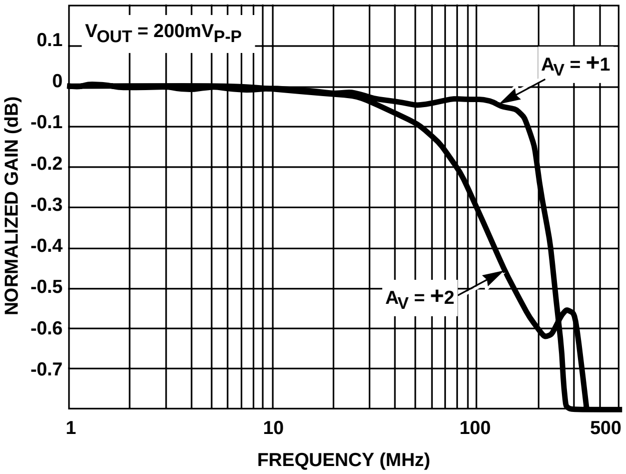


FIGURE 15. GAIN FLATNESS

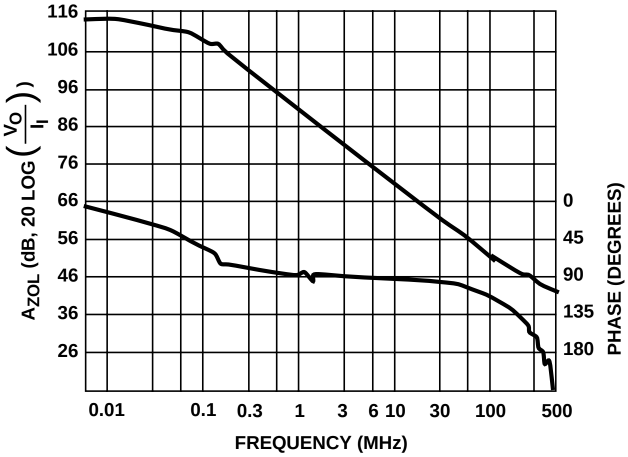


FIGURE 16. OPEN LOOP TRANSIMPEDANCE

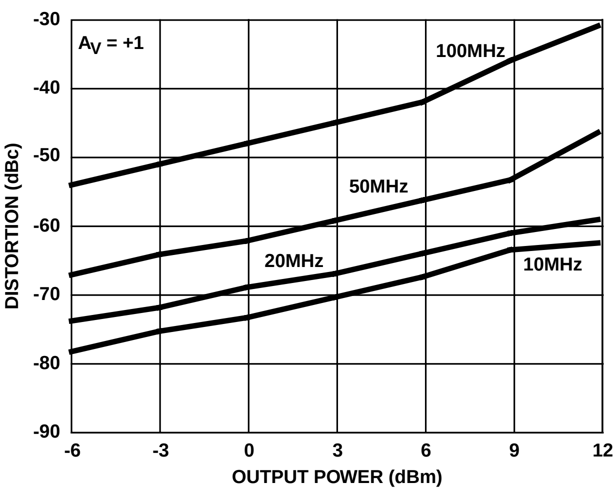


FIGURE 17. 2nd HARMONIC DISTORTION vs P_{OUT}

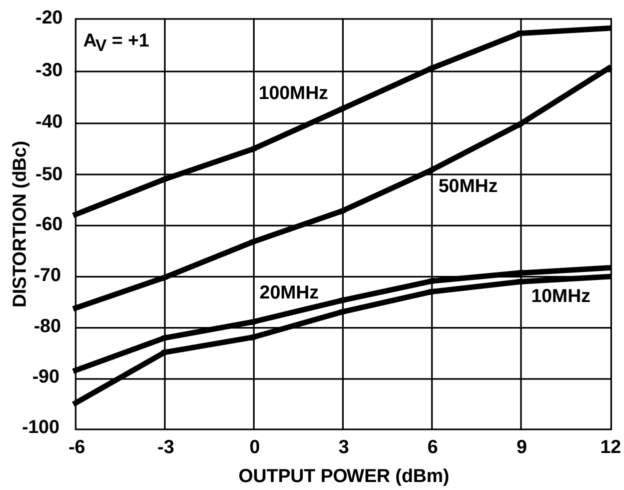


FIGURE 18. 3rd HARMONIC DISTORTION vs P_{OUT}

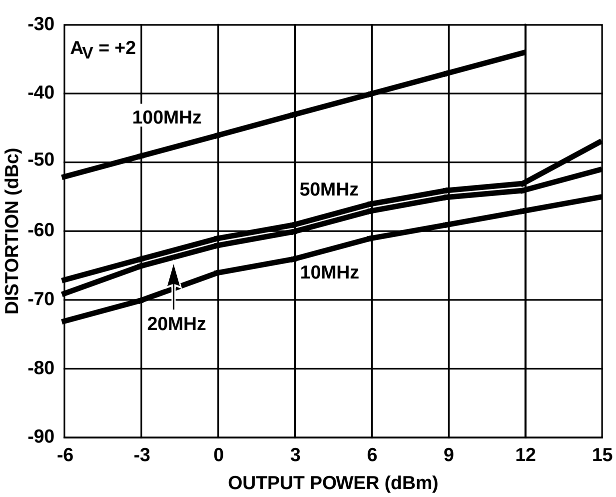


FIGURE 19. 2nd HARMONIC DISTORTION vs P_{OUT}

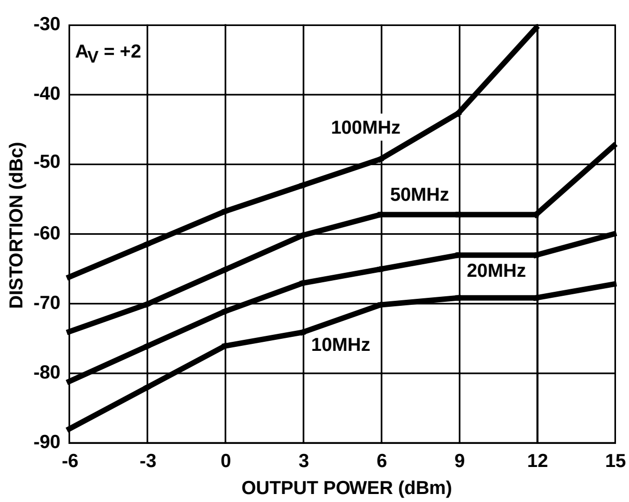


FIGURE 20. 3rd HARMONIC DISTORTION vs P_{OUT}

Typical Performance Curves

V_{SUPPLY} = ±5V, T_A = 25°C, R_F = Value From the Optimum Feedback Resistor Table, R_L = 100Ω, Unless Otherwise Specified **(Continued)**

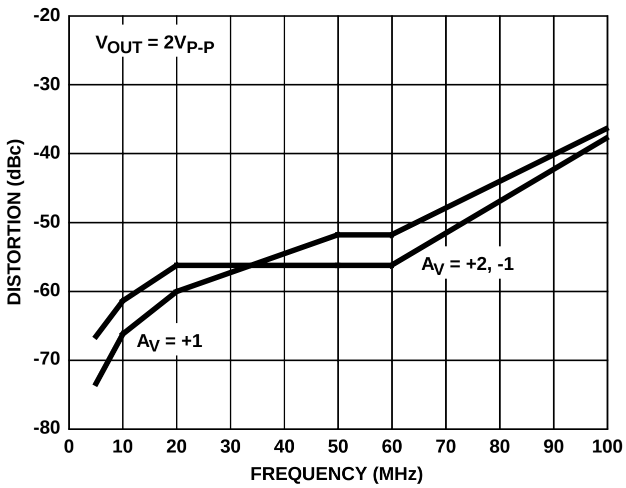


FIGURE 21. 2nd HARMONIC DISTORTION vs FREQUENCY

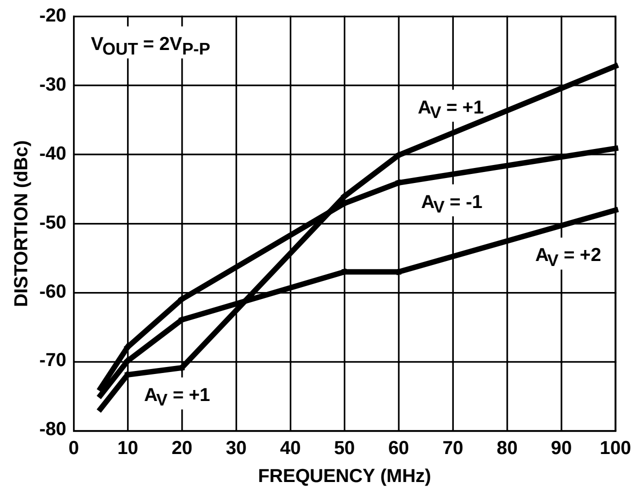


FIGURE 22. 3rd HARMONIC DISTORTION vs FREQUENCY

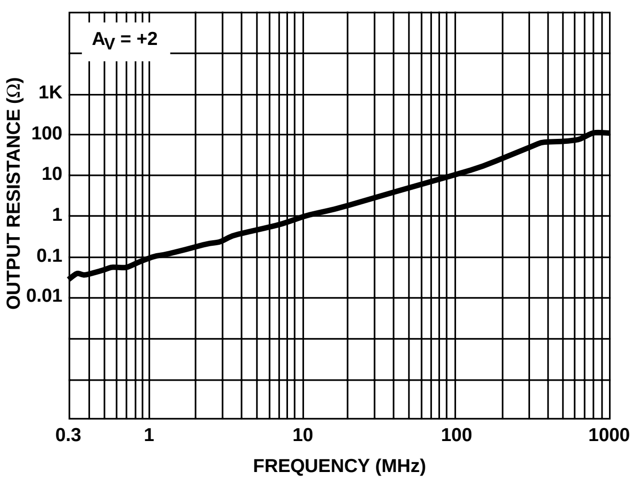


FIGURE 23. CLOSED LOOP OUTPUT RESISTANCE

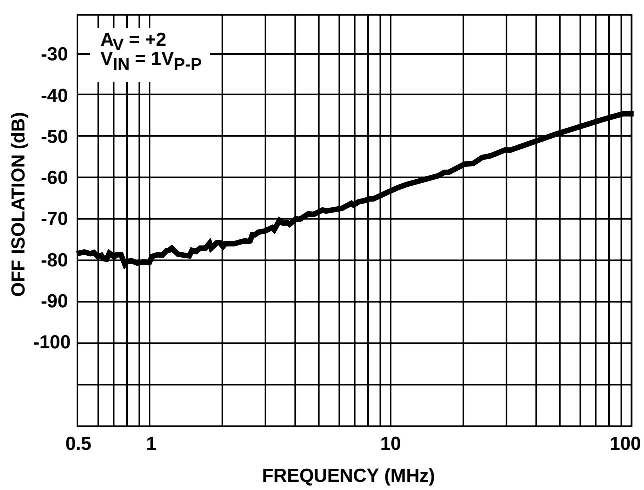


FIGURE 24. OFF ISOLATION

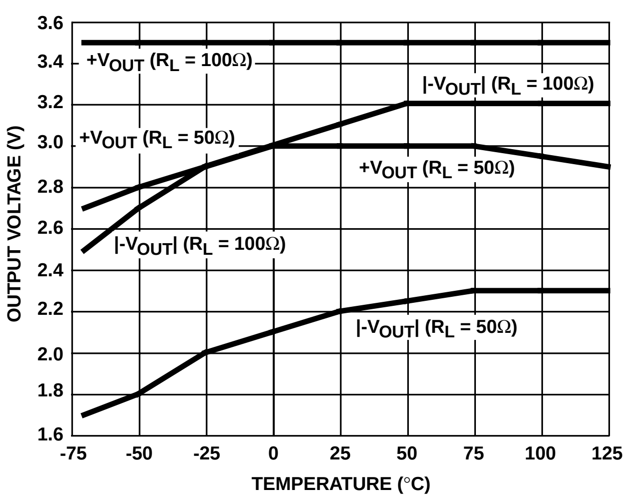


FIGURE 25. OUTPUT VOLTAGE vs TEMPERATURE

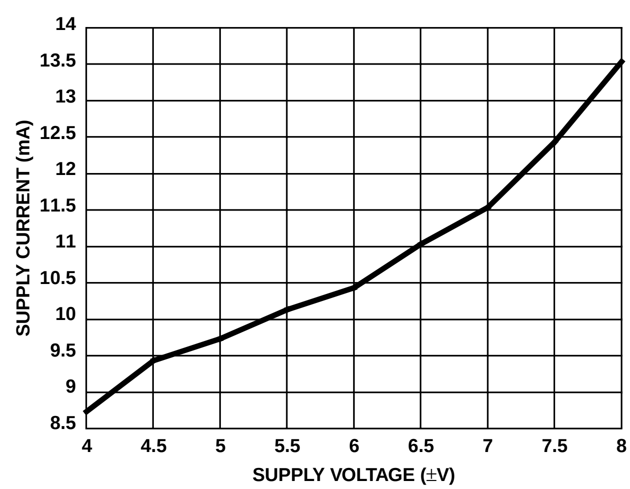


FIGURE 26. SUPPLY CURRENT vs SUPPLY VOLTAGE

Typical Performance Curves

V_{SUPPLY} = ±5V, T_A = 25°C, R_F = Value From the Optimum Feedback Resistor Table, R_L = 100Ω, Unless Otherwise Specified **(Continued)**

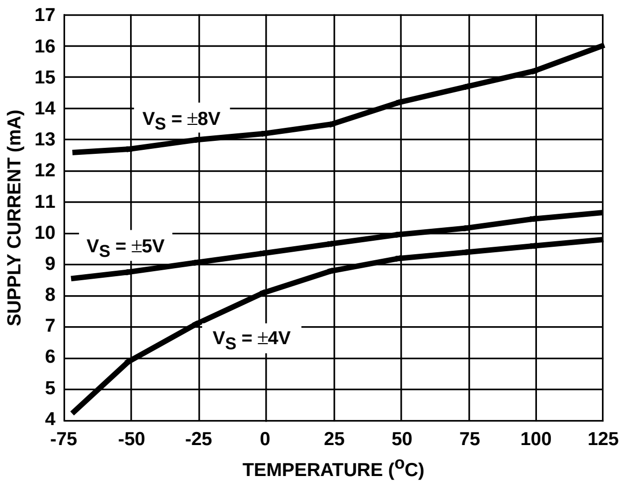


FIGURE 27. SUPPLY CURRENT vs TEMPERATURE

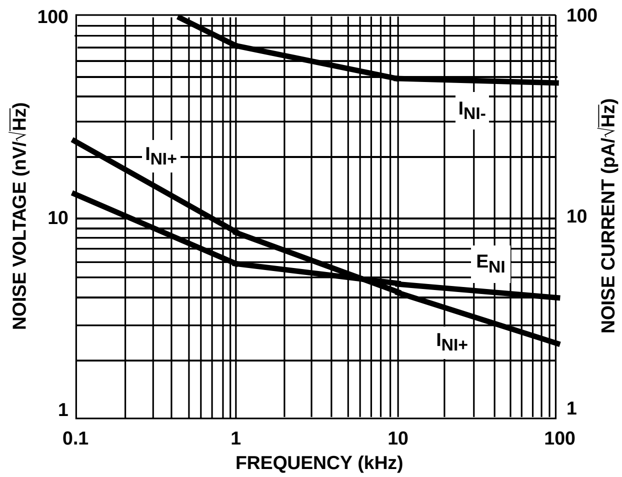


FIGURE 28. INPUT NOISE CHARACTERISTICS

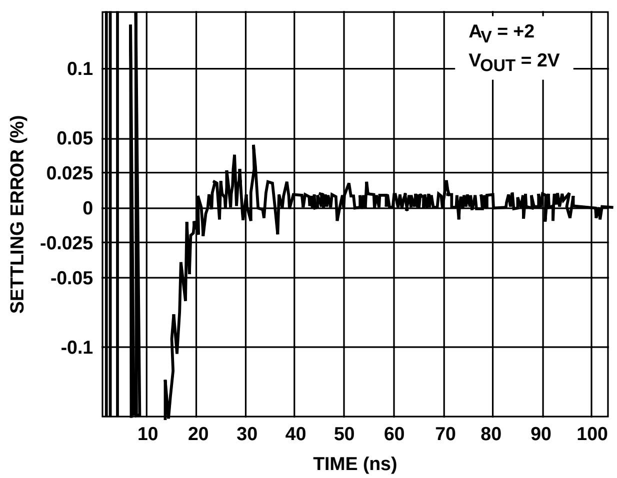


FIGURE 29. SETTLING RESPONSE

Die Characteristics

DIE DIMENSIONS

59 mils x 80 mils x 19 mils
1500µm x 2020µm x 483µm

METALLIZATION

Type: Metal 1: AlCu(2%)/TiW
Type: Metal 2: AlCu(2%)
Thickness: Metal 1: 8kÅ ±0.4kÅ
Thickness: Metal 2: 16kÅ ±0.8kÅ

GLASSIVATION

Type: Nitride
Thickness: 4kÅ ±0.5kÅ

TRANSISTOR COUNT

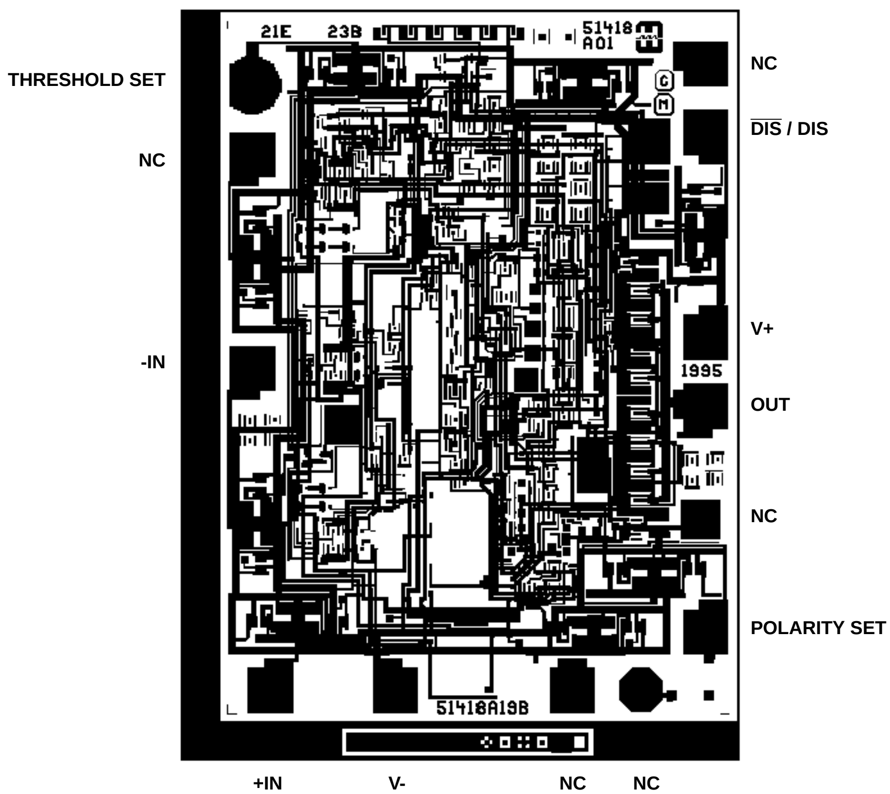
130

SUBSTRATE POTENTIAL (POWERED UP)

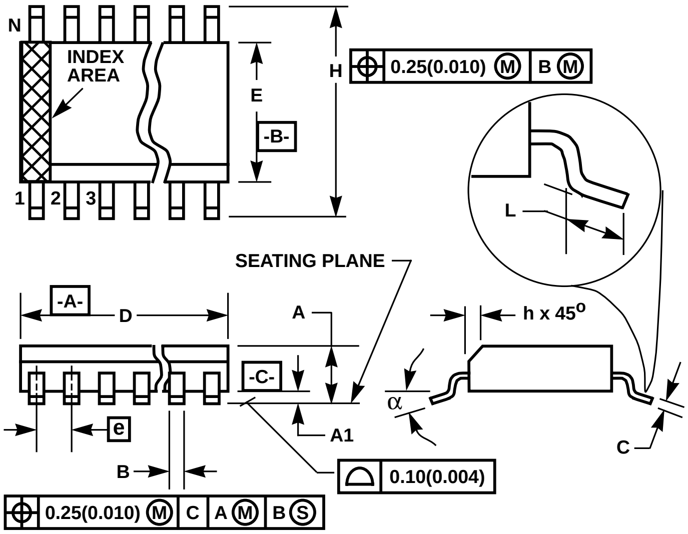
Floating (Recommend Connection to V-)

Metallization Mask Layout

HFA1149



Small Outline Plastic Packages (SOIC)



M8.15 (JEDEC MS-012-AA ISSUE C)
8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.1890	0.1968	4.80	5.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	8		8		7
α	0°	8°	0°	8°	-

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NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

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