
HA13532NT

Three-Phase Stepping Motor Control IC

HITACHI

ADE-207-121A (Z)
2nd Edition
July 1996

Description

The HA13532NT is an IC for control a three-phase stepping motor.

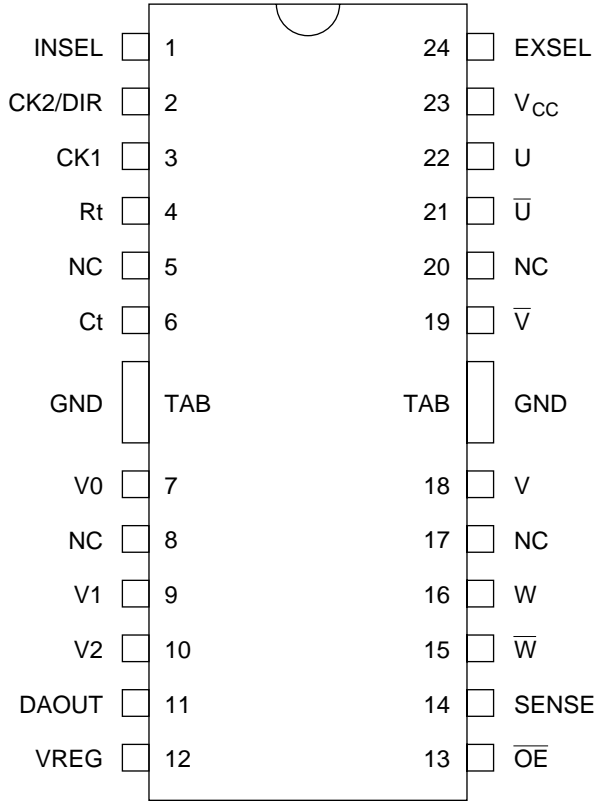
Functions

- PWM current control
- Low-voltage inhibit (LVI)
- Three-bit D/A converter for current programming
- Motor on/off
- Selectable 2-phase or 2-3-phase exciting

Features

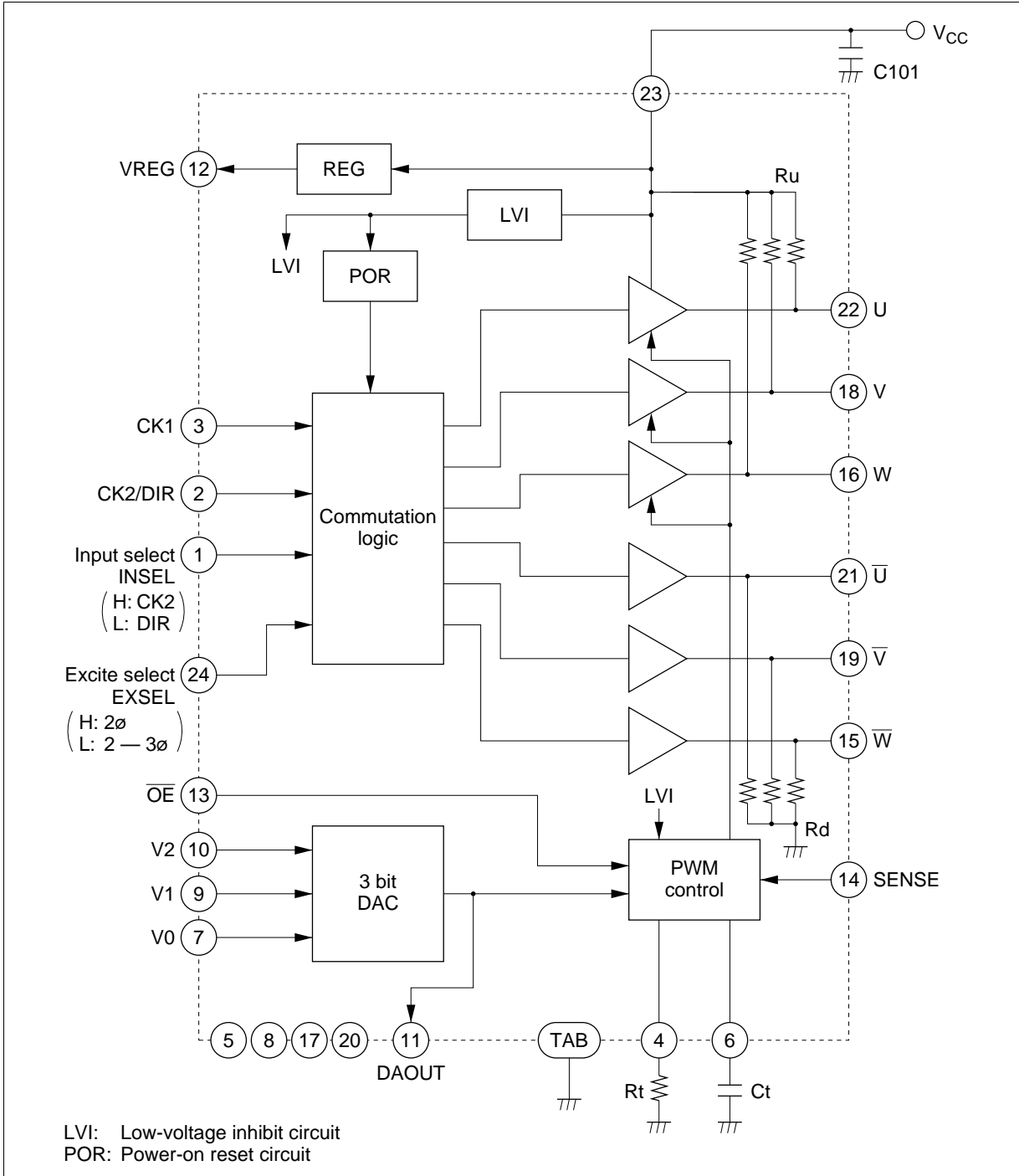
- Wide operating voltage range
- Few external components

Pin Arrangement



(Top view)

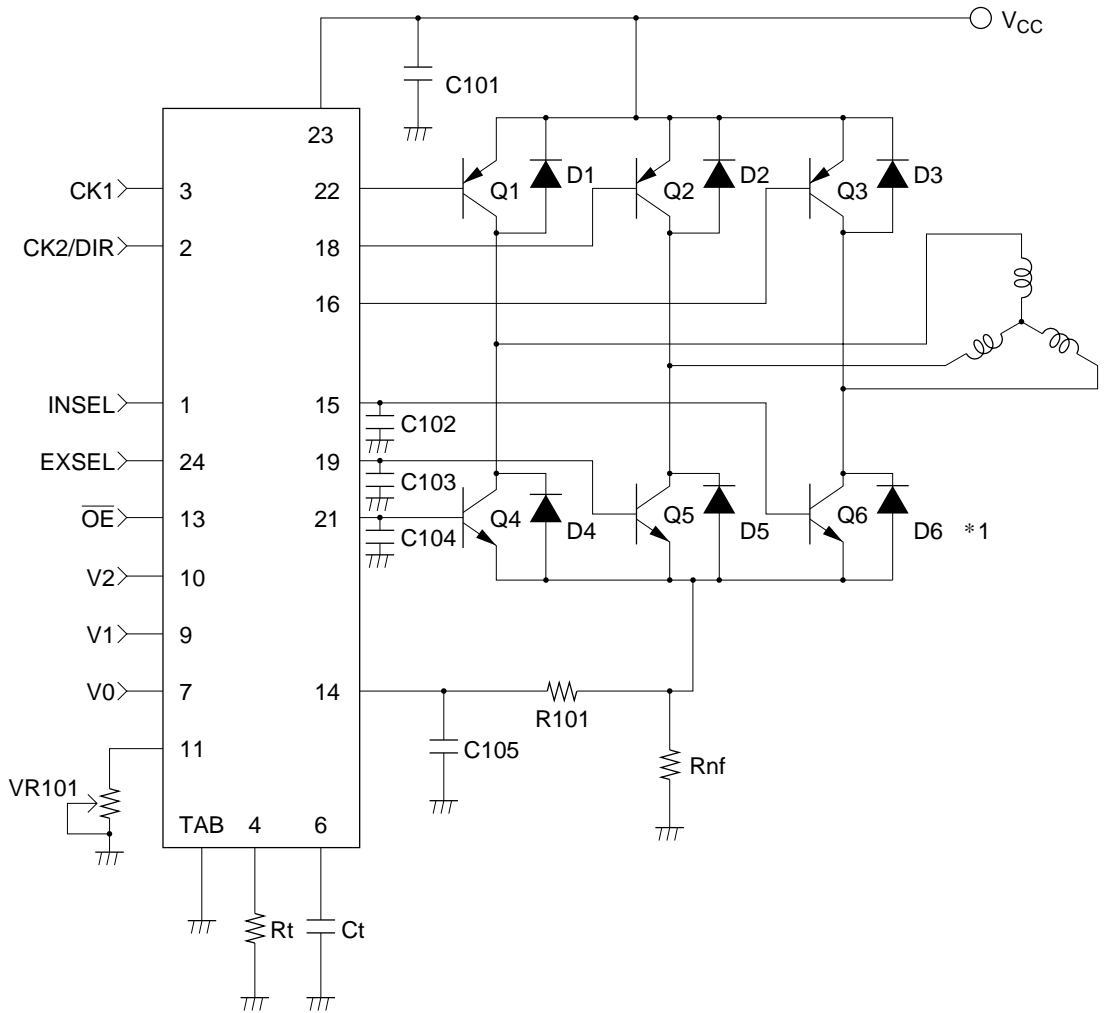
Block Diagram



Pin Description

Pin No.	Pin Name	Function	Pin Voltage
1	INSEL	Selects pin 2 input: CK2 if high; DIR if low (see timing diagrams)	$V_{TH} = 2.5 \text{ V typ}$
2	CK2/DIR	CK2 or DIR input (see timing diagrams)	$V_{TH} = 2.5 \text{ V typ}$
3	CK1	CK1 input (see timing diagrams)	$V_{TH} = 2.5 \text{ V typ}$
4	Rt	Reference value for 3-phase output current and Ct charge/discharge current	4.8 V typ
5	NC	No connection	
6	Ct	Time constant for PWM carrier frequency	
7	V0	Voltage programming input to DAC (LSB)	$V_{TH} = 2.5 \text{ V typ}$
8	NC	No connection	
9	V1	Voltage programming input to DAC	$V_{TH} = 2.5 \text{ V typ}$
10	V2	Voltage programming input to DAC (MSB)	$V_{TH} = 2.5 \text{ V typ}$
11	DAOUT	DAC output	
12	VREG	Regulated output	4.8 V typ (@I = 2 mA)
13	\overline{OE}	Output enable: low enables PWM output phases U, V, and W; high gives high impedance	$V_{TH} = 2.5 \text{ V typ}$
14	SENSE	Current feedback	0 V min, 5.0 V max
15	\overline{W}	Phase-W lower-arm output	
16	W	Phase-W upper-arm output	
17	NC	No connection	
18	V	Phase-V upper-arm output	
19	\overline{V}	Phase-U lower-arm output	
20	\overline{NC}	No connection	
21	\overline{U}	Phase-U lower-arm output	
22	U	Phase-U upper-arm output	
23	V _{cc}	Power supply	10 V min, 27.6 V max
24	EXSEL	Selects exciting mode: 2-phase if high; 2-3-phase if low (see timing diagrams)	$V_{TH} = 2.5 \text{ V typ}$

Application Circuit



Notes: 1. Use high-speed diodes for D4, D5, and D6.

External Components

Symbol	Recommended Value	Purpose	Notes
R _{nf}	0.11 Ω ≤ R _{nf} ≤ 0.33 Ω	Current sensing	1
R _t	51 k Ω	Reference current programming	2
C _t	1000 pF	Time constant for PWM carrier frequency	3
C ₁₀₁	≥ 0.1 μF	Power supply decoupling	
C ₁₀₂ , C ₁₀₃ , C ₁₀₄	0.01 μF	Penetration current control	4
C ₁₀₅	1000 pF	Current sensing filter	
R ₁₀₁	750 Ω		
VR ₁₀₁	100 kΩ	Motor current little adjustment	

Notes: 1. The maximum motor drive current is:

$$I_{max} \approx \pm \frac{V_{dac} + V_{offs}}{R_{nf}} \quad (1)$$

where, V_{dac}: DAC output voltage (see electrical characteristics)

V_{offs}: Offset voltage (see electrical characteristics)

2. The output sink current I_{osnk}, output source current I_{osrc}, and C_t charge/discharge currents I_{ct+} and I_{ct-} are calculated as follows:

where, set R_t to be 2.5kΩ or higher.

$$I_{osnk} \approx \frac{50V_{rt}}{R_t} - \frac{V_{be}}{R_u} \quad (2)$$

$$I_{osrc} \approx \frac{50V_{rt}}{R_t} - \frac{V_{be}}{R_d} \quad (3)$$

$$I_{ct+}, I_{ct-} \approx \frac{V_{rt}}{R_t} \quad (4)$$

where, V_{rt}: R_t voltage (see electrical characteristics)

R_u: pull-up resistance (see electrical characteristics)

R_d: pull-down resistance (see electrical characteristics)

V_{be}: base-emitter voltage of driven transistor

3. The PWM carrier frequency f_c is calculated as follows:

$$f_c \approx \frac{I_{ct}}{2C_t (V_{cth} - V_{ctl})} \quad (5)$$

$$\approx \frac{V_{rt}}{2C_t R_t (V_{cth} - V_{ctl})} \quad (6)$$

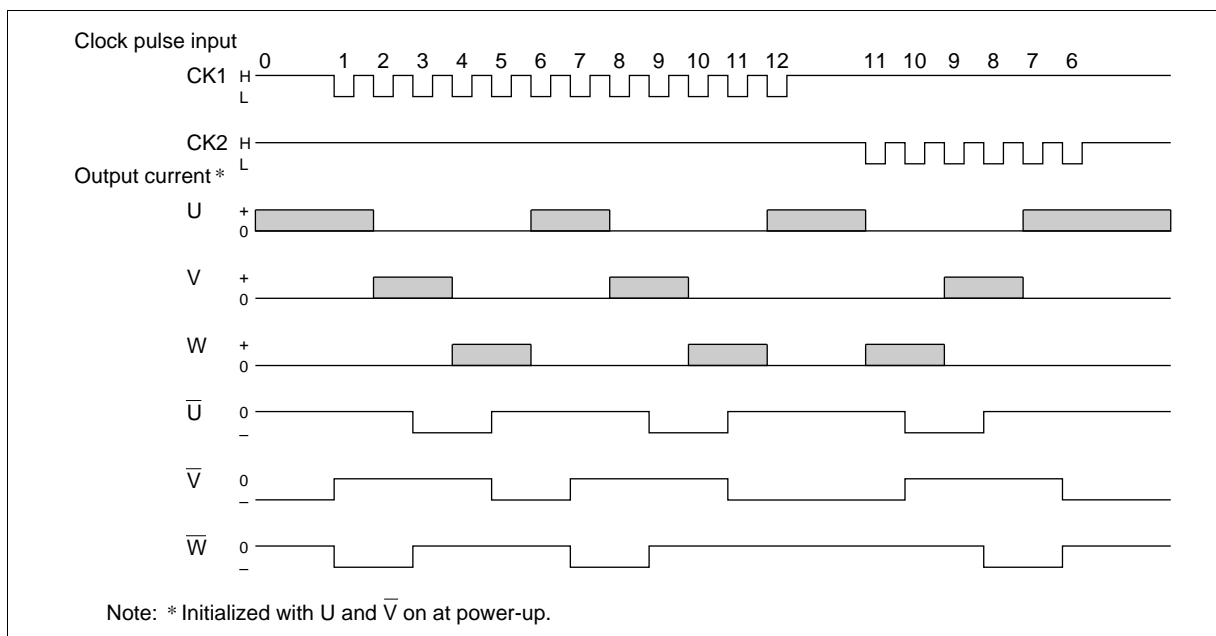
where, V_{cth}: C_t high voltage (see electrical characteristics)

V_{ctl}: C_t low voltage (see electrical characteristics)

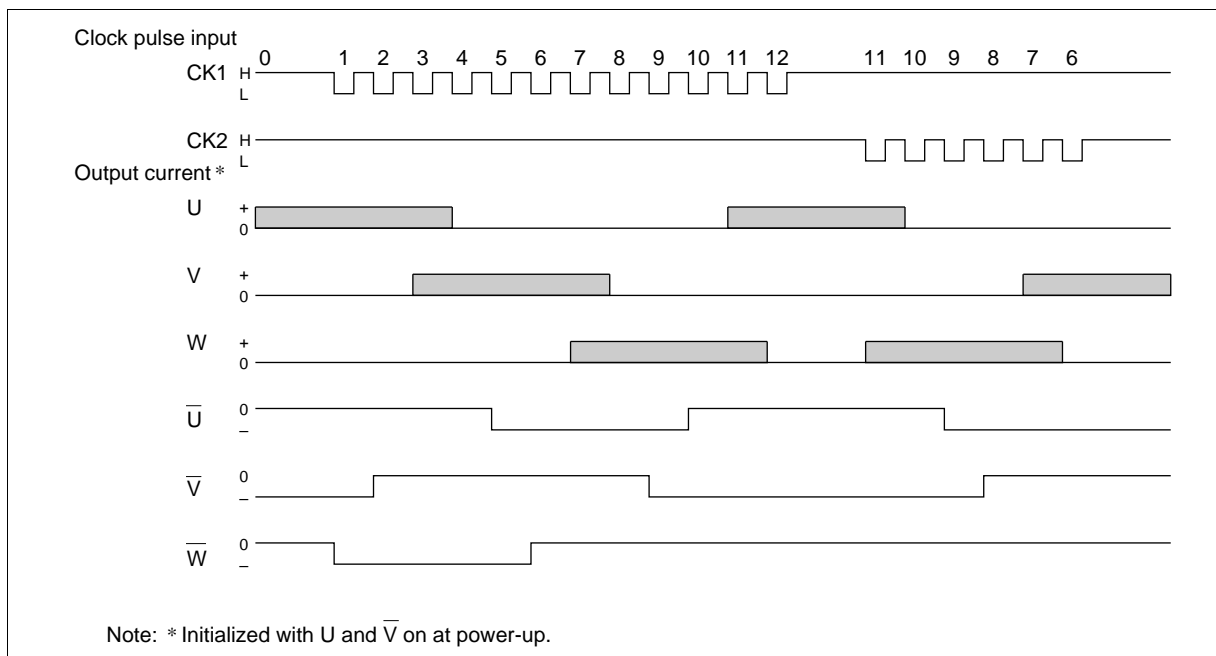
4. Values of C₁₀₂, C₁₀₃, C₁₀₄, C₁₀₅, R₁₀₁ are different from using power transistor

Timing Waveforms

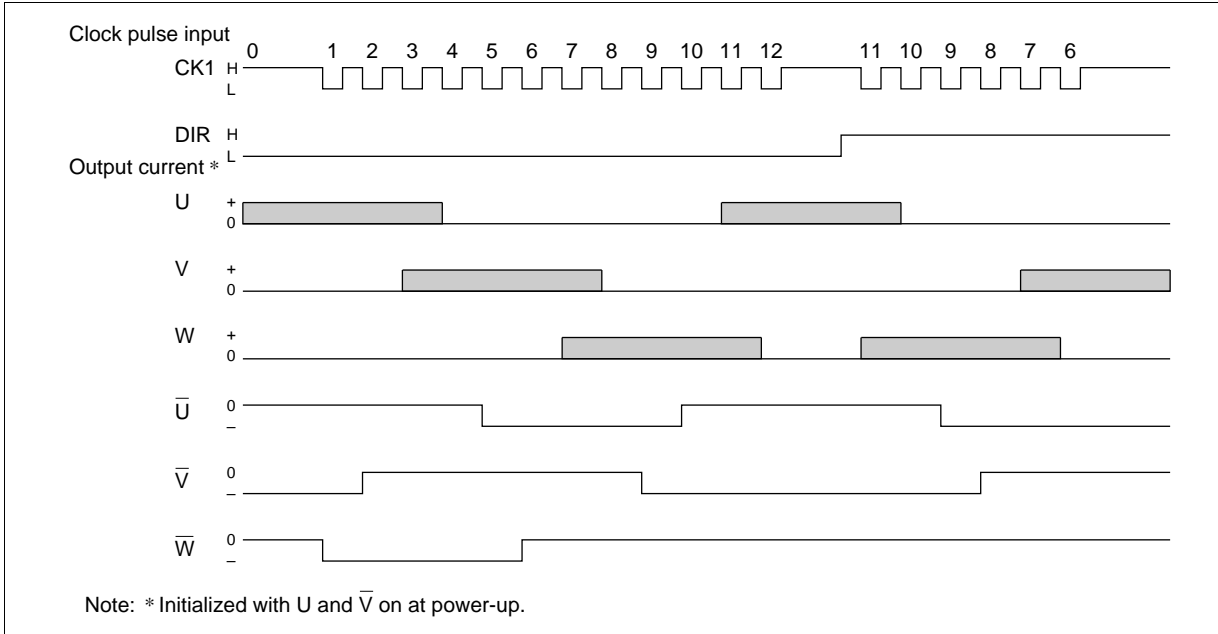
Two Clock Pulse Inputs, Two-Phase Exciting (INSEL High, EXSEL High)



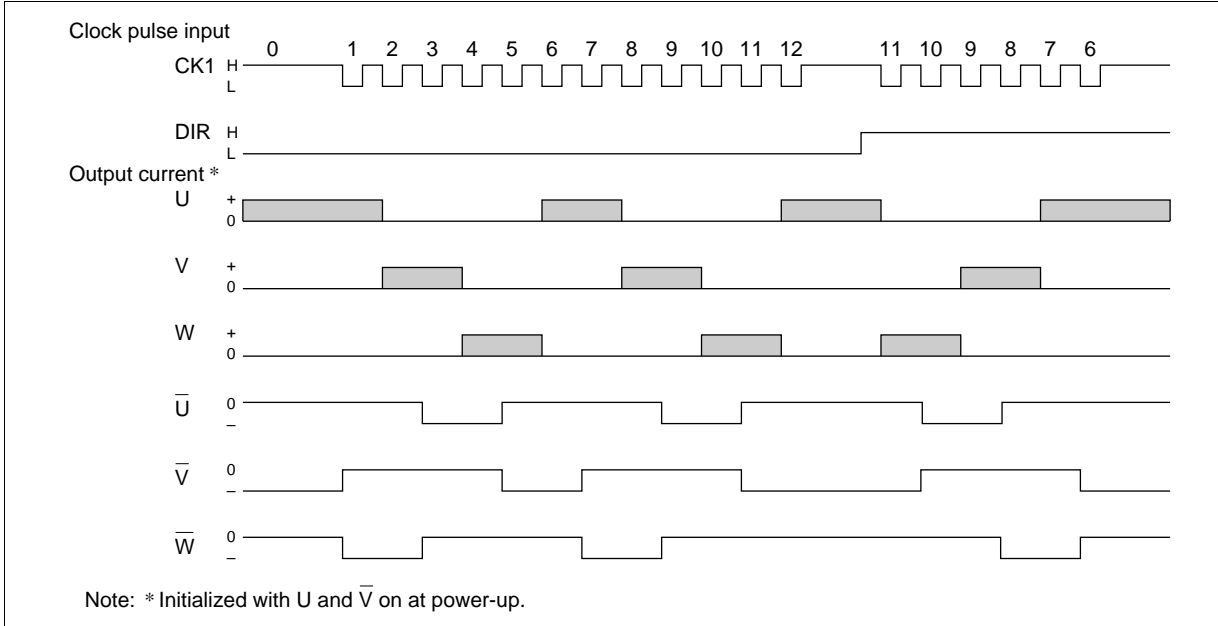
Two Clock Pulse Inputs, Two-Three-Phase Exciting (INSEL High, EXSEL Low)



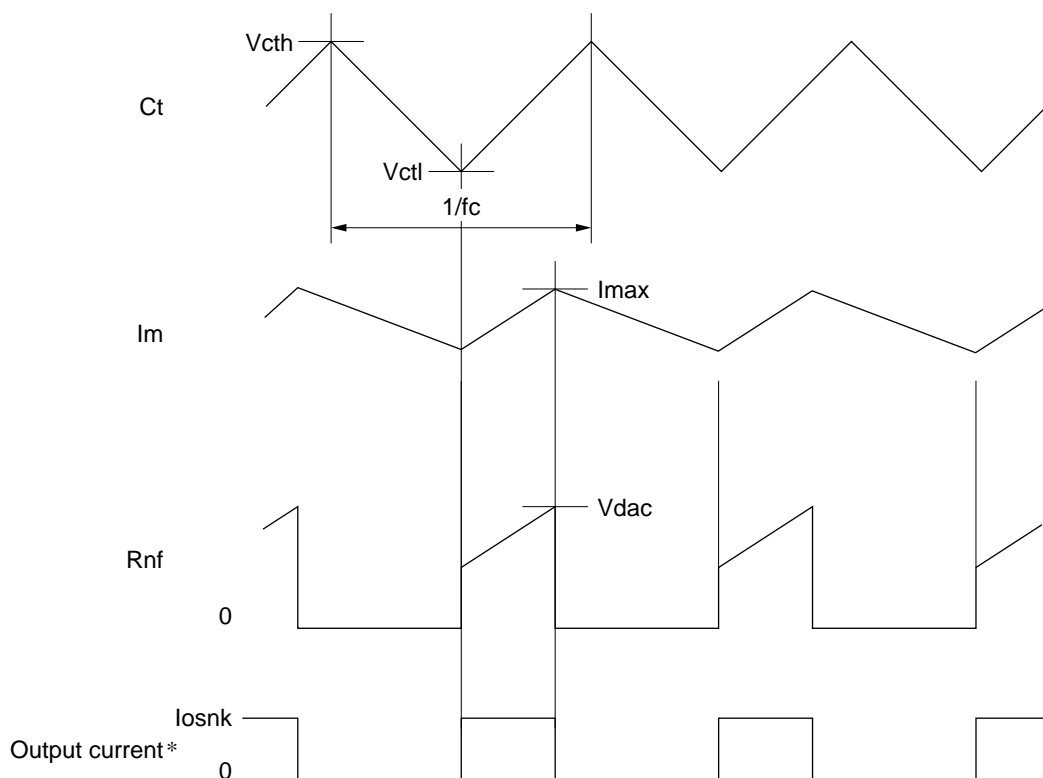
One Clock Pulse Input, Two-Three-Phase Exciting (INSEL Low, EXSEL Low)



One Clock Pulse Input, Two-Phase Exciting (INSEL Low, EXSEL High)



PWM Control



Note: * Only phase U is shown.

Absolute Maximum Ratings

Item	Symbol	Rating	Unit	Notes
Power supply voltage	V_{cc}	30	V	1
Input voltage	V_{in}	7	V	2
Power dissipation	P_T	910	mW	3
Operating temperature	T_{opr}	-10 to +70	°C	
Storage temperature	T_{stg}	-55 to +125	°C	
Output current	I_{reg}	2	mA	

Notes: 1. The operating power supply voltage range is $V_{cc} = 10\text{ V to }27.6\text{ V}$.

2. Applies to logic and DAC input pins.

3. Permitted at $T_a = 70^\circ\text{C}$, if thermal resistance is as below:

$\theta_{j-a} \leq 60^\circ\text{C/W}$ (glass-epoxy board)

Electrical Characteristics (Ta = 25°C, V_{CC} = 24 V)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions	Pins	Notes
Current consumption	I _{CCO}	—	—	33	mA	V _{CC} = 30 V, \overline{OE} = H	23	1
	I _{CC}	—	—	41	mA	V _{CC} = 30 V, \overline{OE} = L		
REG	Output voltage	V _{reg}	4.4	4.8	5.2	V	I _{reg} = 2 mA	12
	Load regulation	ΔV _{reg}	—	—	±0.1	V	I _{reg} = 0 mA to 2 mA	
Logic	Input current	I _{in}	-10	—	1	μA	V _{in} = 0 V to 7 V	1, 2, 3, 13, 24
			-1	—	10	μA		7, 9, 10
	Low voltage level	V _{il}	—	—	1.35	V		1, 2, 3, 7, 9, 10, 13,
	High voltage level	V _{ih}	3.65	—	—	V		24
DAC	Outout voltage	V _{dac}	200	230	260	mV	(V ₂ , V ₁ , V ₀) = (H, L, L)	11
			116	146	176	mV	(V ₂ , V ₁ , V ₀) = (L, H, L)	
			75	105	135	mV	(V ₂ , V ₁ , V ₀) = (L, L, H)	
			33	63	93	mV	(V ₂ , V ₁ , V ₀) = (L, L, L)	
PWM control	Input current	I _{sens}	—	—	±2	μA	V _{sens} = 0 V to 5 V	14
	Offset voltage	V _{offs}	—	—	±10	mV		2
	R _t voltage	V _{rt}	4.4	4.8	5.2	V	R _t = 51 kΩ	4
	C _t change current	I _{ct+}	84	94	104	μA	R _t = 51 kΩ, V _{ct} 6 = 3.75 V	
	C _t discharge current	I _{ct-}	84	94	104	μA	R _t = 51 kΩ, V _{ct} = 3.75 V	

Electrical Characteristics (Ta = 25°C, V_{CC} = 24 V) (Cont)

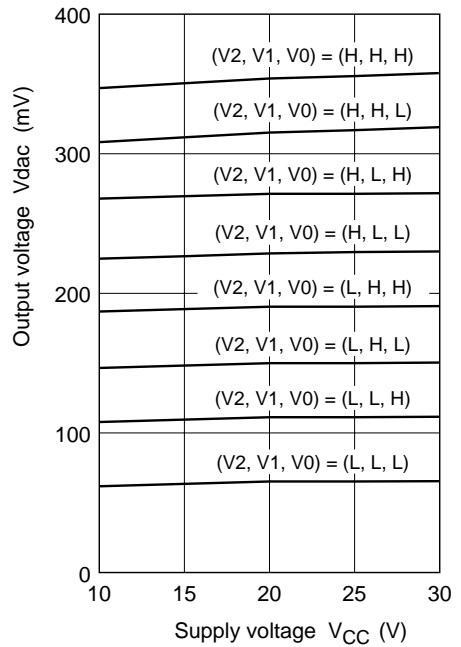
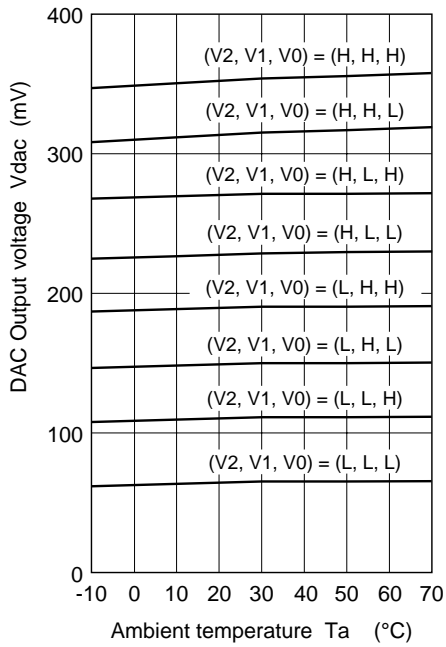
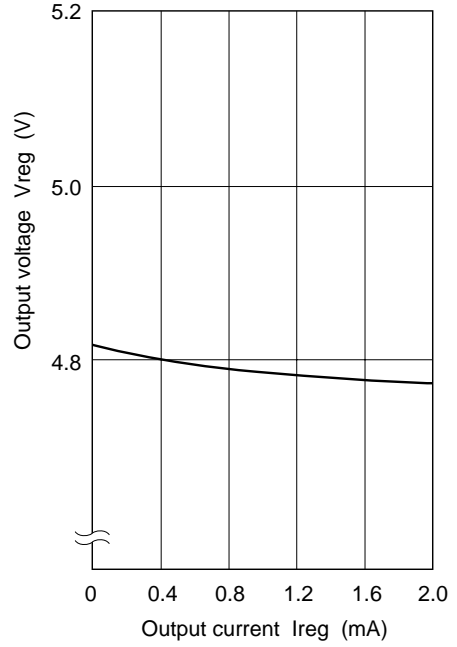
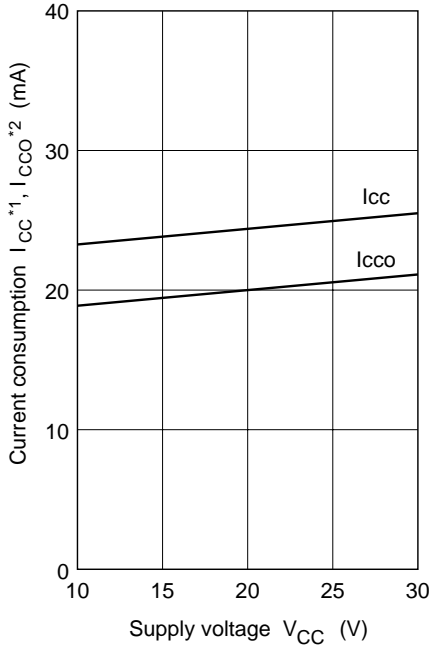
Item	Symbol	Min	Typ	Max	Unit	Test Conditions	Pins	Notes	
PWM control	Ct high voltage	Vcth	4.3	4.8	5.3	V		6	3
	Ct low voltage	Vctl	2.3	2.78	3.3	V			
	Carrier frequency	fc	18.6	23.3	28.0	kHz	Rt = 51 kΩ, Ct = 1000 pF		
3-pahse output	Output sink current	losnk	2.0	3.1	4.2	mA	V _O = V _{CC} - 1.5 V, Rt = 51 kΩ	16, 18, 22	
	Output source current	losrc	2.0	3.1	4.2	mA	V _O = 1.5 V, Rt = 51 kΩ	15, 19, 21	
	Output leakage current	loff	—	—	±10	μA	V _{CC} = 30 V, V _O = V _{CC}	16, 18, 22	
			—	—	±10	μA	V _{CC} = 30 V, V _O = 0 V	15, 19, 21	
	Pull-up resistance	Ru	700	950	1200	Ω		16, 18, 22	
	Pull-down resistance	Rd	700	950	1200	Ω		15, 19, 21	
	Transient response time	t _{phl}	—	—	6.0	μs		15, 16, 18, 19, 21, 22	
—			—	6.0	μs				
LVI	Operating voltage	Vlvi	8.0	—	10	V		23	
	Hysteresis	Vhys	—	0.3	—	V			

Notes: 1. Measured with pins 12, 15, 16, 18, 19, 21, and 22 open.

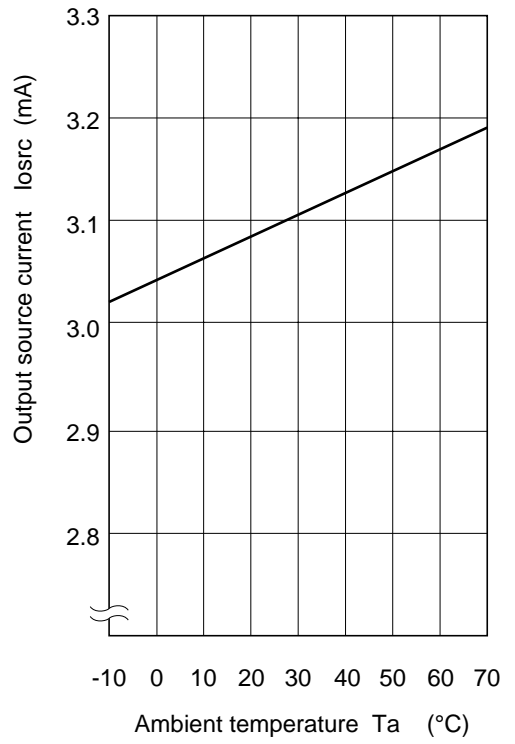
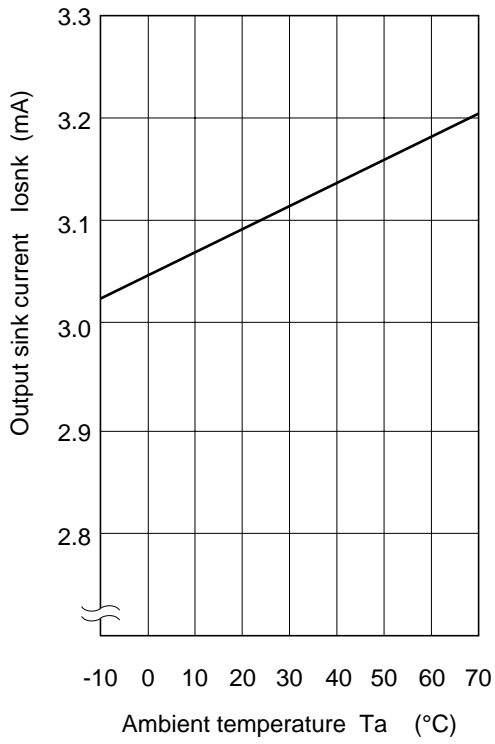
2. Offset between pins 11 and 14.

3. See timing diagrams.

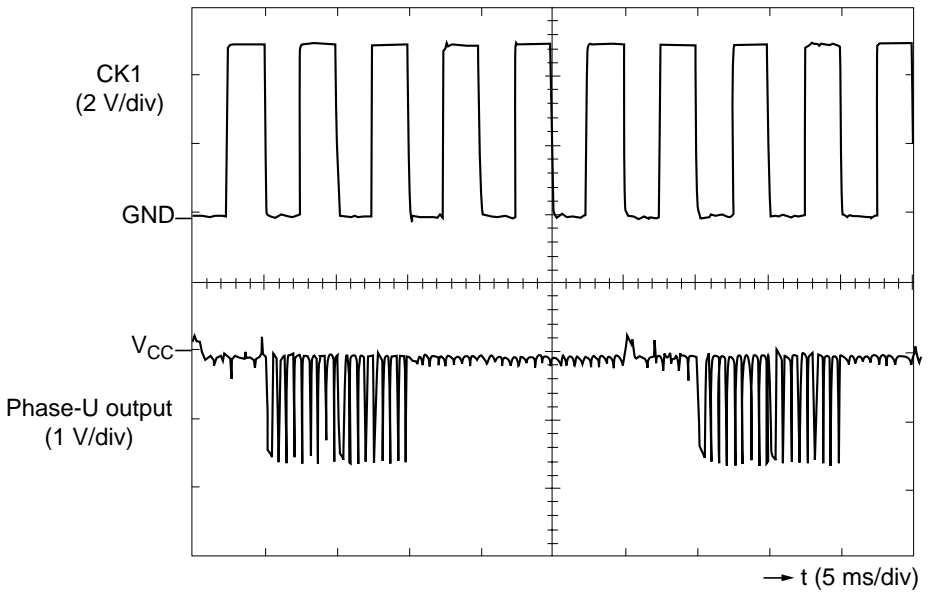
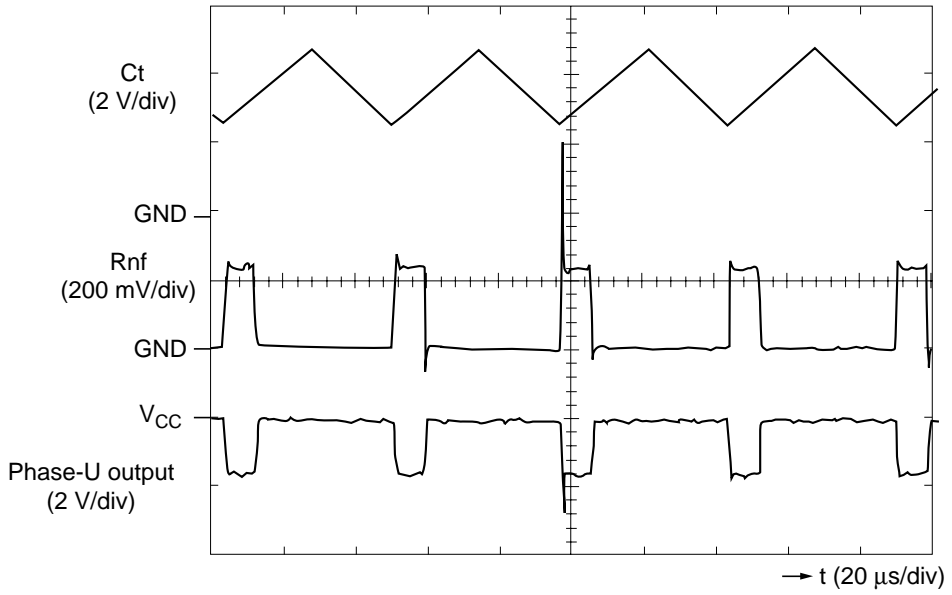
Reference Data



- Notes:
1. $I_{osnk} + I_{osrc}$ is the current during three-channel output.
 2. I_{osnk} is the current during two-channel output.

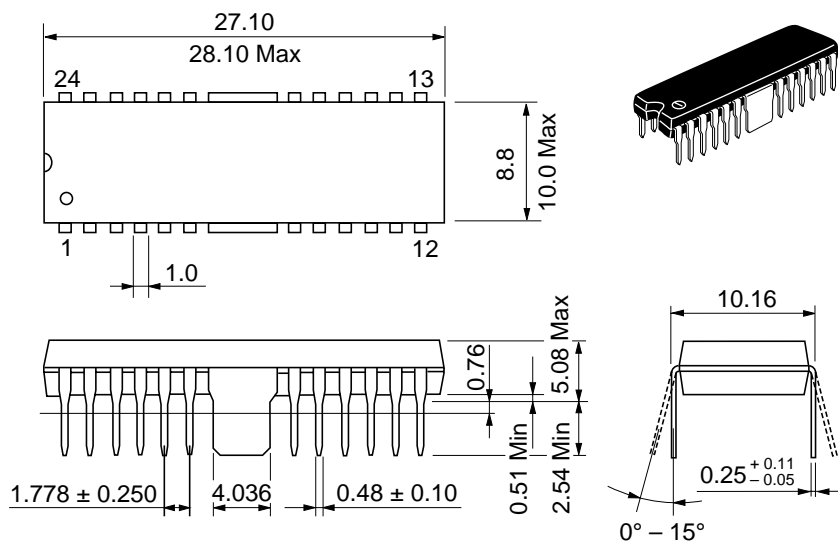


In-Circuit Waveform Characteristics



Package Dimensions

Unit: mm



Hitachi code	DP-24TS
EIAJ code	—
JEDEC code	—

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