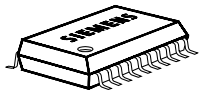
SIEMENS

Quad Driver Incl. Short-Circuit Signaling FZL 4146

Bipolar IC

Features

- Short-circuit signaling
- Four driver circuits for driving power transistors
- Turn-ON threshold setting from 1.5 to 7 V



P-DSO-20-7

Type	Ordering Code	Package
FZL 4146 G	Q67000-H8743	P-DSO-20-7 (SMD)

General Description

The IC comprises four driver circuits capable of driving power transistors (PNP or PMOS). The output transistors are protected against short-circuit to ground and supply voltage. The turn-ON threshold can be set from 1.5 V to 7 V. Overload at one or several outputs will be indicated at pin SQ (signaling output). The corresponding power transistors are then protected by changeover to clock-governed operation.

Circuit Description

Each driver circuit has one active high driver input DI and a common enable input ENA (active high) is provided for all stages. The Q output is designed to drive the output transistors. The load current is sampled and, if necessary, limited via pin W. If the load current exceeds the preset value, the output stage switches off. Switching-ON again is provided by the built-in clock generator T. Its operation requires an external capacitor C_e at pin CE. If C_e is bridged by a break-key, switching-ON can only be carried out by operating this key. The duty cycle of the clock generator is 1:47 (e.g. 45 µs/2.1 ms with C_e = 10 nF). The clock generator is privileged versus the current sensor shut down. When the supply is connected, the internal RS-FF goes into the state corresponding to the released output.

The turn-ON threshold at input Dl and ENA can be set via pin TS from 1.5 to 7 V.

V_{TS} = 0 V … 1.5 V	Turn-ON threshold = 1.5 V
V_{TS} = 1.5 V … 7 V	Turn-ON threshold = V_{TS}
V_{TS} = V_S	Turn-ON threshold = 7 V

Inputs Dl, ENA and W are proof against line break, i.e. an open input at Dl or ENA corresponds to input L, open input W corresponds to overcurrent. If input TS is open, the highest turn-ON threshold is provided.

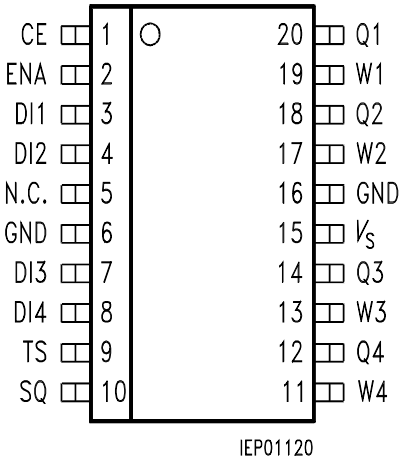
The internal current supply B and the undervoltage monitor UV ensure that in case of a supply voltage that is below the V_S turn-OFF threshold, outputs Q and SQ are disabled and the inputs go high-impedance. Basic functioning is possible within the range from V_S turn-OFF threshold to 4.5 V.

In case of overcurrent or short-circuit to ground at any output stage the signaling output (SQ) will go low. In clock-governed operation (i.e. when there is automatic switching-ON by the clock and not by a key), SQ goes high and low at the clock rate as long as a short-circuit or overload is present. SQ is an open-collector output.

Any input and output is ESD proof within the limit values.

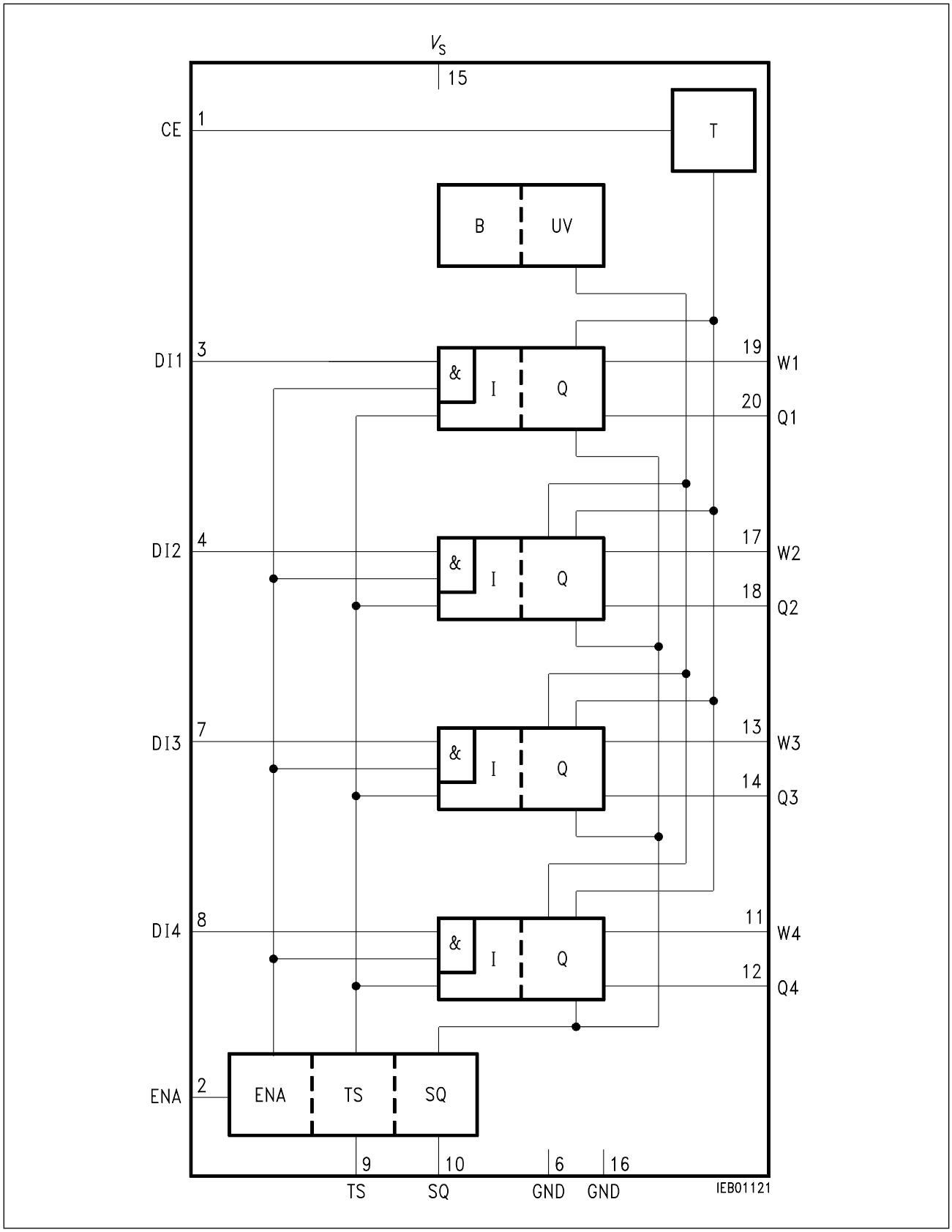
Pin Configuration
(top view)

P-DSO-20-7



Pin Definitions and Functions

Pin	Symbol	Function
1	CE	Pin for C_e
2	ENA	Enable input for drivers 1 to 4
3	DI1	Input driver 1
4	DI2	Input driver 2
5	N.C.	Not connected
6	GND	Ground
7	DI3	Input driver 3
8	DI4	Input driver 4
9	TS	Threshold changeover for all inputs
10	SQ	Short-circuit signaling output for drivers 1 to 4
11	W4	Output current sensor driver 4
12	Q4	Output driver 4
13	W3	Output current sensor driver 3
14	Q3	Output driver 3
15	V_S	Supply voltage
16	GND	Ground
17	W2	Output current sensor driver 2
18	Q2	Output driver 2
19	W1	Output current sensor driver 1
20	Q1	Output driver 1



Block Diagram

Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Supply voltage	V_S	– 0.3	40	V	
Supply voltage	V_S	– 0.3	45	V	100 ms, 5 s interval
Supply voltage	V_S	– 0.3	48	V	120 µs
Reverse supply current in GND	I_{GND}		0.5	A	1) 4)
Input voltage at DI, ENA, TS	$V_{DI, ENA,TS}$	– 5	40	V	
Input voltage at DI, ENA, TS	$V_{DI, ENA,TS}$	– 5	45	V	100 ms, 5 s interval
Output voltage Q	V_Q	V_S – 8	V_S	V	min. – 0.3 V
Current in Q	I_Q	– 10	3	mA	18)
Voltage at W	V_W	V_S – 6.5	V_S + 5	V	min. – 0.3 V, max. 45
Voltage at W	V_W	V_S – 12	V_S + 5	V	min. – 0.3 V, max. 45 V 2)
Voltage at CE	V_C	– 0.3	V_S	V	min. – 0.3 V, max. 45 V 3)
Voltage at SQ	V_{SQ}	– 0.5	45	V	Output high
Input current DI, ENA, TS	$V_{DI, ENA, TS}$	– 3	3	mA	4)
Input current DI, ENA, TS	$V_{DI, ENA, TS}$	– 5	5	mA	100 ms, 5 s interval
Input current DI, ENA, TS	$V_{DI, ENA, TS}$	– 10	10	mA	10 µs, 500 µs interval

Notes: 1) An adequate resistor in the GND line can provide protection in case of wrong polarization of V_S. It should be noted, however, that in this case all pins may become conductive across GND.

2) Loading may lead to degradation and thus to a shift of the switching threshold at W. (Characteristics: switching threshold at W).
Short loading may lead to a deviation of approx. 20 mV.

3) In case of short-circuit of V_S, the capacitance stored in C_e during previous operation will not damage the IC.

4) Note the power loss.

Absolute Maximum Ratings (cont'd)

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Current in SQ	I_{SQ}	– 3	8	mA	Output low
Current in W	I_W	– 5	5	mA	1 ms, 50 ms interval [5]
Current in W	I_W	– 10	10	mA	10 µs, 500 µs interval [5]
Junction temperature	T_j	– 40	150	°C	
Storage temperature	T_{stg}	– 50	150	°C	
Therm. resistance, system-ambient	$R_{th\ SA}$		95	K/W	
Therm. resistance, system-packag.	$R_{th\ SP}$		25	K/W	[6]
ESD strength acc. to MIL - hrs. 883 Meth. 3015 (100 pF/1.5 kΩ, 5 discharges/polarity)	V_{ESD}	– 2	2	kV	
Burst strength of the inputs/ outputs Q and W connected to the power transistors (in acc. with IEC publ. 801-4)	V_{Burst}	300		V	[7]
Junction temperature in normal operation during 15 years with 100 % ED	T_{j15}		125	°C	[8]

Notes: [5] Loading may lead to degradation and thus to a shift of the switching threshold at W. Unfrequent loading leads to a deviation of approx. 20 mV.
[6] Related to GND; the GND pins are connected with the chip carrier via the leadframe.
[7] If it can be prooved with samples.
[8] During normal operation, the failure rate is ≤ 100 fit acc. to SN 29500 at a junction temperature of 75 °C.

Operating Range

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Supply voltage[11)]	V_S	4.5	40	V	V_{TS} = 0 ... 1.5 V
Supply voltage[12)]	V_S	V_{TS} + 3	40	V	V_{TS} = 1.5 ... 7 V
Supply voltage[13)]	V_S	10	40	V	$V_{TS} = V_S$
Supply voltage rise	dV_S/dt	– 1	1	V/µs	[20)]
Junction temperature	T_j	– 25	150	°C	
Time-determining capacitor of the clock generator	C_e	1	100	nF	[10)]
Input voltage	$V_{DI, ENA, TS}$	– 2	40	V	[14) 15) 16) 17) 19)]
Current at output SQ	I_{SQ}	– 1	6	mA	

Notes:

9) W pins that remain open, must be connected to V_S.

10) The C_e value depends on the desired pulse width t_p during short circuit. It applies: C_e = 0.25 mS x t_p.

11) At an input threshold = 1.5 V

12) At an input threshold = 1.5 V to 7 V

13) At an input threshold = 7 V

14) This function is also ensured for 40 V ≤ V_S ≤ 45 V and – 40 °C ≤ T_j ≤ – 25 °C as long as 0 V ≤ $V_{DI, ENA, TS}$ ≤ 40 V.

15) The outputs Q are disabled even if – 3 V ≤ $V_{DI, ENA}$ ≤ – 2 V or – 1 mA ≤ $I_{DI, ENA}$ ≤ 50 µA and V_S – 5 V ≤ V_W ≤ V_S + 5 V, max. 45 V.

16) The outputs Q are enabled even if 40 V ≤ $V_{DI, ENA}$ ≤ 45 V and V_S – 0.2 V ≤ V_W ≤ V_S + 5 V, max. 45 V.

17) Current limiting and disabling of outputs Q are ensured even if 40 V ≤ $V_{DI, ENA}$ ≤ 45 V and V_S – 5 V ≤ V_W ≤ V_S – 0.4 V.

18) Dynamic charge reversal of a 2-nF capacitor as in **figure 1** is permissible (corresponds to short circuit to conducting output in P-channel MOSFET)

19) Proper working of the IC is also ensured if, before V_S is turned-On, an input voltage $V_{DI, ENA}$ is present in the permissible range (footnote 15).

20) At 10 V/µs short-term malfunction is possible, but never a latch-up.

Characteristics

Supply voltage 4.5 V ≤ V_S ≤ 40 V, junction temperature – 25 °C ≤ T_j ≤ 125 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Current consumption	$I_{s,\ OFF}$			5	mA	V_{ENA} = 0 V, $V_w = V_S$ 4)
Current consumption	$I_{s,\ ON}$			13.5	mA	$V_{ENA} = V_{DI} = V_w = V_Q = V_S$; V_{TS} = 0 V 3)
H-input voltage at DI, ENA	$V_{I\,H}$	2			V	V_{TS} = 0 V
H-input voltage at DI, ENA	$V_{I\,H}$	6.8			V	$V_{TS} = V_S$
L-input voltage at DI, ENA	$V_{I\,L}$			0.7	V	V_{TS} = 0 V
L-input voltage at DI, ENA	$V_{I\,L}$			4.8	V	$V_{TS} = V_S$
Input hysteresis	V_{HI} V_{HI}	30 30	100 100	300 300	mV mV	0 V ≤ $V_{TS} \le V_S \le$ 30 V 2 V ≤ $V_{TS} \le V_S$
Input current DI, ENA 1), 7)	$I_{DI,\ ENA}$	50		200	µA	1.5 V ≤ $V_{DI,\ ENA} \le$ 30 V
Input current DI, ENA	$I_{DI0,\ ENA0}$			100	µA	0 V ≤ $V_{DI,\ ENA} \le$ 30 V, V_S = 0 V
L-output voltage at SQ	$V_{SQ\,L}$			0.5	V	I_{SQ} = 5 mA, $V_W = V_S$ – 2 V
Leakage current output SQ	$I_{SQ\,H}$			10	µA	$V_W = V_S$
Output current Q	I_{Q0}	0.6		1.6	mA	V_S – 2 V ≤ $V_Q \le V_S$
Current from TS	$-I_{TS}$	2	5	10	µA	V_{TS} = 0.7 V
Current in W	I_W			100	µA	V_S – 2 V ≤ $V_W \le V_S$
Switching threshold at W 2)	V_W	V_S – 0.25	V_S – 0.3	V_S – 0.35	V	

Notes see page 11.

Characteristics (cont'd)
Supply voltage 4.5 V ≤ V_S ≤ 40 V, junction temperature – 25 °C ≤ T_j ≤ 125 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Current in W	I_W			100	µA	V_S – 2 V ≤ V_W ≤ V_S
Charge current from CE Discharge current from CE	$-I_{Ce}$ I_{Ce}		5 235		µA µA	
Upper switching threshold at CE Lower switching threshold at CE	V_{CU} V_{CL}			2.4 1.4	V V	
V_Q at overcurrent	V_{QR} [6]	V_S – 0.4 V			V	V_W = V_S – 2 V, I_Q = – 20 µA
V_Q at output disable	V_{QL} [6]	V_S – 0.4 V			V	V_{ENA} = 0 V, I_Q = – 20 µA, 0 V ≤ V_S ≤ 40 V
Signal run time LH	t_{PLH}			50	µs	
Signal run time HL	t_{PHL}			50	µs	
Pulse width	t_P	33	45	65	µs	C_e = 10 nF
Duty cycle	t_P/t_0	1:55	1:47	1:40		C_e = 10 nF
Delay time of the short-circuit signaling	t_{PWM} [5]			10	µs	V_C = 0 V
Duration of the negative spikes at input W, which do not result in switching off	t_{VZ}	1			µs	

Notes see page 11.

Characteristics (cont'd)
Supply voltage 4.5 V ≤ V_S ≤ 40 V, junction temperature – 25 °C ≤ T_j ≤ 125 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Difference between V_{TS} and input switching threshold ENA, DI during transition from L to H	$V_{DIH} - V_{TS}$	– 0.2		0.2	V	2 V ≤ V_{TS} ≤ 4.8 V
Idling voltage at output Q	V_{QH}	V_S – 13	V_S – 11.5	V_S – 10	V	V_S ≥ 18 V
V_S turn-Off threshold	V_{TSV}	2.5		4.5	V	$V_Q > V_{QL}$; I_Q = – 20 µA
Resistance across Q and V_S	R_Q	8	13	19	kΩ	V_{ENA} = 0 V; I_Q = – 100 µA $R_Q = (V_S - V_Q)/0.1$ mA
Z-diode internal resistance	R_Z		20	50	Ω	V_{ENA} = 0 V; I_{Q1} = – 3 mA I_{Q2} = – 8 mA, $R_Q = \Delta V_Q/5$ mA

Footnotes for the Characteristics

1) The given limit values apply to inputs DI, ENA, if they are not measured, from 0 to 40 V.
2) The layout provides an adaption of $V_{wtyp.}$ from V_S – 0.3 V to V_S – 0.4 V or V_S – 0.48 V by simply changing of the ALU mask.
3) All inputs DI1 to DI4 and W1 to W4 as well as Q1 to Q4
I_{SON} means the sum of all currents flowing from the voltage source V_S into the IC, i.e.
$I_{SON} = I_S + \Sigma I_{DI} + \Sigma I_{ENA} + \Sigma I_W + \Sigma I_Q$.
4) All other pins are open.
5) The delay time of loop W → I regulator → RS-FF → AND → current source → Q is unaccessable for measurement without external wiring due to fast reaction of the current regulator. For this reason, in case of overload, the above mentioned switch-OFF delay time is replaced by the delay time for input W → output SQ.
Measurement: jump function at W from $V_W = V_S$ to $V_W = V_S$ – 1 V
6) I_Q = leakage current I_{CBO} of the external PNP-driver transistor
7) For $V_{DI, TS}$ < 1.5 V, $I_{DI, ENA}$ remains below its minimum value; it is however ensured that in case of open inputs the corresponding outputs will be safely disabled.

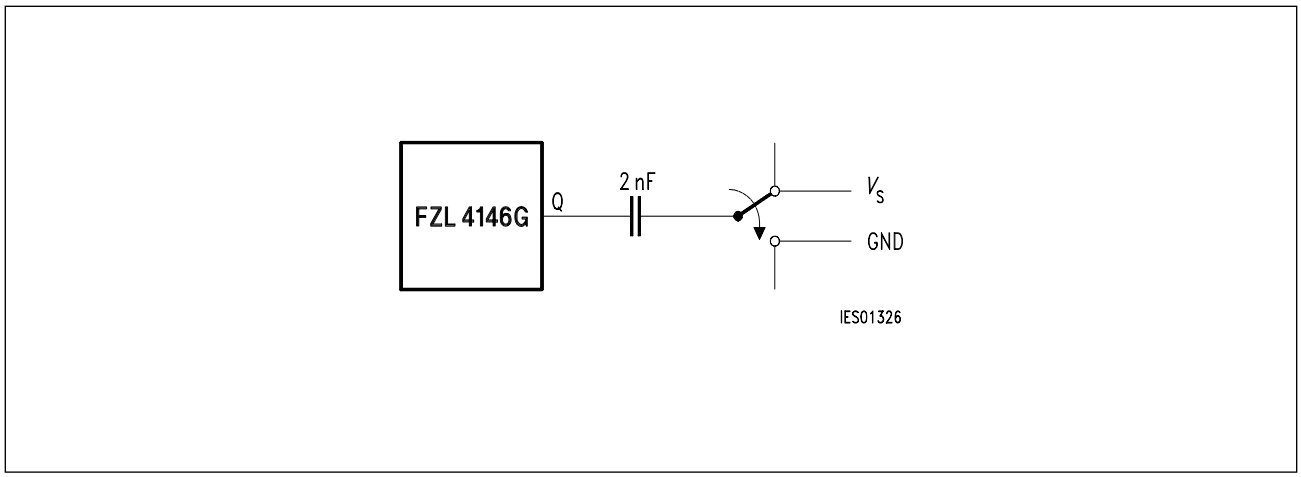


Figure 1

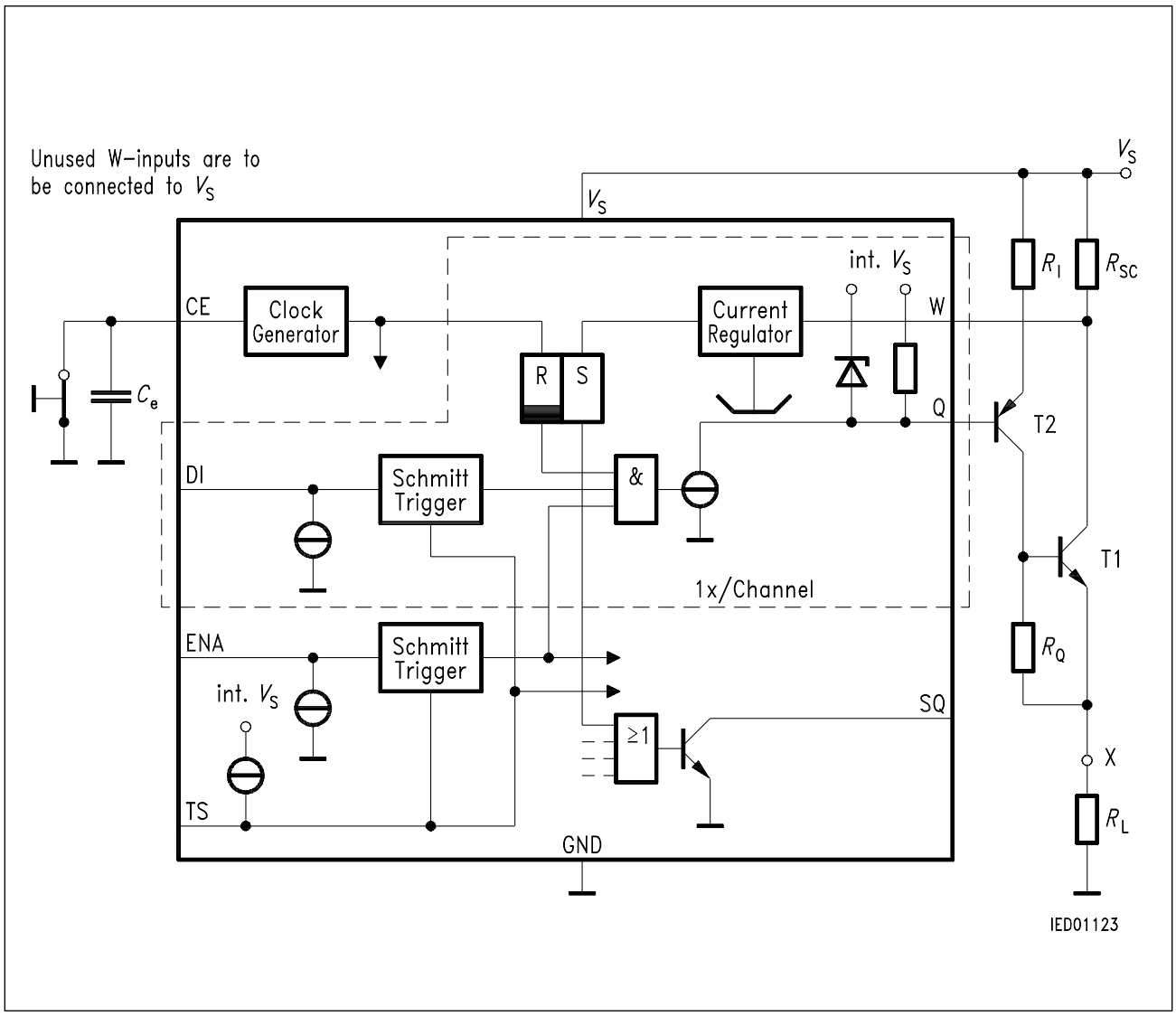


Figure 2
Application Circuit

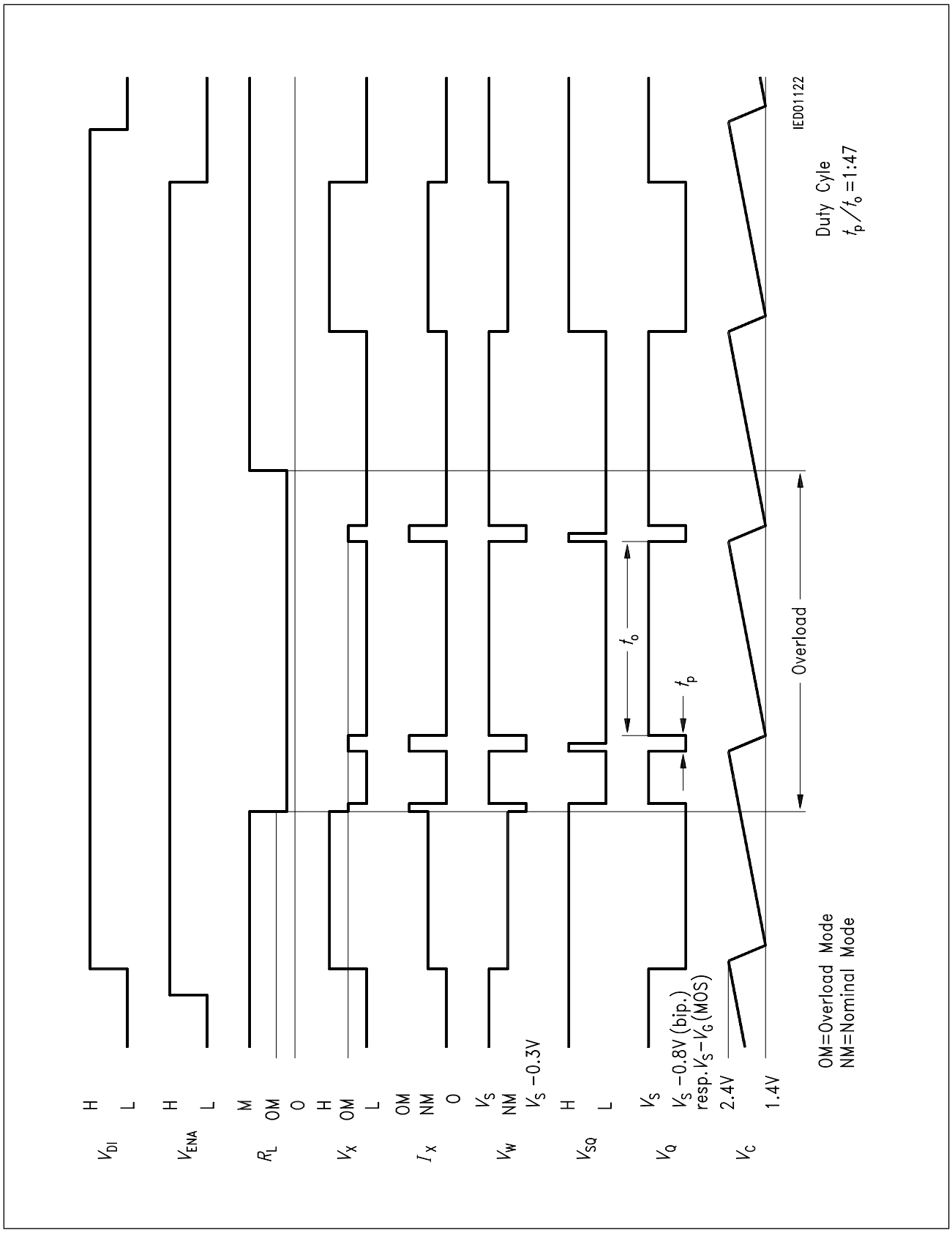
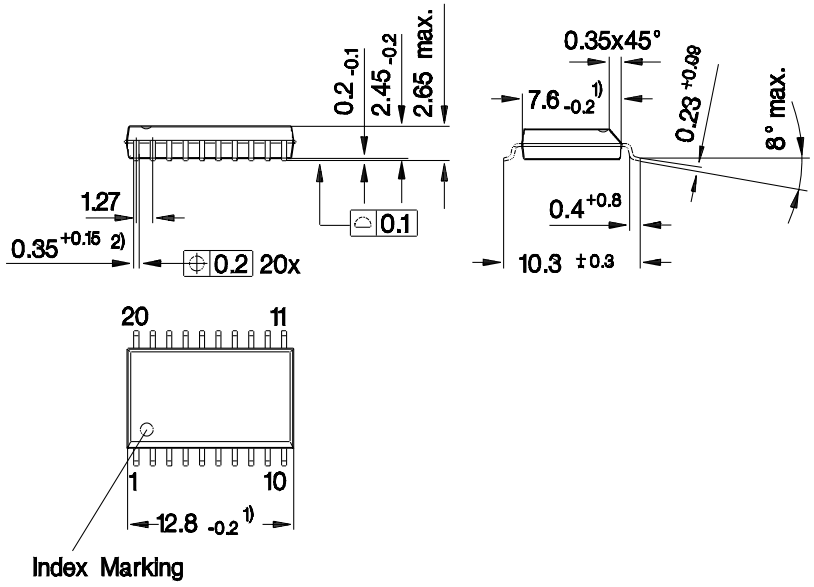


Figure 3
Operating Mode: Automatic Turn-ON after Overload

Package Outlines

P-DSO-20-7
(Plastic Dual Small Outline Package)



1) Does not include plastic or metal protrusion of 0.15 max. per side
2) Does not include dambar protrusion

GPS05094

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.

SMD = Surface Mounted Device

Dimensions in mm