

Power Amplifier for PHS

Description

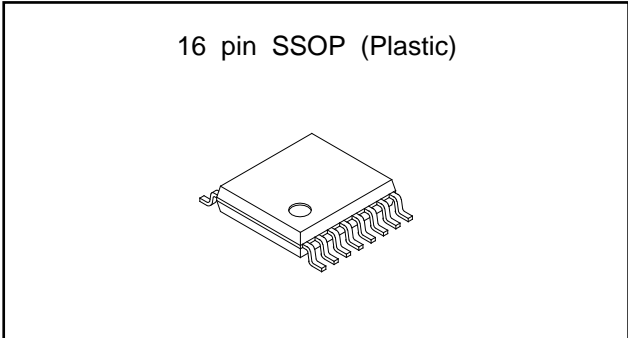
The CXG1030N is a power amplifier for PHS. This IC is designed using the Sony's GaAs J-FET process and operates at a single power supply.

Features

- Output power 21 dBm
- Positive power supply 3.0 V
- Low current consumption 170 mA
- High power gain 39 dB Typ.
- Small mold package 16-pin SSOP

Structure

GaAs J-FET MMIC



Absolute Maximum Ratings (Ta=25 °C)

- Supply voltage V_{DD} 6 V
- Voltage between gate and source V_{GS0} 1.5 V
- Drain current I_{DD} 500 mA
- Power dissipation P_D 3 W
- Channel temperature T_{ch} 175 °C
- Operating temperature T_{op} -35 to +85 °C
- Storage temperature T_{stg} -65 to +150 °C

Electrical Characteristics

V_{DD}=3.0 V, V_{CTL}=2.0 V, f=1.90 GHz

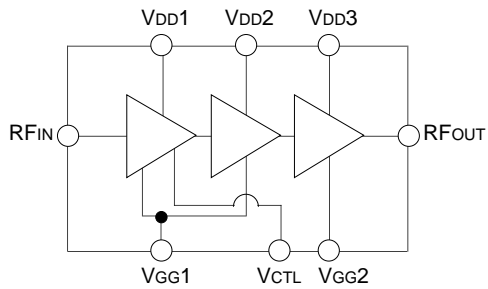
(Ta=25 °C)

Item	Symbol	Min.	Typ.	Max.	Unit
*1 Current consumption	I _{DD}		170		mA
*1 Gate voltage adjustment value	V _{GG2}	0	0.4	0.8	V
Output power	P _{OUT}	21			dBm
*2 Power gain	G _P	36	39		dB
*2 Adjacent channel leak power ratio (600 kHz ±100 kHz)	ACPR600		-59	-54	dBc

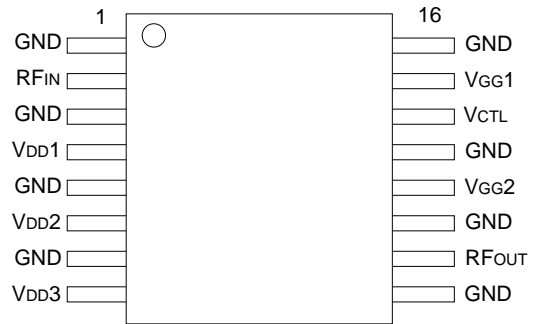
*1 Values where V_{GG1} and V_{GG2} are adjusted so that I_{DD} becomes 170 mA when 21.0 dBm is output.

*2 When 21.0 dBm is output.

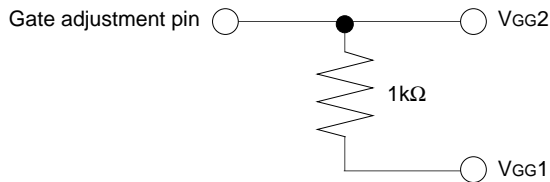
Block Diagram



Pin Configuration

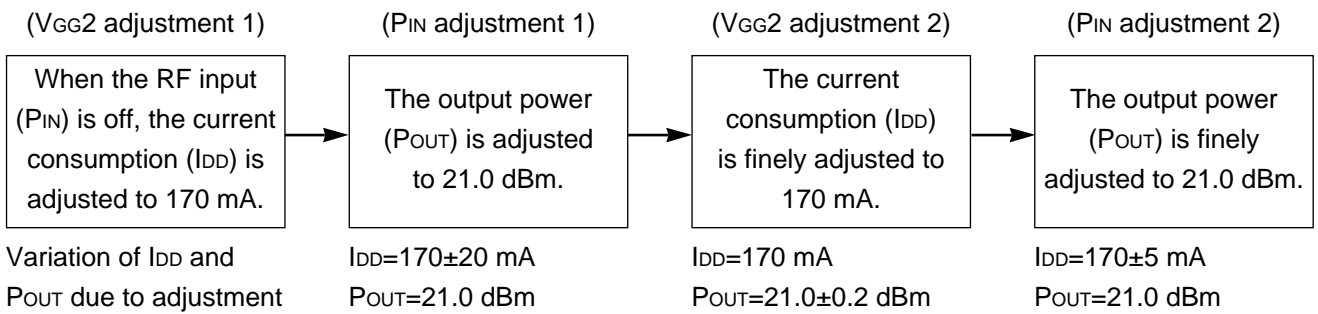


Gate Bias Circuit

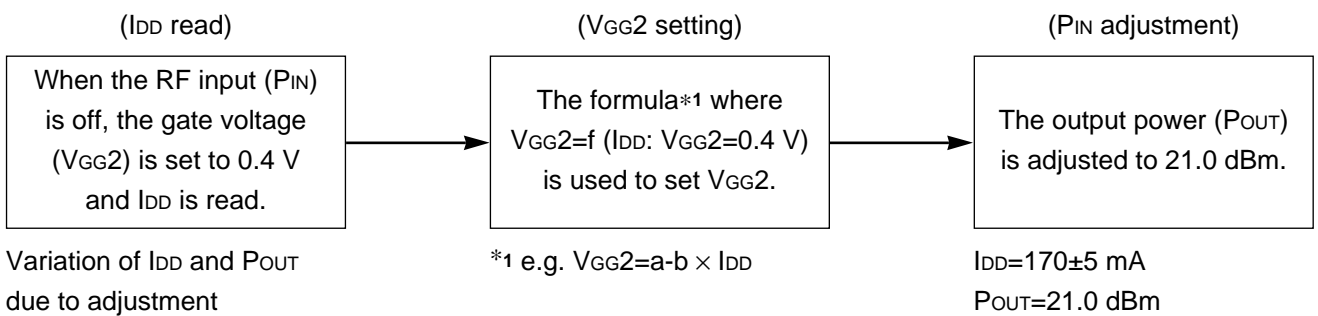


Recommended Current Adjustment Method

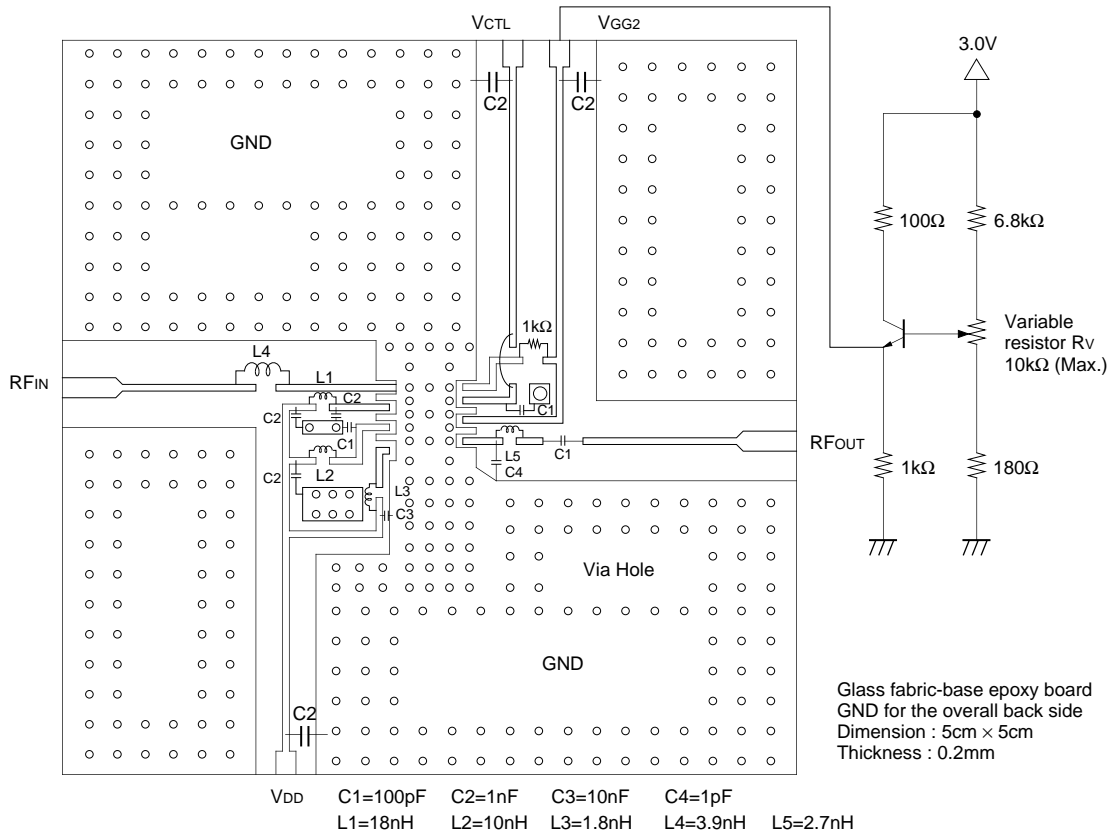
(1) VGG2/PIN separate adjustment



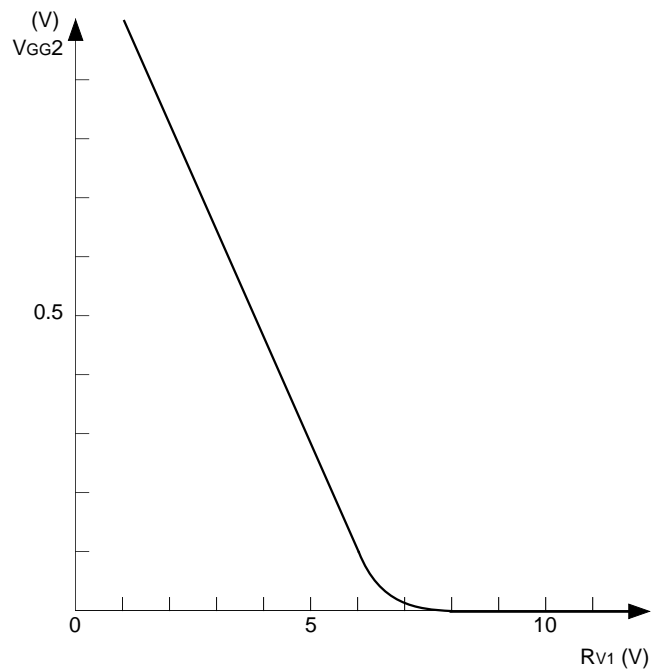
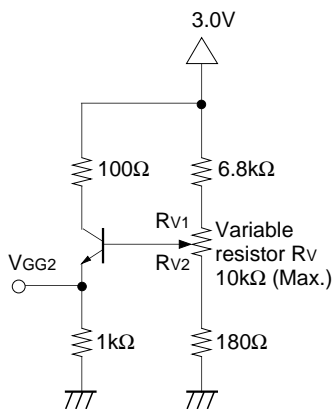
(2) Simple adjustment



Recommended Evaluation Circuit

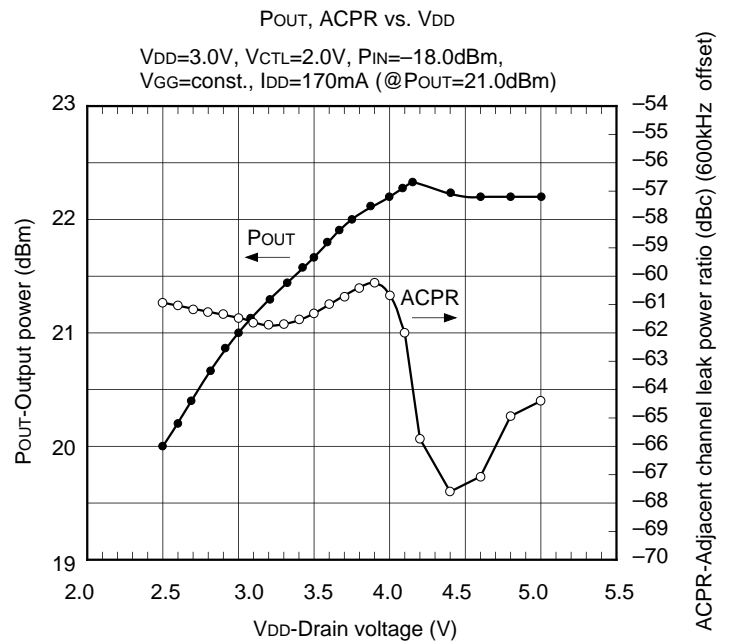
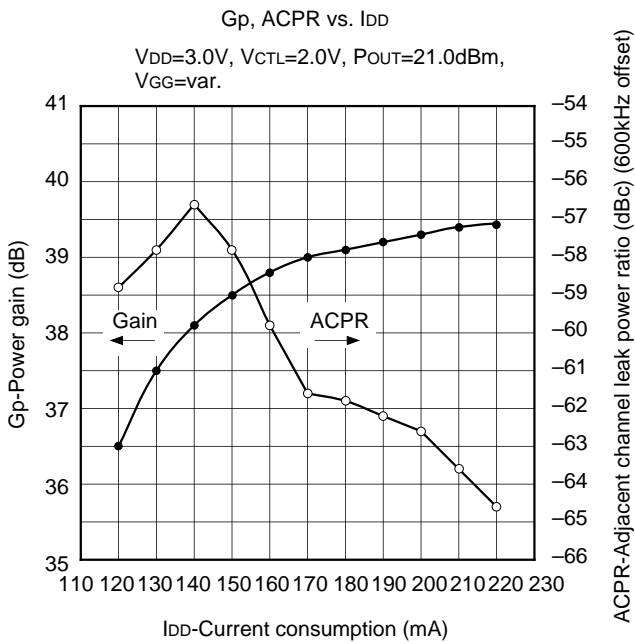
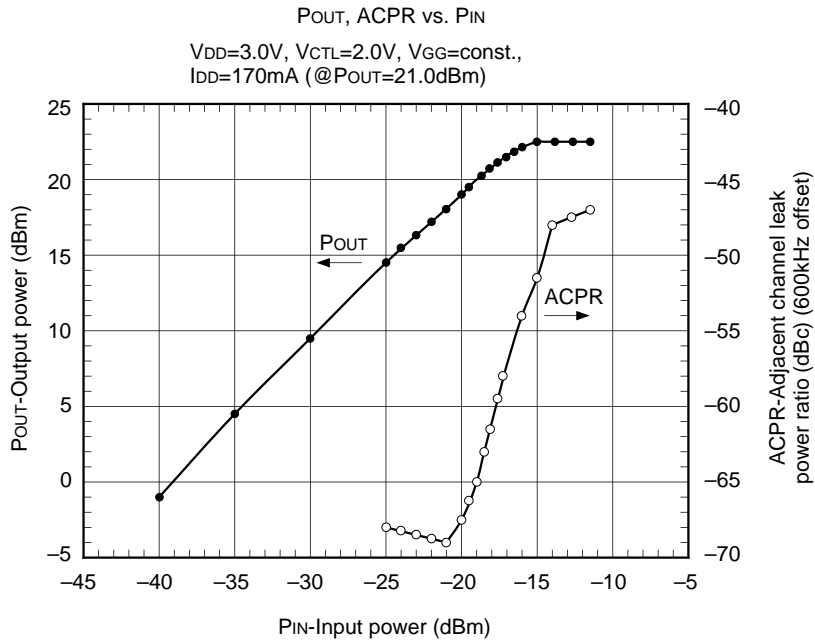


Recommended Gate Bias Circuit and Circuit Characteristics



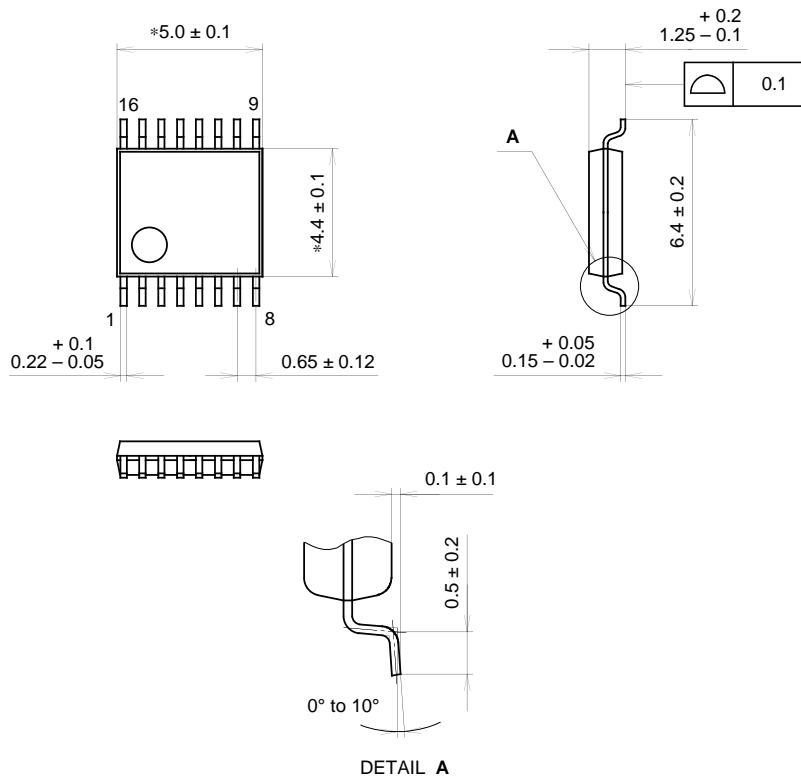
Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Example of Representative Characteristics (Ta=25 °C)



Package Outline Unit : mm

16PIN SSOP (PLASTIC)



NOTE: Dimension "*" does not include mold protrusion.

* : PALLADIUM PLATING
 This product uses PdPPF
 (Palladium Pre-Plated Lead Frame).

PACKAGE STRUCTURE

SONY CODE	SSOP-16P-L01
EIAJ CODE	SSOP016-P-0044
JEDEC CODE	_____

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER / PALLADIUM PLATING
LEAD MATERIAL	COPPER / 42 ALLOY
PACKAGE WEIGHT	0.1g