SONY

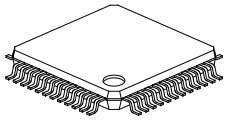
CXD2312R

9-bit 20MSPS Video A/D Converter

Description

The CXD2312R is a 9-bit CMOS A/D converter for video applications. This IC is ideally suited for the A/D conversion of video signals in TVs, VCRs, camcorders, etc.

48 pin LQFP (Plastic)



Structure

Silicon gate CMOS IC

Features

- Resolution: 9-bit ±0.5 LSB (D.L.E.)
- Maximum sampling frequency: 20MSPS
- Low power consumption: 130mW (at 20MSPS typ.) (Not including reference current)
- TTL compatible input
- Tri-state TTL compatible output (DV_{DD} = 3.3V)
- Low input capacitance
- Reference impedance: 300Ω (typ.)

Absolute Maximum Ratings (Ta = 25°C)

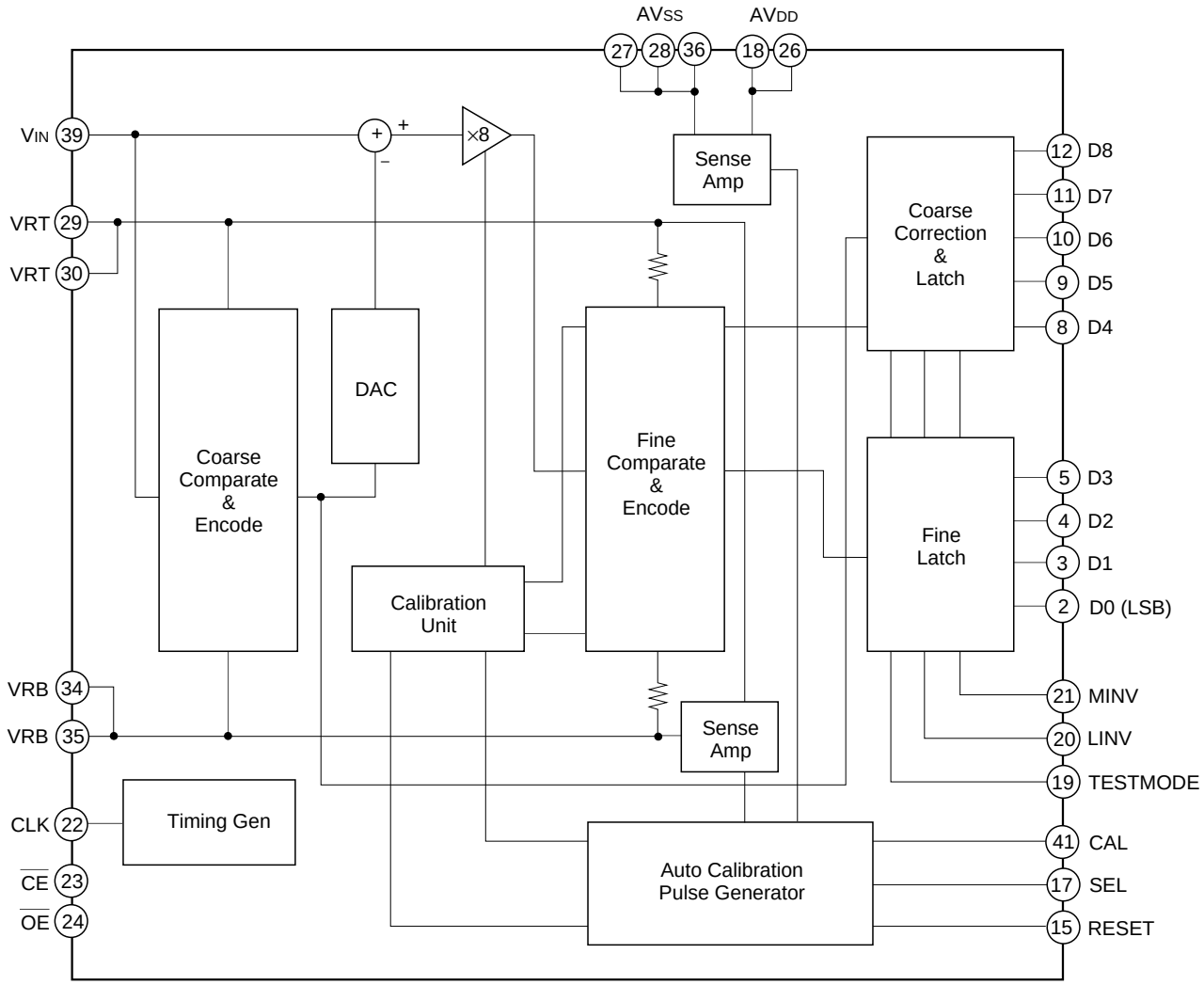
• Supply voltage	V_{DD}	7	V
• Reference voltage	VRT, VRB	V_{DD} + 0.5 to V_{SS} – 0.5	V
• Input voltage (analog)	V_{IN}	V_{DD} + 0.5 to V_{SS} – 0.5	V
• Input voltage (digital)	V_{IH}, V_{IL}	V_{DD} + 0.5 to V_{SS} – 0.5	V
• Output voltage (digital)	V_{OH}, V_{OL}	V_{DD} + 0.5 to V_{SS} – 0.5	V
• Storage temperature	Tstg	–55 to +150	°C

Recommended Operating Conditions

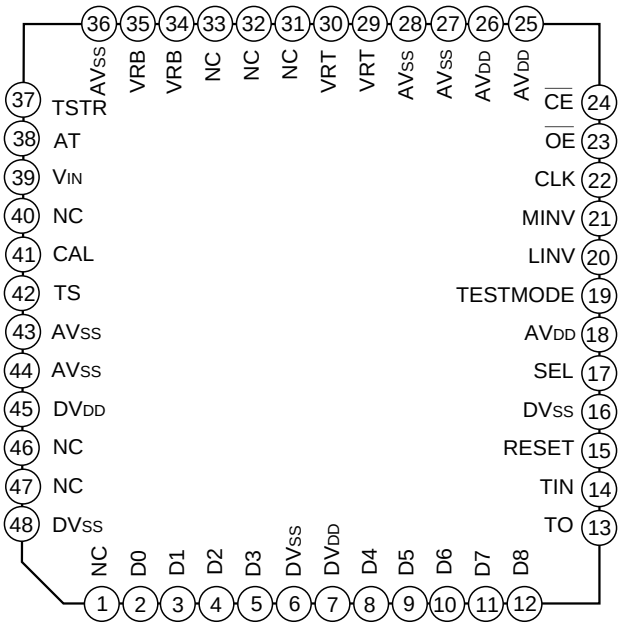
• Supply voltage	AV_{DD}, AV_{SS}	5.0 ± 0.25	V
	DV_{DD}, DV_{SS}	3.0 to 5.25	V
	$\lvert DV_{SS} - AV_{SS} \rvert$	0 to 100	mV
• Reference input voltage	VRB	More than 1.8	V
	VRT	to AV_{DD} – 0.4	V
• Analog input	V_{IN}	More than 1.8Vp-p	
• Clock pulse width	$T_{PW}1$	25 (min.)	ns
	$T_{PW}0$	25 (min.)	ns
• Operating ambient temperature			
	Topr	–20 to + 75	°C

E94Z29C79-PS

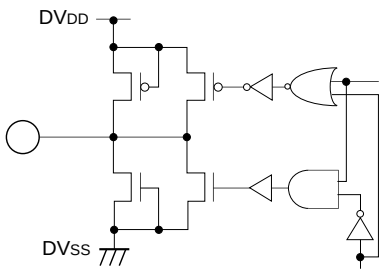
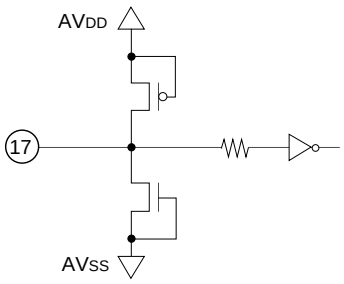
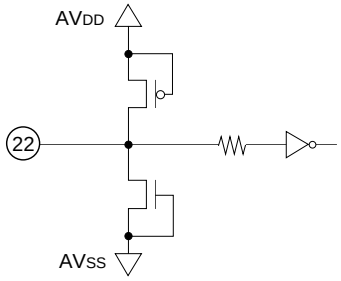
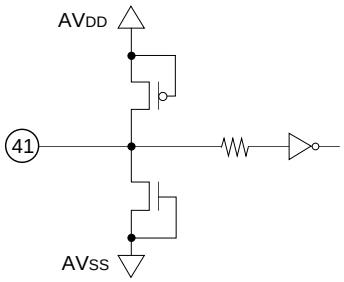
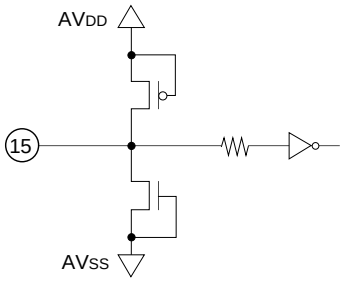
Block Diagram

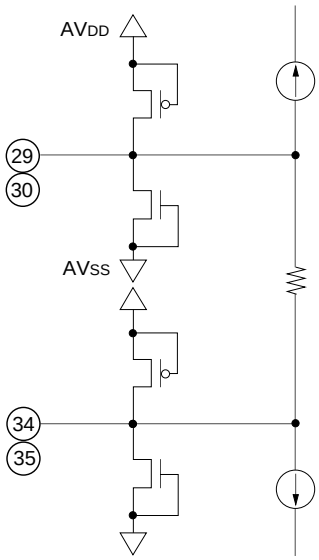
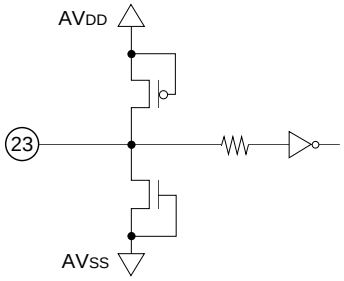
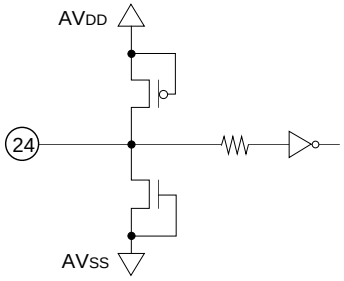


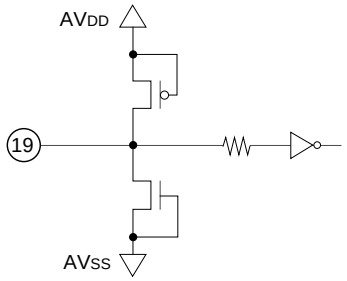
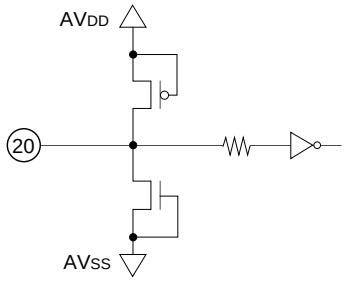
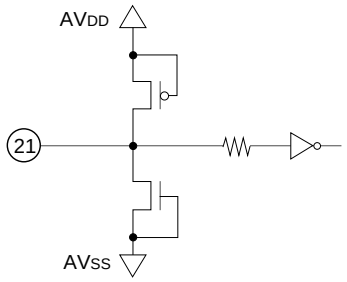
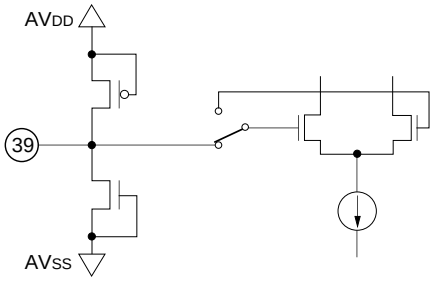
Pin Configuration



Pin Description

Pin No	Symbol	Equivalent circuit	Description
2 to 5 8 to 12	D0 to D8		D0 (LSB) to D8 (MSB) output.
13	TO		Test pin. TS = High: High impedance state
7, 45	DVDD		Digital VDD.
6, 16, 48	DVSS		Digital VSS.
27, 28, 36, 43, 44	AVSS		Analog VSS.
17	SEL		Calibration input pulse select after completion of the startup calibration. High : Internal pulse generation Low : External input
22	CLK		Clock pin.
41	CAL		Calibration pulse input.
15	RESET		Calibration circuit reset and startup calibration restart.

Pin No.	Symbol	Equivalent circuit	Description
14	TIN		Test signal input. Normally fixed to AV_{DD} or AV_{SS}.
29, 30	VRT		Reference top.
34, 35	VRB		Reference bottom.
38	AT		Test signal output. TS = High: High impedance state
42	TS		Test signal input. Normally fixed to AV_{DD}.
37	TSTR		Test signal input. Normally fixed to AV_{SS}.
23	$\overline{OE}$		D0 to D8 output enable. Low : Output state High : High impedance state
24	$\overline{CE}$		Chip enable. Low : Active state High : Standby state

Pin No.	Symbol	Equivalent circuit	Description
19	TESTMODE		Test mode. High : Output state Low : Output fixed
20	LINV		Output inversion. High : D0 to D7 are inverted and output.
21	MINV		Output inversion. High : D8 is inverted and output.
18, 25, 26	AVDD		Analog VDD.
39	VIN		Analog input.

Digital Output

The following table shows the correlation between the analog input voltage and the digital output code (TESTMODE = 1, LINV, MINV = 0)

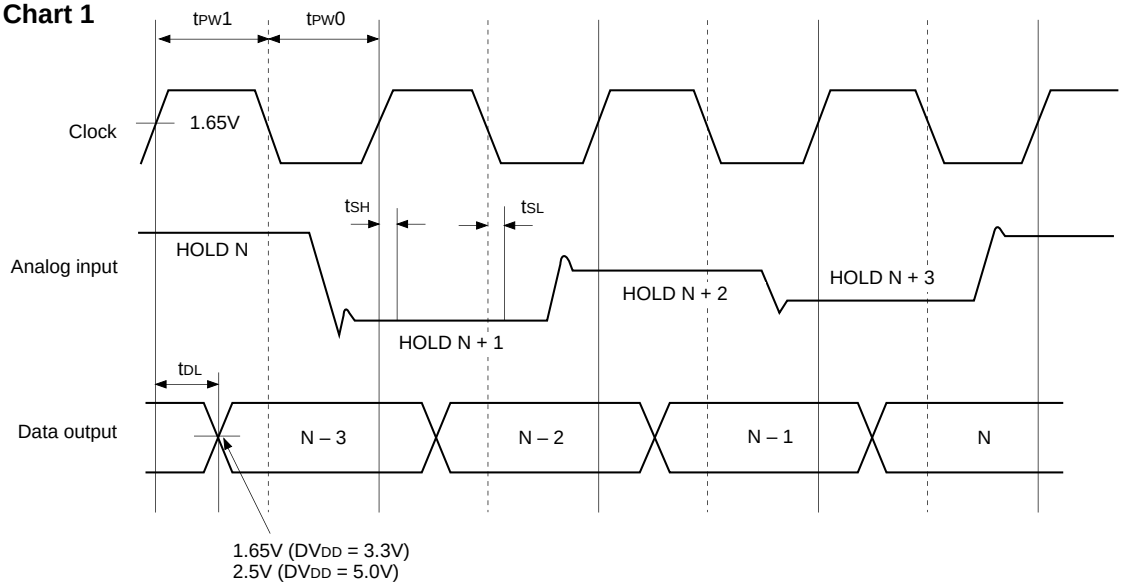
Input signal voltage	Step	Digital output code MSB LSB
VRT	0	1 1 1 1 1 1 1 1 1
	255	1 0 0 0 0 0 0 0 0
	256	0 1 1 1 1 1 1 1 1
VRB	511	0 0 0 0 0 0 0 0 0

The following table shows the output state for the combination of TESTMODE, LINV, and MINV states.

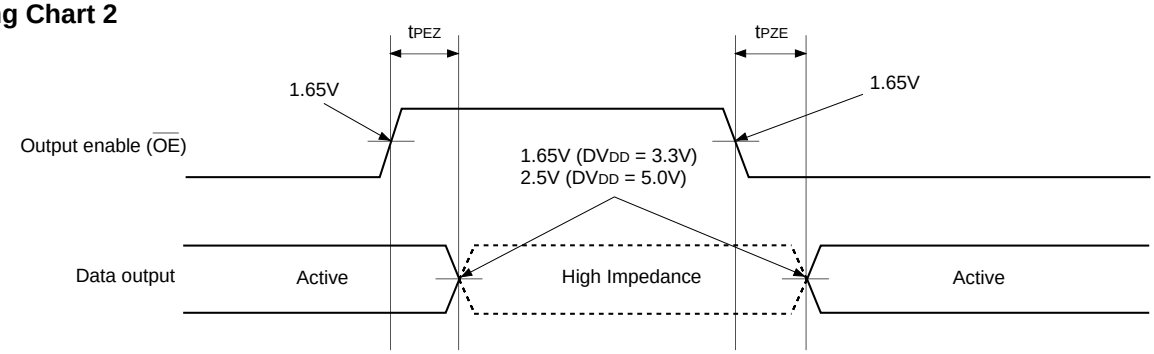
TESTMODE	LINV	MINV	D0	D1	D2	D3	D4	D5	D6	D7	D8
1	0	0	P	P	P	P	P	P	P	P	P
1	1	0	N	N	N	N	N	N	N	N	P
1	0	1	P	P	P	P	P	P	P	P	N
1	1	1	N	N	N	N	N	N	N	N	N
0	0	0	0	1	0	1	0	1	0	1	0
0	1	0	1	0	1	0	1	0	1	0	0
0	0	1	0	1	0	1	0	1	0	1	1
0	1	1	1	0	1	0	1	0	1	0	1

P: Forward-phase output N: Inverted output

Timing Chart 1



Timing Chart 2

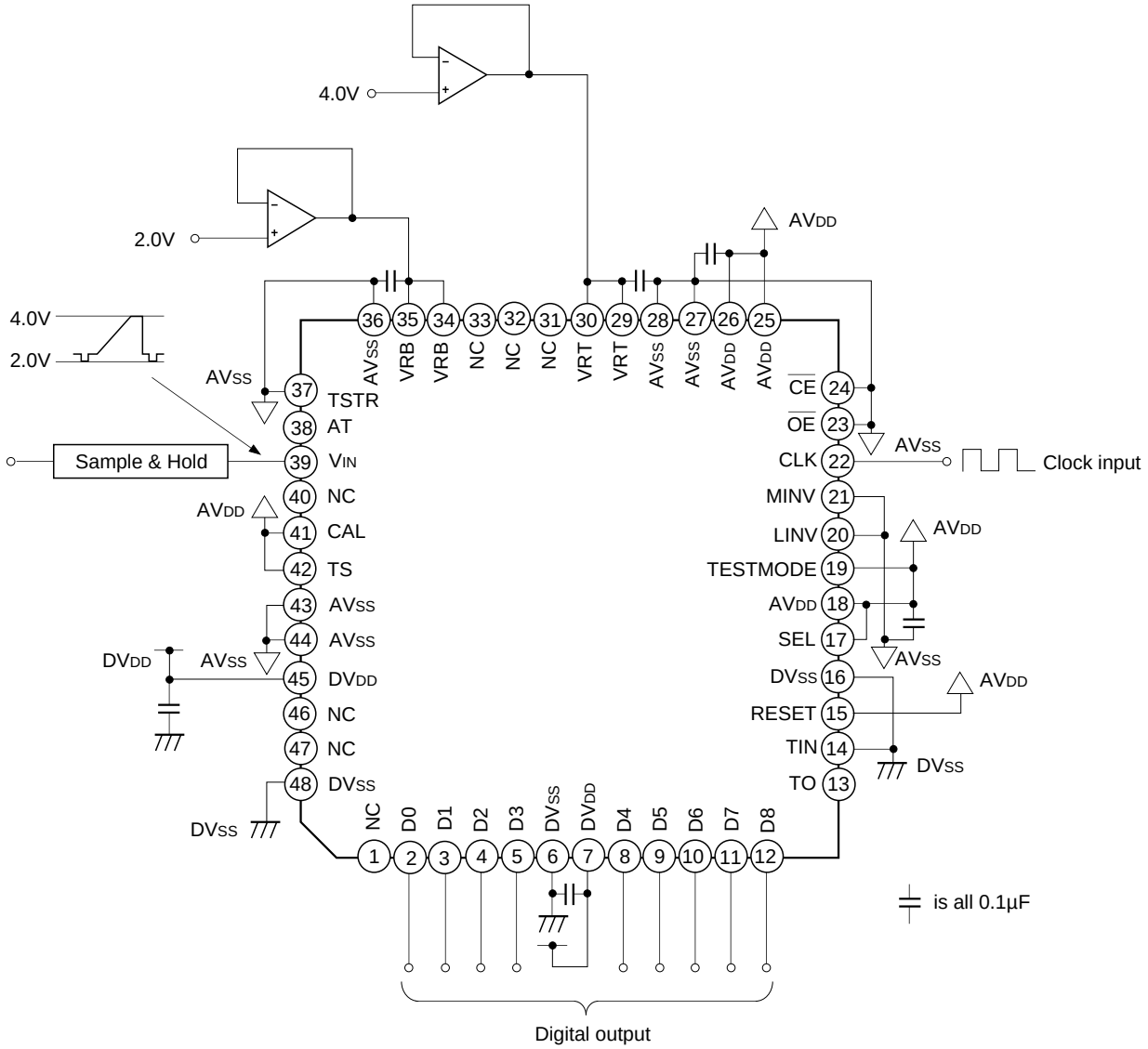


Electrical Characteristics (Fc = 20MSPS, AV_{DD} = 5V, DV_{DD} = 3.3V, VRB = 2.0V, VRT = 4.0V, Ta = 25°C)

Item		Symbol	Conditions		Min.	Typ.	Max.	Unit
Max. conversion rate		Fc max	F_{IN} = 1.0kHz triangular wave input		20			MSPS
Min. conversion rate		Fc min					0.5	
Supply current	Analog	IA_{DD}	F_{IN} = 1.0kHz triangular wave input		21	24	28	mA
	Digital	ID_{DD}			1.6	1.7	1.8	
Standby current	Analog	IA_{ST}	$\overline{CE}$ = High				1.0	
	Digital	ID_{ST}					1.0	µA
Reference pin current		I_{RT}			5.0	7.5	10.0	mA
		I_{RB}			3.0	5.5	8.0	
Analog input band		BW	–1dB			35		MHz
Analog input capacitance		C_{IN}				10		pF
Reference resistance value (VRT – VRB)		R_{REF}			210	300	390	Ω
Offset voltage		E_{OT}	E_{OT} = theoretical value-actual measured value		–30	8.0	30	mV
		E_{OB}	EOB = actual measured value-theoretical value		–30	12	30	
Startup calibration start voltage		$V_{CAL}1$	$AV_{DD} – AV_{SS}$			2.5		V
		$V_{CAL}2$	VRT – VRB			1.0		
Digital input voltage		V_{IH}	AV_{DD} = 4.75V to 5.25V		2.3			V
		V_{IL}					0.8	
Analog input current		A_{IH}	V_{IN} = 4V				20	µA
		A_{IL}	V_{IN} = 2V		–10			
Digital input current		I_{IH}	DV_{DD} = max	$V_{IH} = DV_{DD}$			5	µA
		I_{IL}		V_{IL} = 0V			5	
Digital output current		I_{OH}	$\overline{OE}$ = AV_{SS} DV_{DD} = min	$V_{OH} = DV_{DD} – 0.5V$	4.0			mA
		I_{OL}		V_{OH} = 0.4V	3.5			
Digital output current		I_{OZH}	$\overline{OE}$ = AV_{DD} DV_{DD} = max	$V_{OH} = DV_{DD}$			1	µA
		I_{OZL}		V_{OL} = 0V			1	
Tri-state output disable time		t_{PEZ}	Clock not synchronized for active → high impedance		20	25	30	ns
Tri-state output enable time		t_{PZE}	Clock not synchronized for high impedance → active		10	15	20	ns
Integral non-linearity error		E_L				±0.5	±1.0	LSB
Differential non-linearity error		E_D				±0.3	±0.5	
Differential gain error		DG	NTSC 40 IRE mod ramp, Fc = 14.3MSPS			1.0		%
Differential phase error		DP				0.3		deg
Output data delay		t_{DL}	C_L = 20pF		8	13	18	ns
Sampling delay		t_{SH}			0	6		ns
		t_{SL}				2	4	

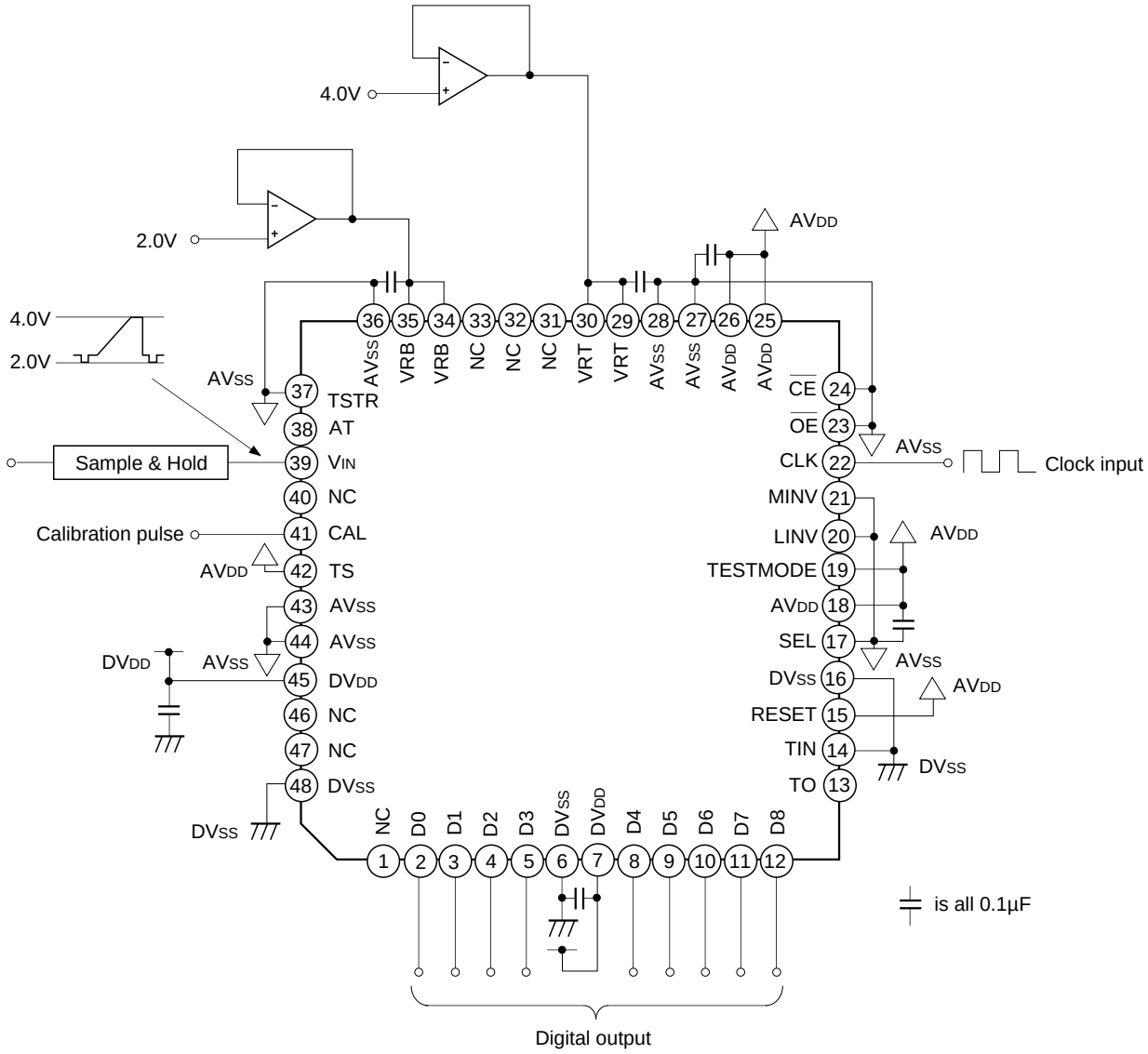
Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
SNR	SNR	F_{IN} = 100kHz		53		dB
		F_{IN} = 500kHz		53		
		F_{IN} = 1MHz		53		
		F_{IN} = 3MHz		51		
		F_{IN} = 7MHz		51		
		F_{IN} = 10MHz		49		
SFDR	SFDR	F_{IN} = 100kHz		68		dB
		F_{IN} = 500kHz		66		
		F_{IN} = 1MHz		66		
		F_{IN} = 3MHz		62		
		F_{IN} = 7MHz		56		
		F_{IN} = 10MHz		51		

Application Circuit 1. Startup calibration + internal auto calibration



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

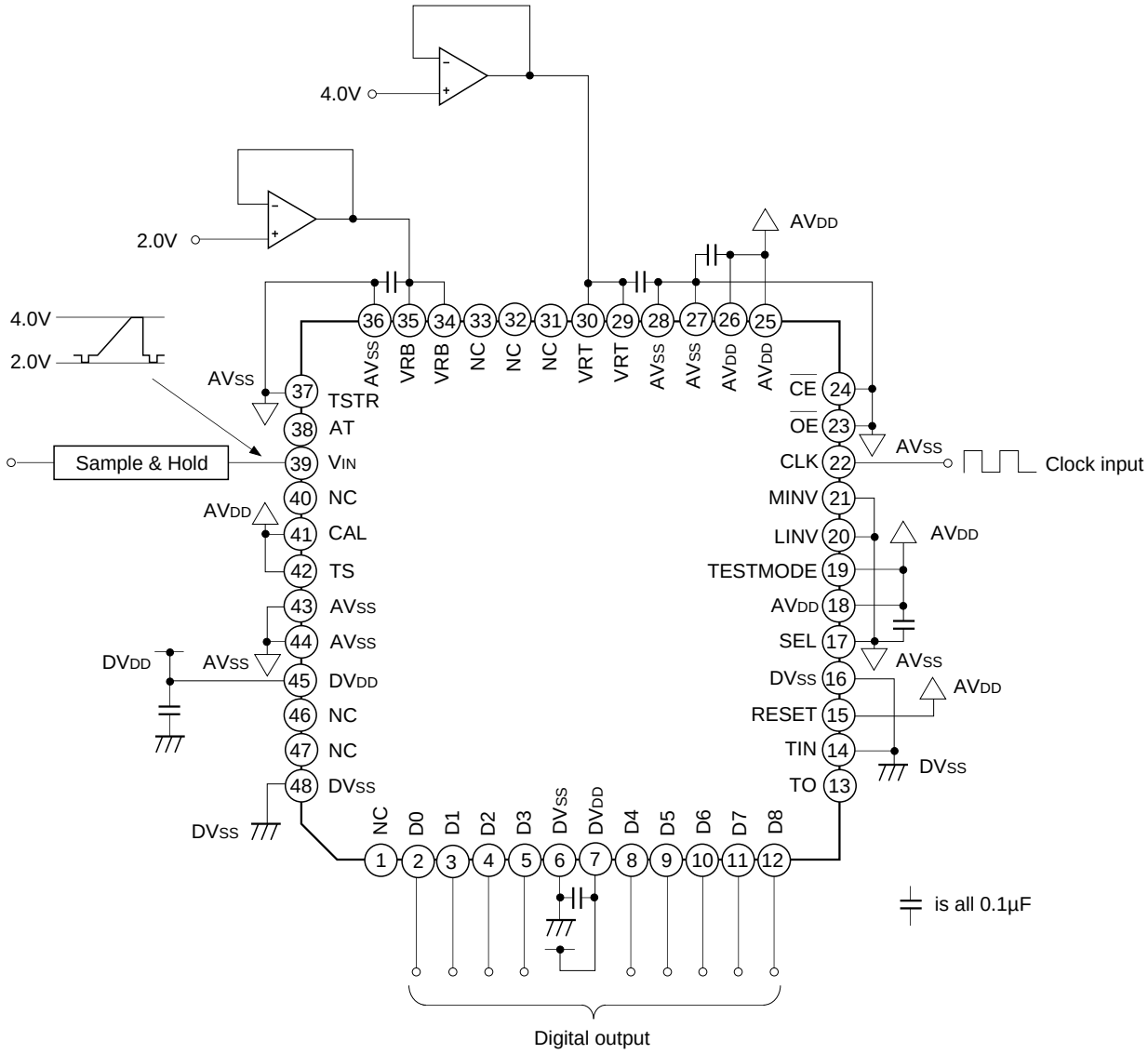
Application Circuit 2. Startup calibration + external sync calibration



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Application Circuit 3. Only startup calibration

(Less than supply voltage fluctuation range of AV_{DD} = ±100mV and reference voltage fluctuation range of |VRT – VRB| = 200mV)



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

1. Calibration Function

In order to achieve superior linearity, the CXD2312R has a built-in calibration circuit and a calibration pulse auto generation circuit which is used to execute a calibration circuit. Fig. 1 shows a block diagram of the calibration pulse generation circuit.

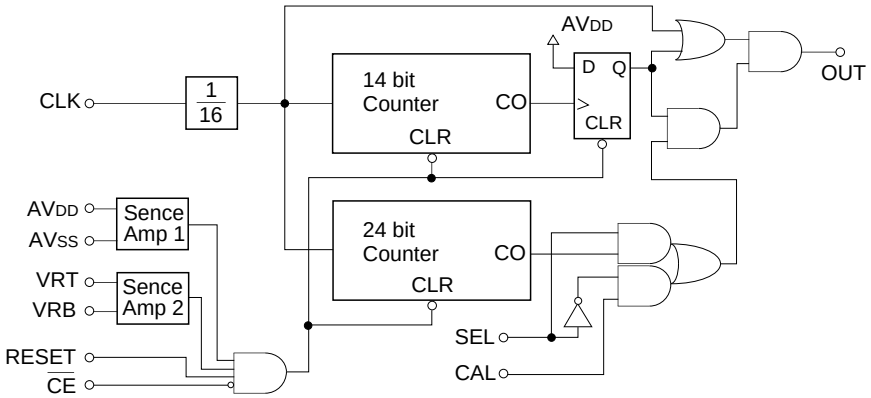
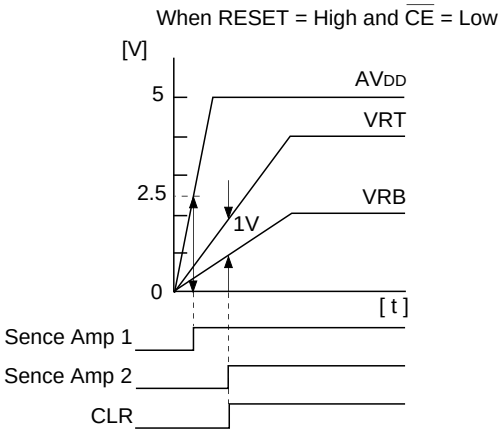


Fig. 1. Calibration Pulse Generation Circuit

(1) Startup Calibration Function

Over 600 calibration pulses are needed to complete the initial calibration process when the power is first supplied to the IC. The startup calibration function automatically generates these pulses internally and completes the initial calibration process.



The following five conditions must be satisfied to initiate the startup calibration function.

a) The voltage between AV_{DD} and AV_{SS} is approximately 2.5V or more.
b) The voltage between VRT and VRB is approximately 1V or more.
c) The RESET pin (Pin 15) must is high.
d) The CE pin (Pin 24) must is low.
e) Condition b is met after condition a.

Once all five of these conditions have been met, the calibration pulses are generated. The pulses are generated by counting 16 main clock cycles on a 14-bit counter and closing the gate when the carry-out occurs. Therefore, the time required for startup calibration after the above five conditions have been met is determined by the following formula:

$$\text{Startup calibration time} = \text{main clock cycle} \times 16 \times 16{,}384$$

For example, if the main clock frequency is 14.3MHz, the time required for startup calibration is 18ms.

(2) Auto Calibration Pulse Generation Function

After startup calibration is completed, this function periodically generates calibration pulses so that calibration can be performed constantly without any need for input of calibration pulses from an external source. This function counts 16 main clock cycles on a 24-bit counter and uses the carry-out as the calibration pulse. The cycle of the calibration pulse generated in this fashion is as follows:

$$\text{Internal calibration pulse generation cycle} = \text{main clock cycle} \times 16 \times 16{,}777{,}216$$

Therefore, if the main clock frequency is 14.3MHz, the calibration pulse cycle is approximately 19 seconds; since calibration is performed once every seven pulses, the calibration cycle is approximately 130 seconds. In order to use this function, the SEL pin (Pin 17) must be high.

Note that this function cannot be used if fixing the lower bits in the calibration operation as described below will cause problems because this function is executed asynchronously without regard to the input signals.

(3) External Calibration Pulse Input Function

If the auto calibration function cannot be used, calibration can be performed in synchronization with the input signals when a calibration pulse is input from the CAL pin (Pin 41) by setting the SEL pin (Pin 17) low.

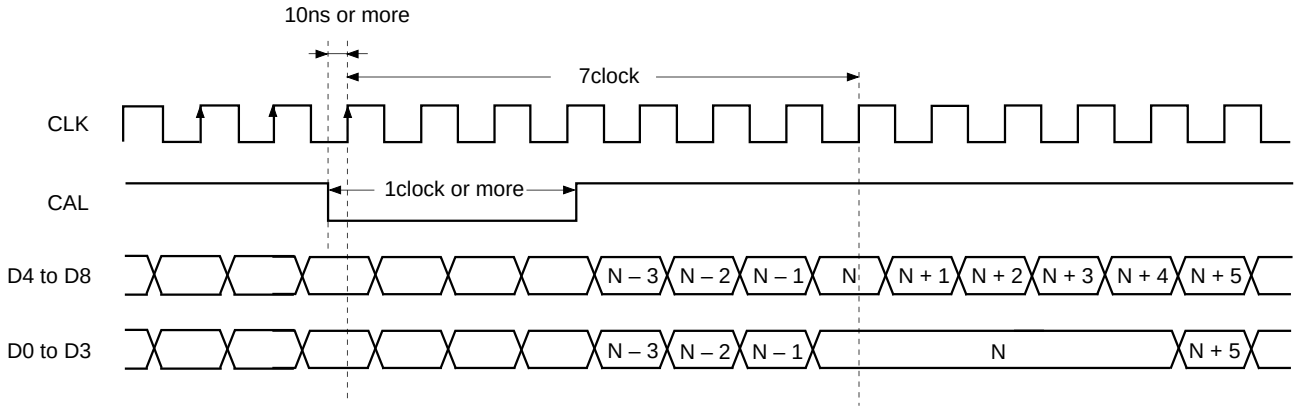
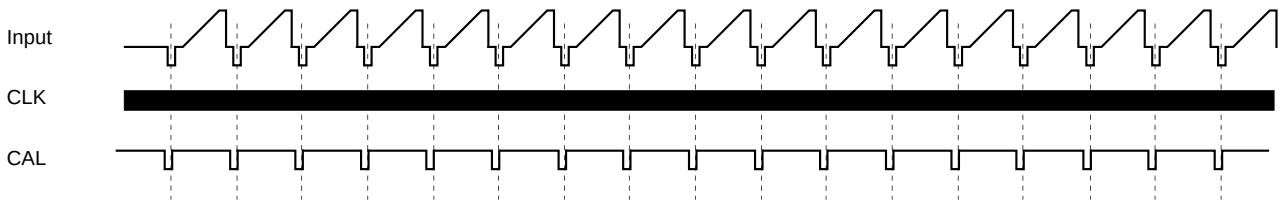


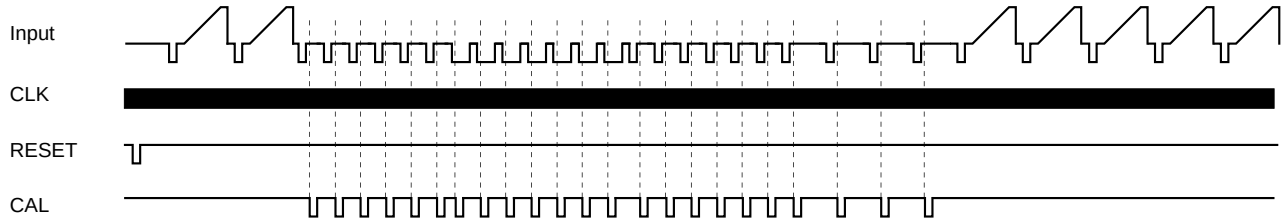
Fig. 2. Calibration Timing Chart

Calibration starts when the falling edge of the pulse input to the CAL pin (Pin 41) is detected. Because the lower comparator is occupied for four clock cycles at this point, the previous lower data is held for four clock cycles after seven clock cycles since the rising edge of the clock cycle in which the falling edge of CAL was detected. Calibration can be performed outside of video intervals by using the sync signal, etc., to input the CAL signal. An example of this is shown below.

(1) Inputting CAL every H-sync



(2) Inputting CAL every V-sync



It is also possible to use only the startup calibration function by leaving the SEL pin (Pin 17) low and fixing the CAL pin (Pin 41) either high or low. Note that this method requires restriction of the fluctuation range of the supply voltage and the reference voltage.

(4) Re-initiating the Startup Calibration Function

The startup calibration function can be re-initiated after the power and reference voltage are supplied by using the CE pin (Pin 24) and the RESET pin (Pin 15). Particularly in cases where the riseup characteristics of the power supply and the reference voltage are unstable, it is possible to initiate startup calibration properly by connecting a CR and delaying startup until after power supply riseup.

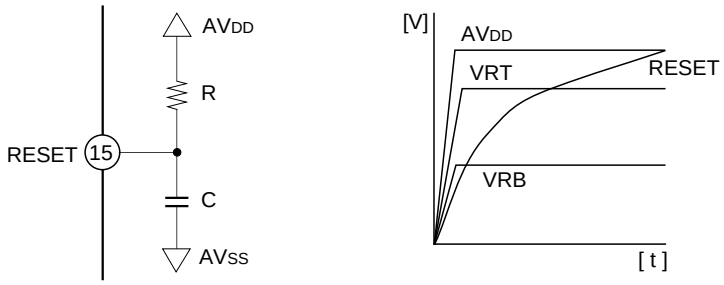


Fig. 3. Initiation of the Startup Calibration Function Using the RESET pin

2. Power supply

To prevent the influence of noise, connect the power supply to a 0.1µF by-pass capacitor as near the device as possible.

3. DV_{DD}

Either a 3.3V or 5.0V digital power supply can be used. Compared to the 5.0V power supply, the 3.3V power supply generates a decreased amount of radiation noise but offers a decreased drive capacity. These two power supplies do not virtually differ in static and dynamic characteristics. Further, the High output level rises up to DV_{DD}.

4. Reference input

The voltage to be supplied to the reference pins must be driven by a buffer having a 10mA or more drive capacity. For supplied voltage stabilization, connect the buffer to a 0.1µF by-pass capacitor as near the pins as possible.

5. Latch-up

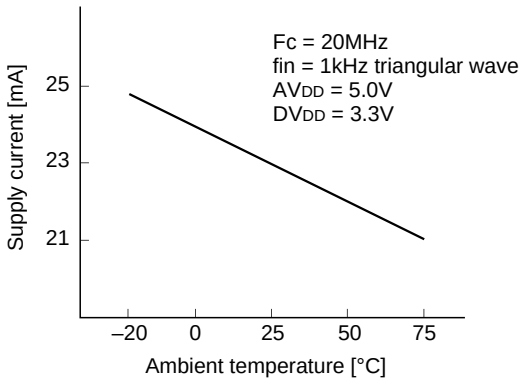
Ensure that the AV_{DD} and DV_{DD} pins share the same power supply on a board to prevent latch-up which may be caused by power ON time-lag.

6. Board

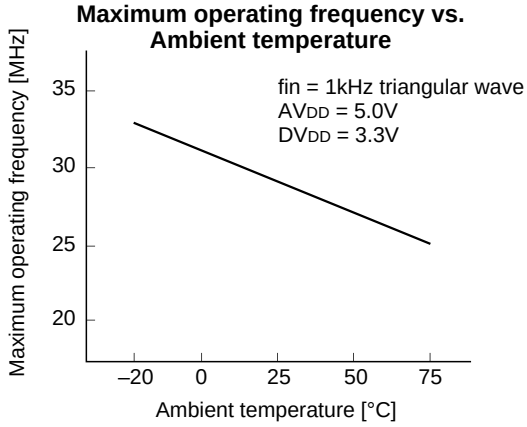
To obtain full-expected performance from this IC, be sure that the mounting board has a large ground pattern for lower impedance. It is recommended that the IC be mounted on a board without using a socket to evaluate its characteristics adequately.

Example of Representative Characteristics

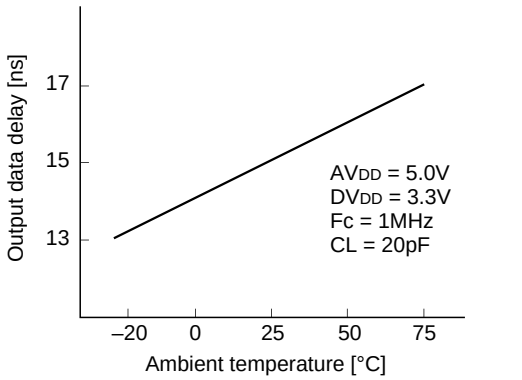
Supply current vs. Ambient temperature



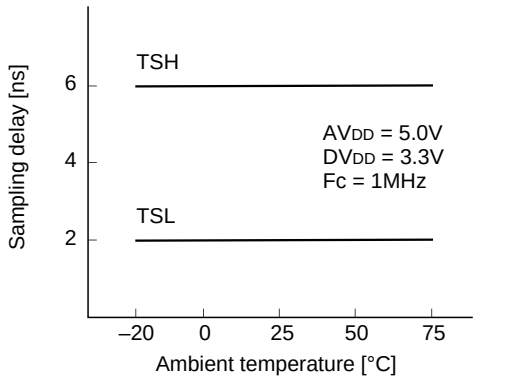
Maximum operating frequency vs. Ambient temperature



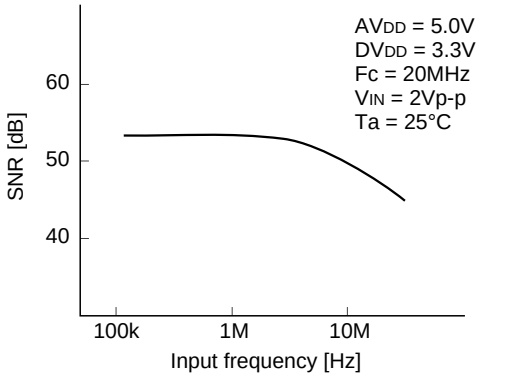
Output data delay vs Ambient temperature



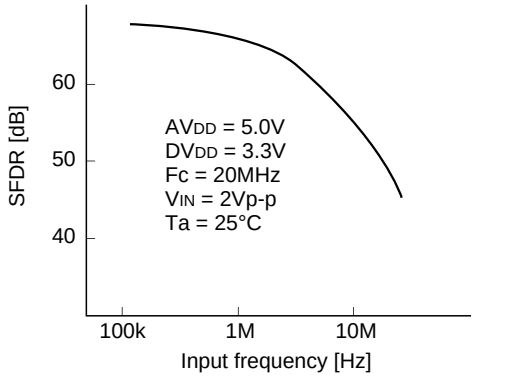
Sampling delay vs. Ambient temperature



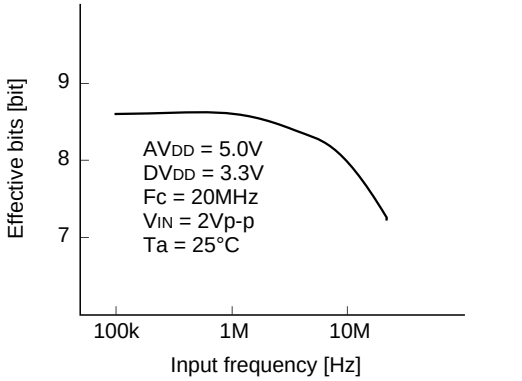
Input frequency vs. SNR



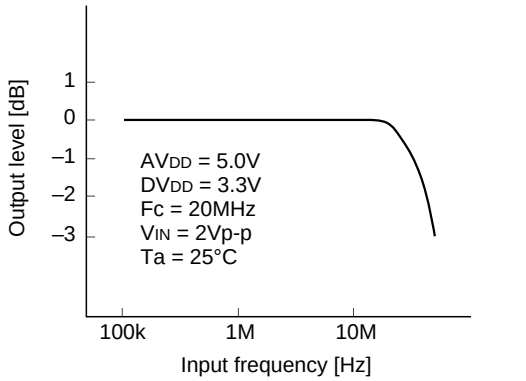
Input frequency vs. SFDR



Input frequency vs. Effective bits

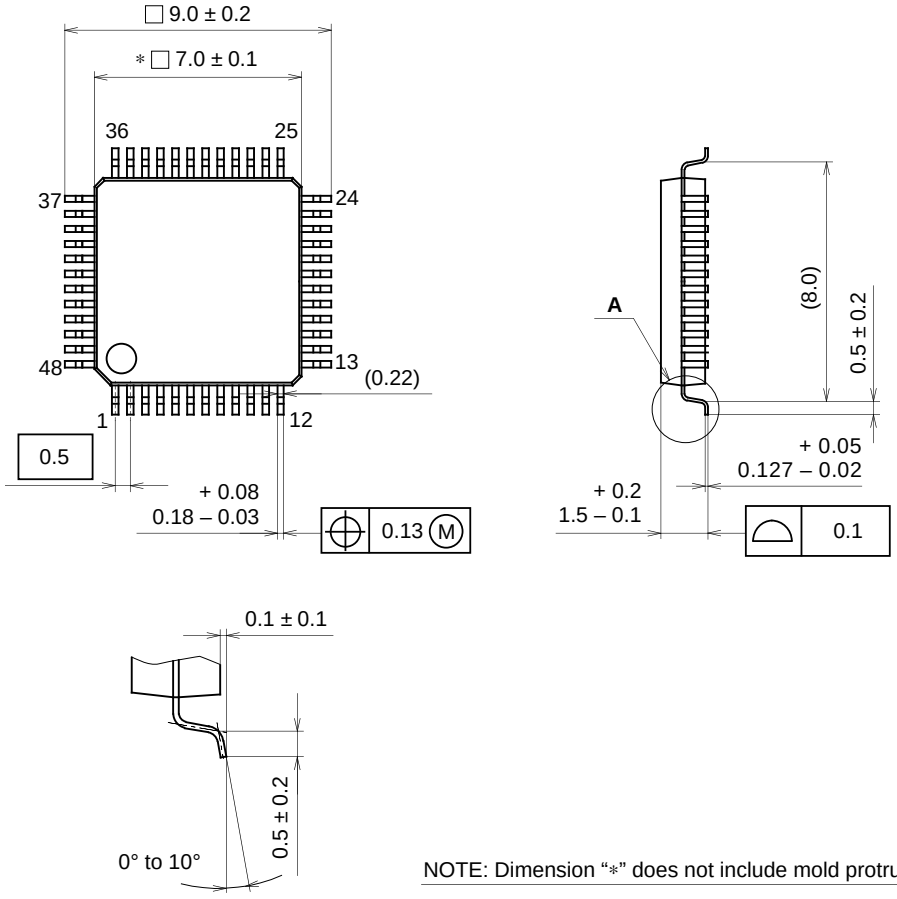


Input band



Package Outline Unit: mm

48PIN LQFP (PLASTIC)



DETAIL **A**

NOTE: Dimension "∗" does not include mold protrusion.

SONY CODE	LQFP-48P-L01
EIAJ CODE	LQFP048-P-0707
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER/PALLADIUM PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	0.2g