DATA SHEET

TDA8779H
10-bit converter interface (ADC/DAC) for quadrature transceiver

Product specification
1999 Sep 16
Supersedes data of 1999 Jan 18
File under Integrated Circuits, IC02

Philips Semiconductors

PHILIPS

10-bit converter interface (ADC/DAC) for quadrature transceiver

TDA8779H

FEATURES

- Two 10-bit ADCs with multiplexed outputs
- Two 10-bit DACs with multiplexed inputs
- Sampling rate for the ADCs and DACs up to 20 MHz
- Digital outputs (for the ADC) and inputs (for the DAC) are TTL/CMOS compatible
- Internal reference voltage regulator
- Power dissipation 520 mW
- Standby mode.

APPLICATIONS

- Wireless communication.

GENERAL DESCRIPTION

The TDA8779 contains two 10-bit high speed ADCs and two 10-bit DACs for wireless communication (for use in transceiver modules). This device converts two analog input signals (channels I and Q) and digital inputs (D0 to D9) at a maximum sampling rate of 20 MHz. The input bias voltages for the analog input voltages are provided internally at the middle code. The analog input and output voltages are AC coupled.

The data sampling is performed on the rising edge of the clock for ADCs and DACs.

All reference voltages are generated internally.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CCA1}	analog supply voltage for the ADC part		4.75	5.0	5.5	V
V_{CCD1}	digital supply voltage for the ADC part		4.75	5.0	5.5	V
V_{CCA2}	analog supply voltage for the DAC part		4.75	5.0	5.5	V
V_{CCD2}	digital supply voltage for the DAC part		4.75	5.0	5.5	V
V_{CCO}	output stage supply voltage		2.7	3.0	3.3	V
I_{CCA}	analog supply current		59	74	85	mA
I_{CCD}	digital supply current		15	23	35	mA
I_{CCO}	output stage supply current	ramp input; f_{CLK} = 20 MHz	–	7	–	mA
$f_{CLK(ADC)max}$	maximum clock frequency for the ADC part		20	–	–	MHz
INLA	integral non linearity for the ADC part	full-scale; ramp input; f_{CLK} = 20 MHz	–	±2.25	±4	LSB
DNLA	differential non linearity for the ADC part	full-scale; ramp input; f_{CLK} = 20 MHz	–	+1.55 to –0.9	+2.8 to –1.1	LSB
$f_{CLK(DAC)max}$	maximum clock frequency for the DAC part		20	–	–	MHz
INLD	integral non linearity for the DAC part	full-scale; ramp input; f_{CLK} = 20 MHz	–	±0.4	±1.25	LSB
DNLD	differential non linearity for the DAC part	full-scale; ramp input; f_{CLK} = 20 MHz	–	±0.35	±1.5	LSB
P_{tot}	total power dissipation		–	520	745	mW

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8779H	QFP44	plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 × 10 × 1.75 mm	SOT307-2

BLOCK DIAGRAM

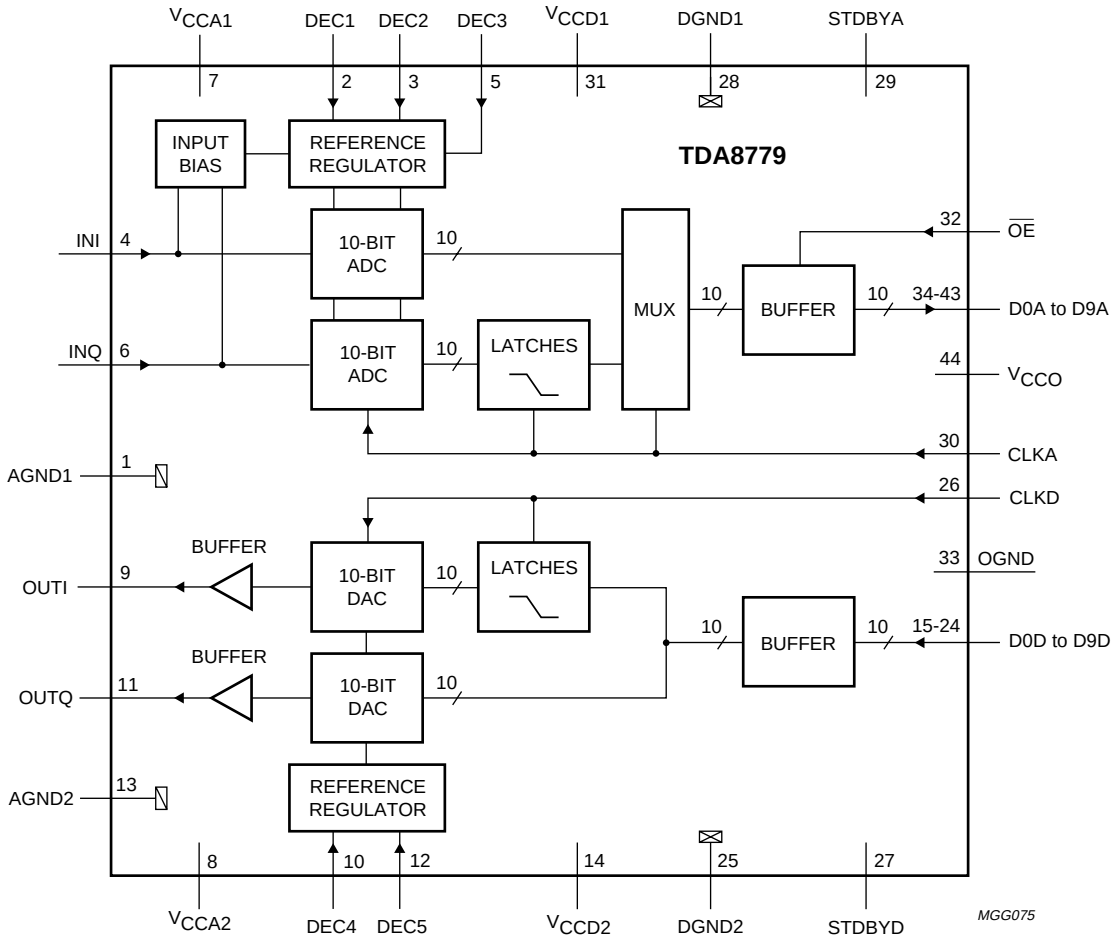


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
AGND1	1	analog ground 1
DEC1	2	decoupling input 1
DEC2	3	decoupling input 2
INI	4	I channel ADC input
DEC3	5	decoupling input 3
INQ	6	Q channel ADC input
V_{CCA1}	7	analog supply voltage 1 for ADC part (5 V)
V_{CCA2}	8	analog supply voltage 2 for DAC part (5 V)
OUTI	9	I channel DAC analog output
DEC4	10	decoupling input 4
OUTQ	11	Q channel DAC analog output
DEC5	12	decoupling input 5
AGND2	13	analog ground 2
V_{CCD2}	14	digital supply voltage 2 for DAC part (5 V)
D0D	15	multiplexed input for the DACs; bit 0
D1D	16	multiplexed input for the DACs; bit 1
D2D	17	multiplexed input for the DACs; bit 2
D3D	18	multiplexed input for the DACs; bit 3
D4D	19	multiplexed input for the DACs; bit 4
D5D	20	multiplexed input for the DACs; bit 5
D6D	21	multiplexed input for the DACs; bit 6
D7D	22	multiplexed input for the DACs; bit 7
D8D	23	multiplexed input for the DACs; bit 8
D9D	24	multiplexed input for the DACs; bit 9
DGND2	25	digital ground 2
CLKD	26	transmission block clock
STDBYD	27	power standby for the DAC part (active HIGH)
DGND1	28	digital ground 1
STDBYA	29	power standby for the ADC part (active HIGH)
CLKA	30	reception block clock
V_{CCD1}	31	digital supply voltage 1 for ADC part (5 V)
$\overline{OE}$	32	ADCs digital output enable (3-state output); (active LOW)
OGND	33	input/output ground
D0A	34	I and Q digital outputs; bit 0
D1A	35	I and Q digital outputs; bit 1
D2A	36	I and Q digital outputs; bit 2
D3A	37	I and Q digital outputs; bit 3
D4A	38	I and Q digital outputs; bit 4
D5A	39	I and Q digital outputs; bit 5
D6A	40	I and Q digital outputs; bit 6

SYMBOL	PIN	DESCRIPTION
D7A	41	I and Q digital outputs; bit 7
D8A	42	I and Q digital outputs; bit 8
D9A	43	I and Q digital outputs; bit 9
V_{CCO}	44	output supply voltage (2.7 to 3.3 V)

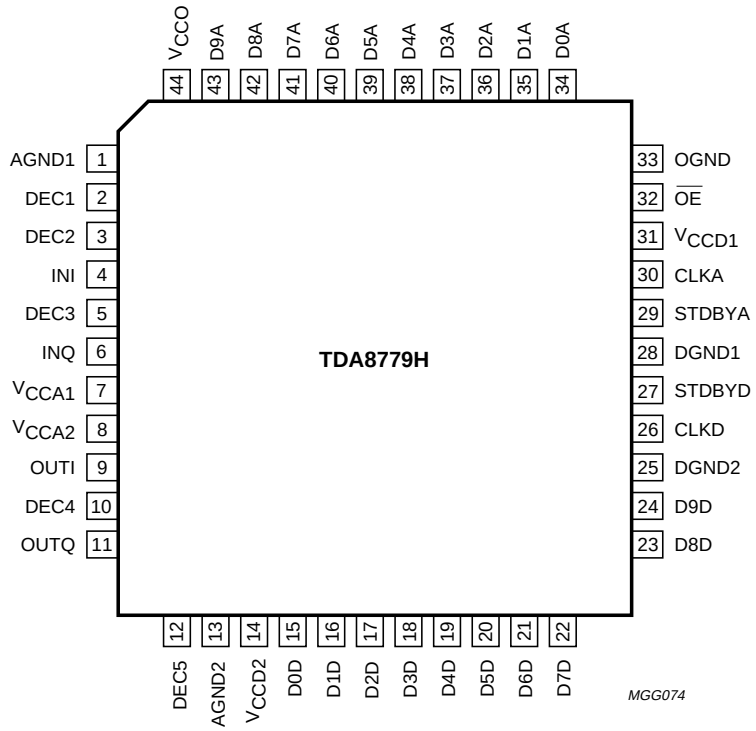


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CCA1}	analog supply voltage for the ADC part		–0.3	+6.0	V
V_{CCA2}	analog supply voltage for the DAC part		–0.3	+6.0	V
V_{CCD1}	digital supply voltage for the ADC part		–0.3	+6.0	V
V_{CCD2}	digital supply voltage for the DAC part		–0.3	+6.0	V
V_{CCO}	output stage supply voltage		–0.3	+6.0	V
ΔV_{CC}	voltage difference between				
	$V_{CCA} - V_{CCD}$		–1.0	+1.0	V
	$V_{CCA} - V_{CCO}$		–1.0	+4.0	V
	$V_{CCD} - V_{CCO}$		–1.0	+4.0	V
I_o	output current		–	10	mA
V_i	input voltage	with respect to AGND	–0.3	+6.0	V
$V_{clk(p-p)}$	AC input switching voltage (peak-to-peak value)	with respect to DGND	–	V_{CCD}	V
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	ambient temperature		–20	+75	°C
T_j	junction temperature		–	150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	75	K/W

CHARACTERISTICS

$V_{CCA} = V_7$ and V_8 to V_1 and V_{13} = 4.75 to 5.5 V; $V_{CCD} = V_{31}$ and V_{14} to V_{28} and V_{25} = 4.75 to 5.5 V; $V_{CCO} = V_{44}$ to V_{33} = 2.7 to 3.3 V; AGND1, AGND2, OGND, DGND1 and DGND2 are shorted together; T_{amb} = –20 to +75 °C; measured typically at $V_{CCA} = V_{CCD}$ = 5 V and V_{CCO} = 3.0 V; C_L = 15 pF; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{CCA1}	analog supply voltage for the ADC part		4.75	5.0	5.5	V
V_{CCD1}	digital supply voltage for the ADC part		4.75	5.0	5.5	V
V_{CCA2}	analog supply voltage for the DAC part		4.75	5.0	5.5	V
V_{CCD2}	digital supply voltage for the DAC part		4.75	5.0	5.5	V
V_{CCO}	output stage supply voltage		2.7	3.0	3.3	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
ΔV_{CC}	voltage difference between	T_{amb} = 25 °C				
	$V_{CCA} - V_{CCD}$		–0.2	–	+0.2	V
	$V_{CCA} - V_{CCO}$		0	–	2.8	V
	$V_{CCD} - V_{CCO}$		0	–	2.8	V
I_{CCA}	analog supply current		59	74	85	mA
I_{CCD}	digital supply current		15	23	35	mA
I_{CCO}	output stage supply current	ramp input; f_{CLK} = 20 MHz	–	7	15	mA
$I_{CCA1(stb)}$	analog standby current for the ADC part		–	0.7	3	mA
$I_{CCA2(stb)}$	analog standby current for the DAC part		–	2.5	5	mA
ADC part						
CLOCK INPUT						
V_{IL}	LOW-level input voltage	T_{amb} = 25 °C	0	–	0.8	V
V_{IH}	HIGH-level input voltage	T_{amb} = 25 °C	2.0	–	V_{CCD1}	V
I_{IL}	LOW-level input current		–10	–	+10	µA
I_{IH}	HIGH-level input current		–10	–	+10	µA
DIGITAL INPUTS: PINS $\overline{OE}$ AND STDBYA						
V_{IL}	LOW-level input voltage	T_{amb} = 25 °C	0	–	0.8	V
V_{IH}	HIGH-level input voltage	T_{amb} = 25 °C	2.0	–	V_{CCD1}	V
I_{IL}	LOW-level input current		–10	–	+10	µA
I_{IH}	HIGH-level input current		–10	–	+10	µA
ANALOG INPUTS						
I_{IL}	LOW-level input current	for code 0	–	–91	–	µA
I_{IH}	HIGH-level input current	for code 1023	–	80	–	µA
$V_{i(p-p)}$	analog input voltage (peak-to-peak value)	full-scale	1.52	1.57	1.62	V
$V_{i(p-p)over}$	maximum analog input overvoltage (peak-to-peak value)	overvoltage for f_i = 4.43 MHz; T_{amb} = 25 °C	–	–	3.0	V
Z_I	input impedance		–	10	–	kΩ
C_I	input capacitance		–	3	–	pF
DIGITAL OUTPUTS: D0A TO D9A						
V_{OL}	LOW-level output voltage	I_o = 1 mA	0	–	0.5	V
V_{OH}	HIGH-level output voltage	I_o = –1 mA	V_{CCO} – 0.5	–	V_{CCO}	V
I_{oZ}	output current in 3-state mode	0.5 V < V_o < V_{CCO} – 0.5 V	–20	–	+20	µA
SWITCHING CHARACTERISTICS; T_{amb} = 25 °C (see Fig.3)						
$f_{CLK(max)}$	maximum clock frequency		20	–	–	MHz
t_{CH}	clock pulse width HIGH		20	–	–	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_{CL}	clock pulse width LOW		20	–	–	ns
t_r	clock rise time		–	4	–	ns
t_f	clock fall time		–	4	–	ns
ANALOG SIGNAL PROCESSING						
Linearity						
INLA	integral non linearity	ramp input; f_{CLK} = 20 MHz	–	±2.25	±4	LSB
DNLA	differential non linearity maximum missing codes guaranteed: 20	full-scale; ramp input; f_{CLK} = 20 MHz	–	+1.55 to –0.9	+2.8 to –1.1	LSB
Noise floor; note 1						
NF	noise floor	f_i = 4.43 MHz; 20 Msps	–55	–71	–	dB
Harmonics; note 2						
THD	total harmonic distortion	f_i = 4.43 MHz; 20 Msps	–50	–58	–	dB
Spurious free dynamic range						
SFDR	spurious free dynamic range	f_i = 4.43 MHz; 20 Msps	50	58	–	dB
Matching between the I and Q channels						
ΔV	amplitude matching	f_i = 4.43 MHz; f_{CLK} = 20 MHz; T_{amb} = 25 °C	–	0.1	6	%
Δφ	phase matching	f_i = 4.43 MHz; f_{CLK} = 20 MHz; T_{amb} = 25 °C	–	0.05	2	deg
Bandwidth						
B	bandwidth (maximum attenuation of –0.3 dB)	full-scale sine wave; T_{amb} = 25 °C	30	–	–	MHz
		50% full-scale sine wave; T_{amb} = 25 °C	30	–	–	MHz
TIMING (THE OUTPUT DATA IS AVAILABLE AFTER THE MAXIMUM DELAY TIME t_d); C_L = 15 pF; T_{amb} = 25 °C (see Fig.3)						
t_{ds}	sampling delay time		–	–	11	ns
t_h	output hold time		5	–	–	ns
t_d	output delay time	V_{CCO} = 3.3 V	–	12	–	ns
		V_{CCO} = 2.7 V	–	13	–	ns
3-STATE OUTPUT DELAY TIMES; T_{amb} = 25 °C (see Fig.4)						
t_{dZH}	output delay enable HIGH		–	10	–	ns
t_{dZL}	output delay enable LOW		–	7.7	–	ns
t_{dHZ}	output delay disable HIGH		–	15.5	–	ns
t_{dLZ}	output delay disable LOW		–	14.9	–	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
STANDBY MODE OUTPUT DELAY TIMES; STDBYA; T_{amb} = 25 °C						
$t_{d(stb)LH}$	standby delay (LOW-to-HIGH transition)		–	–	100	µs
$t_{d(stb)HL}$	start-up delay (HIGH-to-LOW transition)		–	–	100	µs
CROSSTALK ON THE ADC						
α_{ct}	crosstalk on the ADC	$f_{CLK(DAC)}$ = 16.384 MHz; $f_{CLK(ADC)}$ = 8.192 MHz; T_{amb} = 25 °C; both DACs switching between input codes 0 and 1023; one ADC 1 V (p-p) sine wave at 4 MHz and the other ADC set at the middle code	–50	–55	–	dB
DAC part						
DIGITAL INPUTS: D0D TO D9D AND CLKD						
V_{IL}	LOW-level input voltage	T_{amb} = 25 °C	0	–	0.8	V
V_{IH}	HIGH-level input voltage	T_{amb} = 25 °C	2.0	–	V_{CCD2}	V
I_{IL}	LOW-level input current		–200	–	0	µA
I_{IH}	HIGH-level input current		–10	–	+10	µA
DIGITAL INPUT; STDBYD						
V_{IL}	LOW-level input voltage	T_{amb} = 25 °C	0	–	0.8	V
V_{IH}	HIGH-level input voltage	T_{amb} = 25 °C	2.0	–	V_{CCD2}	V
I_{IL}	LOW-level input current		–10	–	+10	µA
I_{IH}	HIGH-level input current		–10	–	+10	µA
TIMING; T_{amb} = 25 °C (see Fig.5)						
$f_{CLK(max)}$	maximum clock frequency		20	–	–	MHz
t_{CH}	clock pulse width HIGH		20	–	–	ns
t_{CL}	clock pulse width LOW		20	–	–	ns
t_r	clock rise time		–	4	–	ns
t_f	clock fall time		–	4	–	ns
t_s	input data set-up time		11	–	–	ns
t_h	input data hold time		0	–	–	ns
ANALOG OUTPUTS; note 3						
$V_{o(p-p)}$	output voltage (peak-to-peak value)	full-scale	0.9	1	1.1	V
Z_{oL}	output load impedance	see Fig.6	–	15	–	pF
			–	0.3	–	kΩ

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
TRANSFER FUNCTION						
INLD	integral non linearity	ramp input; f_{CLK} = 20 MHz	–	±0.4	±1.25	LSB
DNLD	differential non linearity	ramp input; f_{CLK} = 20 MHz	–	±0.35	±1.5	LSB
t_{st}	settling time	10% to 90% full-scale; T_{amb} = 25 °C	–	8.0	–	ns
		10% to 90% for 10% full-scale; T_{amb} = 25 °C	–	7	–	ns
MATCHING BETWEEN CHANNEL I AND Q						
ΔV	amplitude matching	f_o = 4.43 MHz; f_{CLK} = 20 MHz; T_{amb} = 25 °C	–	0.2	6	%
$\Delta\varphi$	phase matching	f_o = 4.43 MHz; f_{CLK} = 20 MHz; T_{amb} = 25 °C	–	–	2	deg
DYNAMIC RANGE; note 1						
NF	noise floor	f_o = 4.43 MHz; f_{CLK} = 20 MHz	–56	–61	–	dB
SPURIOUS FREE DYNAMIC RANGE						
SFDR	spurious free dynamic range	f_o = 4.43 MHz; f_{CLK} = 20 MHz	–	55	–	dB
STANDBY MODE OUTPUT DELAY; STDBYD; T_{amb} = 25 °C						
$t_{d(stb)LH}$	standby delay (LOW-to-HIGH transition)		–	–	100	µs
$t_{d(stb)HL}$	start-up delay (HIGH-to-LOW transition)		–	–	100	µs
CROSSTALK ON THE DAC						
α_{ct}	crosstalk on the DAC	$f_{CLK(DAC)}$ = 16.384 MHz; $f_{CLK(ADC)}$ = 8.192 MHz; T_{amb} = 25 °C; one DAC switching between input codes 0 and 1023 the other DAC set at the middle code; both ADCs 1 V (p-p) sine wave at 4 MHz; incoherent	–60	–75	–	dB

Notes

1. The noise floor is the maximum value of the output spectrum without taking into account fundamental and harmonics of the input signal up to the 6th harmonic.
2. Harmonics are obtained via a Fast Fourier Transformer (FFT) treatment taking 8k acquisition points per period.
3. It is recommended that the DAC output voltage is AC coupled in order to achieve optimum performance.

Table 1 Output coding and input voltage (typical value, with respect to AGND)

STEP	$V_i - V_{512}$ (V)	BINARY OUTPUT BITS									
		D9A	D8A	D7A	D6A	D5A	D4A	D3A	D2A	D1A	D0A
underflow	<–0.75	0	0	0	0	0	0	0	0	0	0
0	–0.75	0	0	0	0	0	0	0	0	0	0
...	...	...	...	...	...	...	...	...	...	...	...
512	0	1	0	0	0	0	0	0	0	0	0
...	...	...	...	...	...	...	...	...	...	...	...
1023	0.75	1	1	1	1	1	1	1	1	1	0
overflow	>0.75	1	1	1	1	1	1	1	1	1	1

Table 2 Input coding and output voltage (typical value, with respect to DGND)

STEP	BINARY INPUT BITS										$V_o - V_{512}$ (V)
	D9D	D8D	D7D	D6D	D5D	D4D	D3D	D2D	D1D	D0D	
0	0	0	0	0	0	0	0	0	0	0	–0.5
...	...	...	...	...	...	...	...	...	...	...	...
512	1	0	0	0	0	0	0	0	0	0	0
...	...	...	...	...	...	...	...	...	...	...	...
1023	1	1	1	1	1	1	1	1	1	0	0.5

Table 3 Mode selection

$\overline{OE}$	D0A TO D9A
1	high impedance
0	active; binary

Table 4 Standby selection (ADC part)

STDBYA	D0 TO D9	$I_{CCA} + I_{CCD}$ (typ.)
1	–	5 mA
0	ADC active	64 mA

Table 5 Standby selection (DAC part)

STDBYD	OUTI AND OUTQ	$I_{CCA} + I_{CCD}$ (typ.)
1	–	5 mA
0	DAC active	38 mA

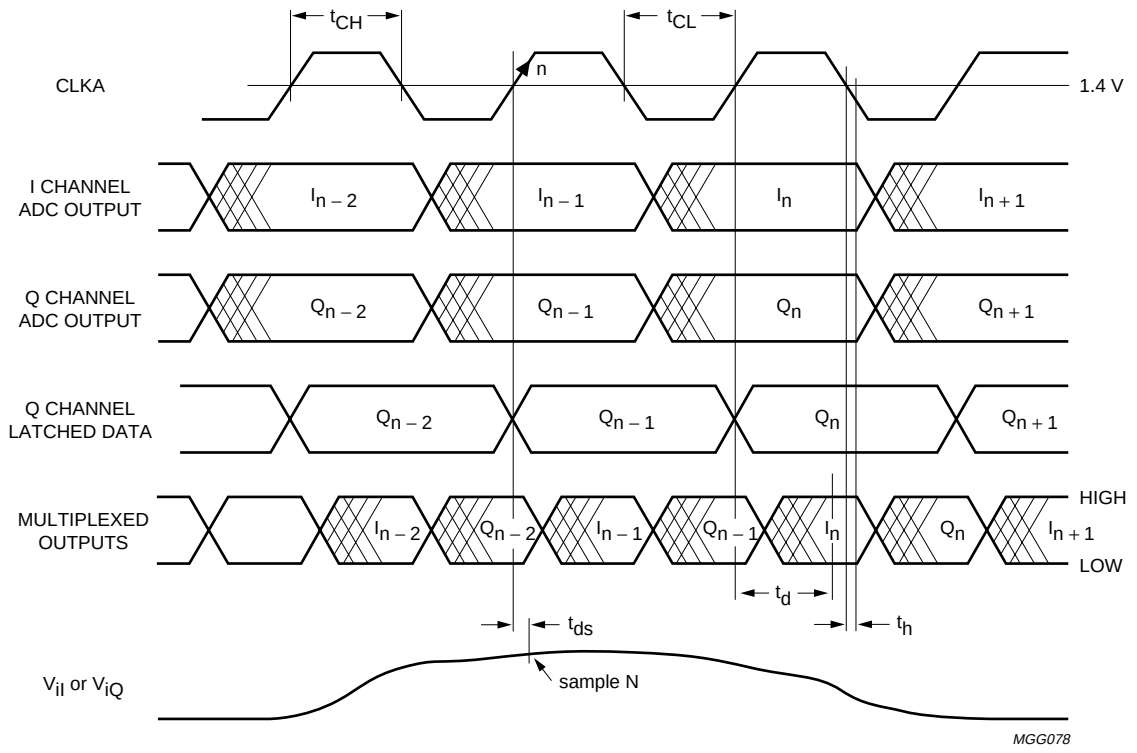
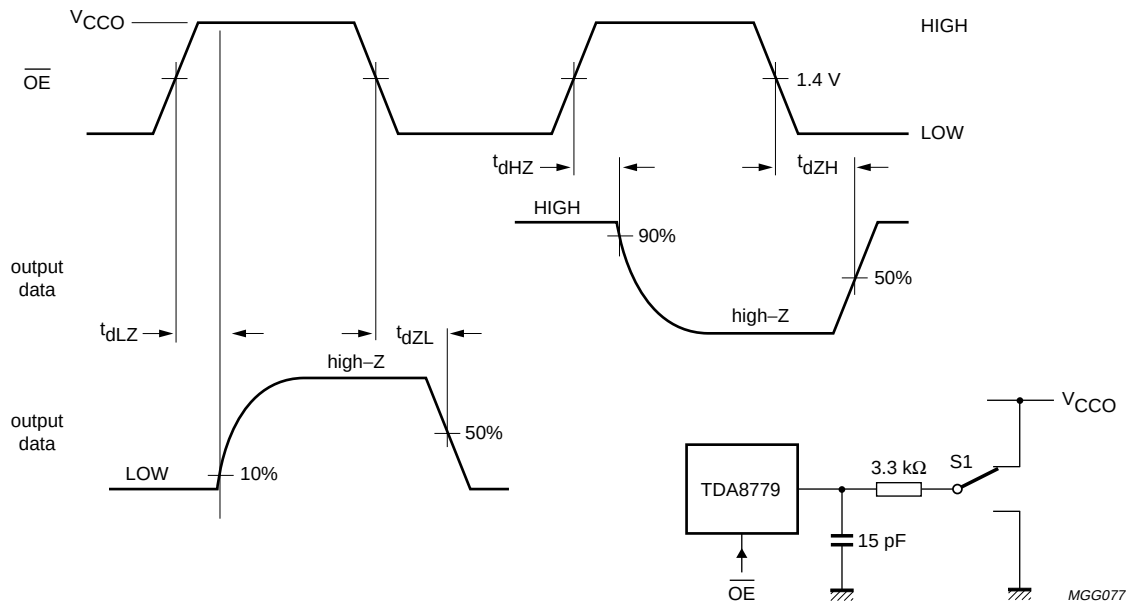


Fig.3 Timing diagram for the ADC.



$f_{\overline{OE}}$ = 100 kHz.

Fig.4 Timing diagram and test conditions of the 3-state output delay time.

Table 6 Test conditions for Fig.4

TEST	SWITCH S1
t_{dLZ}	V_{CCO}
t_{dZL}	V_{CCO}
t_{dHZ}	OGND
t_{dZH}	OGND

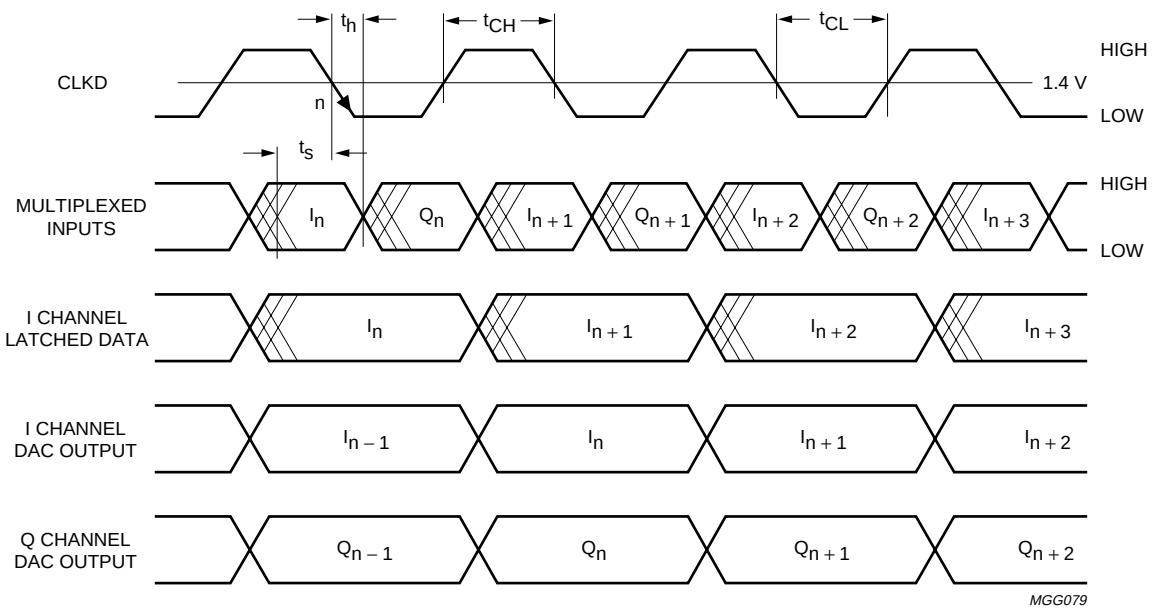


Fig.5 DACs multiplexed inputs timing diagram.

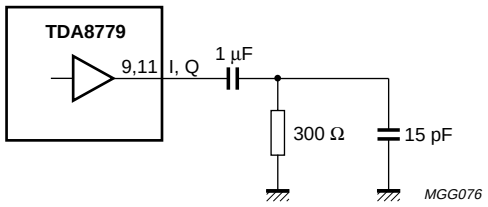


Fig.6 Equivalent DACs output load.

APPLICATION INFORMATION

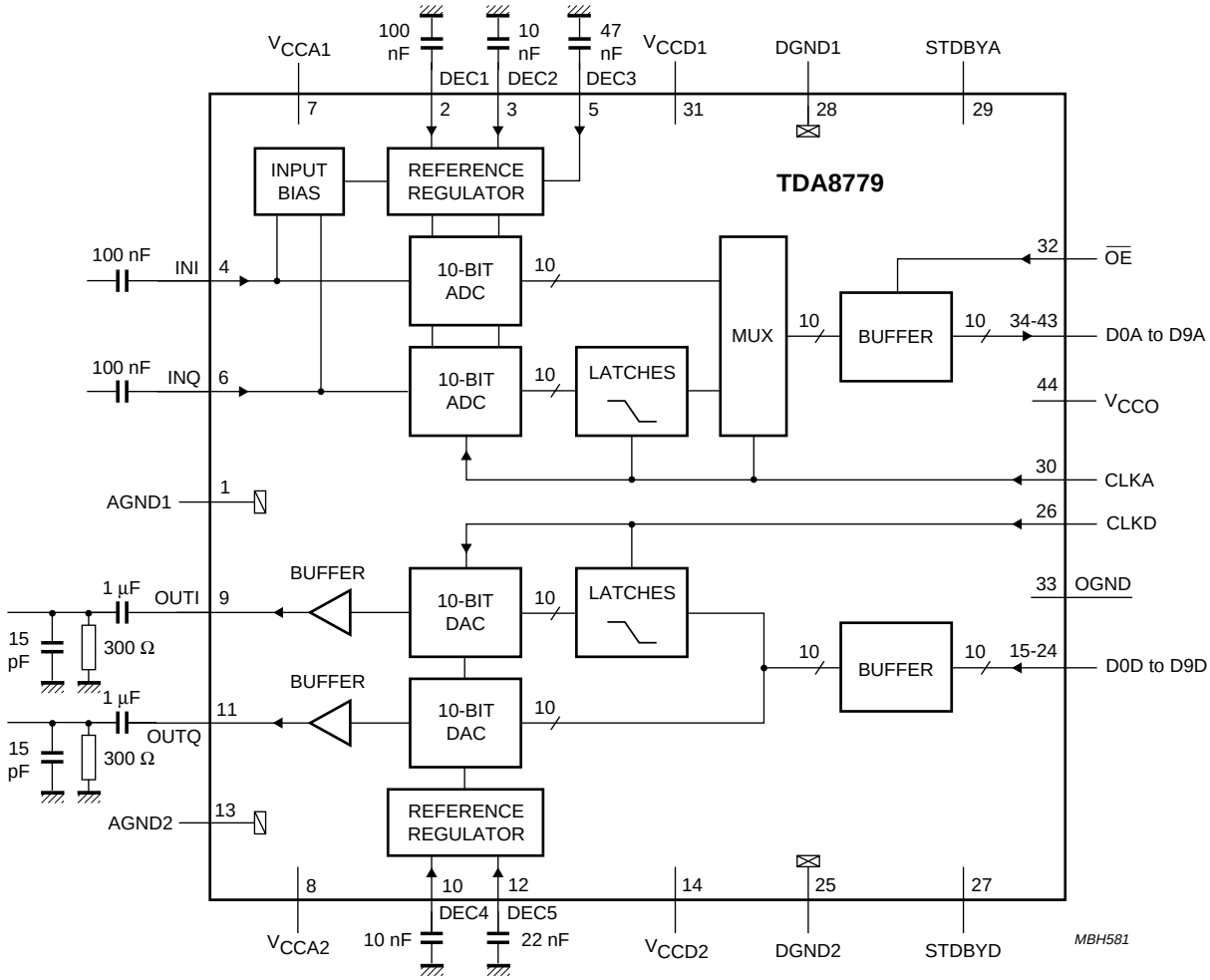
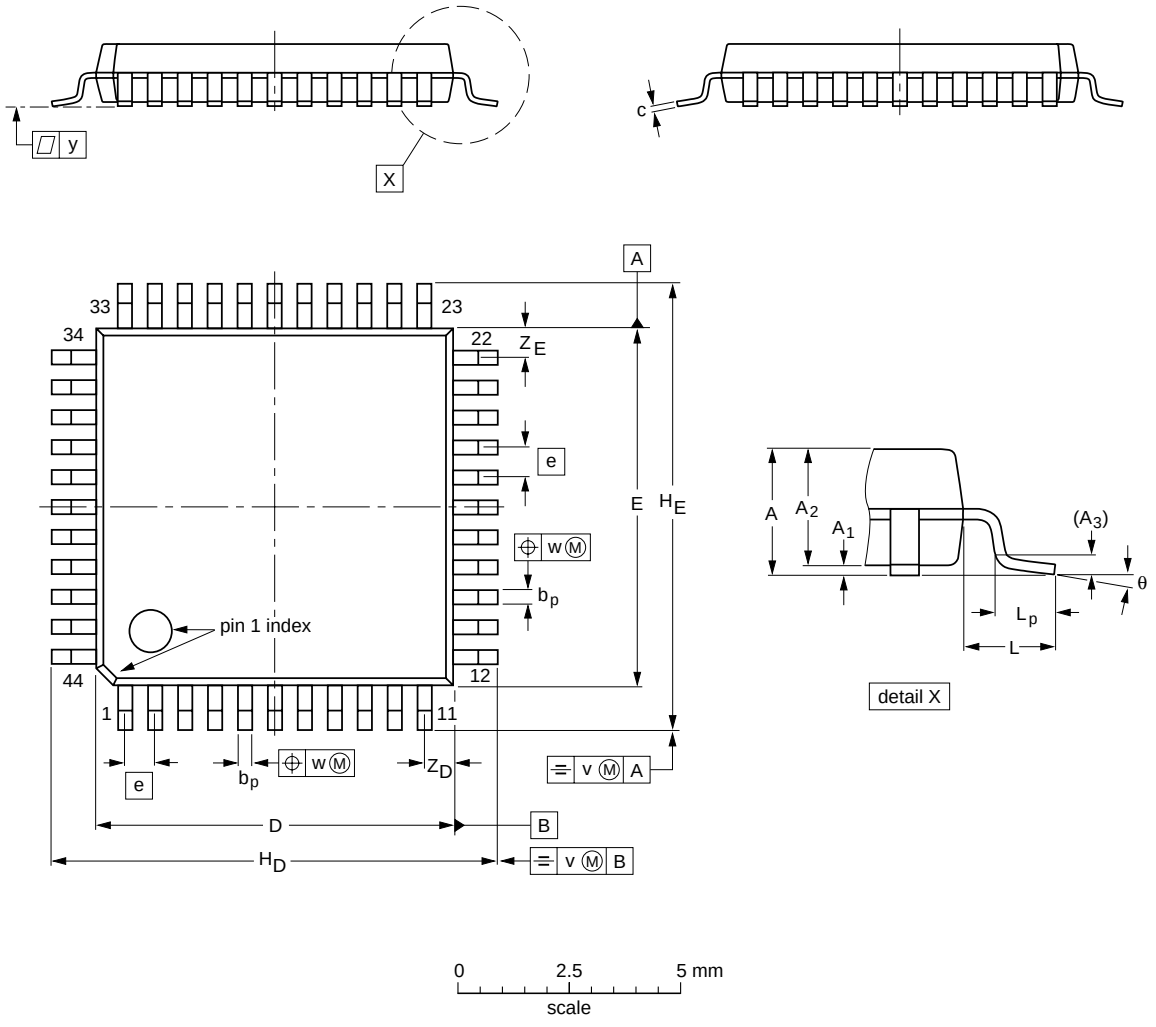


Fig.7 Application diagram.

PACKAGE OUTLINE

QFP44: plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 x 10 x 1.75 mm **SOT307-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	2.10	0.25 0.05	1.85 1.65	0.25	0.40 0.20	0.25 0.14	10.1 9.9	10.1 9.9	0.8	12.9 12.3	12.9 12.3	1.3	0.95 0.55	0.15	0.15	0.1	1.2 0.8	1.2 0.8	10^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT307-2						~~95-02-04~~ 97-08-01

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 230 °C.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW[1]
HLQFP, HSQFP, HSOP, SMS	not suitable[2]	suitable
PLCC[3], SO	suitable	suitable
LQFP, QFP, TQFP	not recommended[3][4]	suitable
SQFP	not suitable	suitable
SSOP, TSSOP, VSO	not recommended[5]	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

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