

TA7678

LINEAR INTEGRATED CIRCUIT

VIDEO AND SOUND IF AMPLIFIER FOR MONOCHROME TV RECEIVERS

DESCRIPTION

The Contek TA7678 is a monolithic integrated circuit designed for the VIF and SIF stage in B/W television receivers. The UTC TA7678 is used for forward AGC Type.

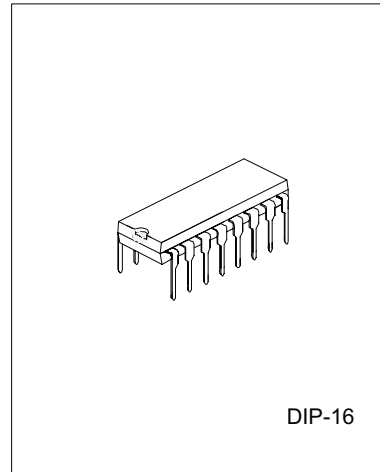
FEATURE

VIF STAGE

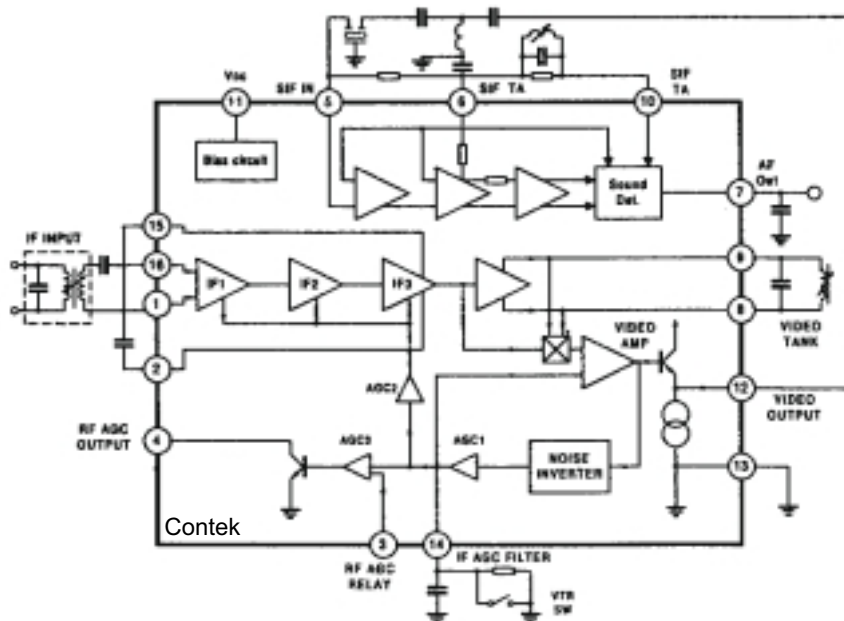
- *High gain wide band IF amplifier 50dB at 45MHz
- *Gain reduction with excellent stability: 55dB at 45MHz
- *Excellent DG/DP and S/N characteristics

SIF STAGE

- *Excellent limiter characteristics
- *Excellent AM Rejection
- *Large undistorted audio output voltage with quadrature detector



BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS(Ta=25 C)

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	Vcc	15	V
Open Loop Voltage	V4	15	V
Video DC output current (note)	V12	6	V
Operating Temperature	Topr	-20 to +65	C
Storage Temperature	Tstg	-55 to 155	C
Power dissipation	PD	1.4	W

ELECTRICAL CHARACTERISTICS(Ta=25 C,Vcc=12V,fp=45.75MHz,unless otherwise specified)

PARAMETER	TEST CIRCUIT	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Recommended Supply Voltage		Vcc		10.8	12	13.2	V
Quiescent circuit current	1	Iccq	S1:ON,S3:2,S5:2,S4:1	35	50	65	mA
Video DC output	1	V12	S1:OFF,S3:2,S5:2,S4:1	5.2	5.5	5.8	V
Terminal 5 voltage	1	V5	S1:ON,S3:2,S5:2,S4:1	3.5	4.4	5.3	V
Terminal 7 voltage	1	V5	S1:ON,S3:2,S5:2,S4:1	4.6	6.0	7.2	V
RF AGC Residual Output Voltage	1	V4(sat)	S1:OFF,S3:2,S5:2,S4:1			0.5	V
RF AGC Leak Current	1	I4(leak)	S1:OFF,S3:1,S5:2,S4:1			1	μA
Video sensitivity	2	SVI	Note 1	60	150	250	μVrms
AGC Range	2	V _{AGC(IF)}	Note 2	60	64		dB
Sync Tip Level Voltage (pin12)	2	V _{sync} (pin12)	Note 3	2.3	2.5	2.7	V
Maximum IF Input Voltage	2	V _{I(MAX)}	Note 4	100	120		mVrms
White Noise Threshold (pin12)	2	V _{WTH} (pin12)	Note 5	5.8	6.2	6.6	V
White Noise Clamp Level (pin12)	2	V _{WCL} (pin12)	Note 5	3.7	4.1	4.5	V
Black Noise Threshold (pin12)	2	V _{BTH} (pin12)	Note 5	1.4	1.6	1.8	V
Black Noise Clamp Level (pin12)	2	V _{BCL} (pin12)	Note 5	2.9	3.3	3.7	V
Video Frequency Response	3	Gv(IF)	Note 6	4.5	5.5		MHz
Suppression of carrier	4	CL	Note 7	40	50		dB
Suppression of 2 nd Carrier	4	I2nd	Note 8	40	50		dB
920kHz Beat level	4	I920	Note 9	33	38		dB
Differential Gain	5	DG	Note 10		7	10	dB
Differential Phase	5	DP	Note 10		3.5	5	C
VIF Input Impedance	6	RIN	Note 11	1.5	3.0	6.0	k
		CIN			3.0	10.0	pF
Maximum Available Current	1	I4(MAX)	Note 12	7			mA
RF AGC delay Point Range	2	Vin(delay)	Note 13	5.0	7.0	9.0	V
Video output level	2	Vo0	Note 14	2.25	2.5	2.75	V



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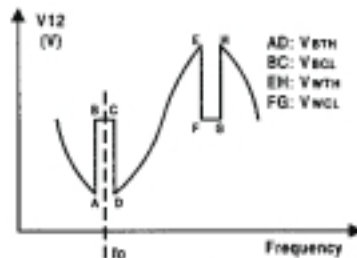
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SIF STAGE ($T_a=25^\circ\text{C}$, $V_{CC}=12\text{V}$, $f_o=45.75\text{MHz}$, unless otherwise specified)

PARAMETER	TEST CIRCUIT	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
SIF Output Voltage	3	VSO	Note 15	200	400	600	mVrms
Input limiting voltage	8	$V_i(\text{lim})$	Note 16	200	400		μVrms
AM Rejection Ratio	8	AMR	Note 17	40	45		dB
Recovered Output Voltage	8	VOD	Note 18	0.5	0.75		Vrms
Total Harmonic distortion	8	THD	Note 18		1.0	2.0	%
Maximum Audi Output Voltage	8	VOM	Note 19	4.0			Vp-p
SIF Input Impedance	7	RIN(SIF)		10	20	30	k Ω
		CIN(SIF)			3	10	pF
Audio Output Impedance	9	RO(AF)	Note 20	10	15	20	k Ω

Note:

- $V_{AGC}=11.5\text{V}$, VIF Input : 45.5MHz, 1kHz, 30 AM Modulation. Adjust VIF input V_i level so that the detected output of Pin 12 with high impedance probe will be 0.8Vp-p and measure the input Level.
- $V_{AGC}=4\text{V}$. Measure VIF input level v_i is same as note 1 $\Delta A=20\log(V_i/V_i)(\text{dB})$
- VIF input : $f=45.75\text{MHz}$ CW 15mVrms. Measure the DC level of Pin12.
- VIF Input : $f=45.75\text{MHz}$ APL 100%. 87.5% AM Modulation. Pin 14 Open
 - Adjust VIF inpt level 50mVp-p and measure the detected output level $V_o(\text{p-p})$
 - Then increase the input level so that the detected output level will be $1.1 * V_o(\text{p-p})$ and measure the input level.
- $V_{AGC}=8\text{V}$. VIF input : $f=45.75\text{MHz} \pm 10\text{MHz}$ variable or sweep 15mVrms measure DC level of Pin12.



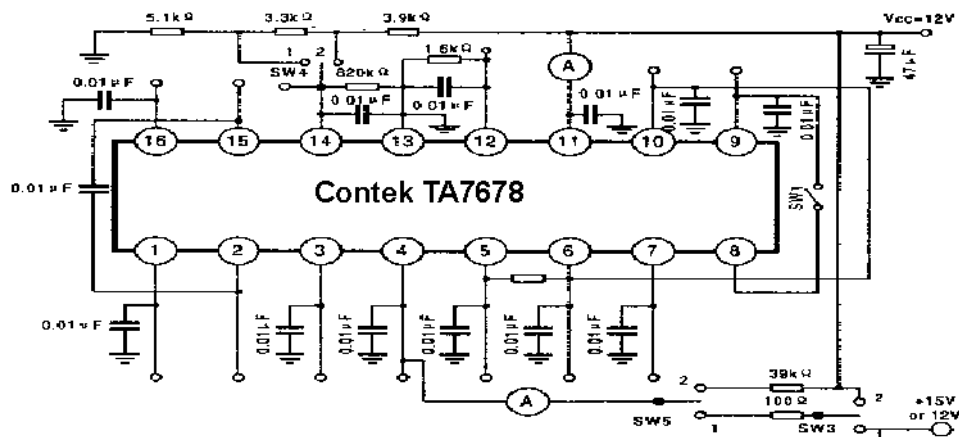
- $V_{AGC}=8\text{V}$. SG1:45.75MHz CW. SG2:45.65~27MHz variable.
 - Setting output of SG1 so that the DC level of Pin12 will be
 - Setting output of SG1(45.65MHz) so that the AC level of Pin12 will be 0.5Vp-p.
 - Decreasing frequency of SG2 until the AC level of Pin 12 will be 0.35vp-p(-3dB of 0.5Vp-p) then read $F_{SG2}=F$, $f_{BW}=45.75-F$ MHZ
- SG1:45.75MHz, 1kHz 80% AM Modulation 100mVrms. SG2 ,SG3:OFF. Setting VAGC so that the output AC level of Pin12 will be 2.7Vp-p. Measure CL of Pin12 after setting to 0% AM of SG1.
- Measure 2nd of Pin12 same as note 9.

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9. $V_{AGC}=8V$. SG1 :45.75MHz(P:picture) 100mVrms, SG2:41.25MHz(S: Sound) 32mVrms(-10dB of SG1),SG3:42.17MHz(C:Chroma) 32mVrms(-10dB of SG1)
 - 9.1. Setting V_{AGC} so that the output Pin12 will be 3.0V DC.
 - 9.2. Measure the level difference between the C-level and 920kHz.
10. $V_{AGC}=8V$. VIF Input : f=45.75MHz video signal (RAMP) 87.5% AM 100mVp-p. Setting ATT so that the SYNC TIP level of Pin12 will be 2.5VDC measure DP and DG.
11. $V_{AGC}=5V$. f=45.75MHz. Measure RIN and CIN.
12. S1=ON, S3=2,S5=1,S4=2
13. Pin 14 open. VIF Input : 45.75MHz CW 20mVrms.
 - 13.1. Adjust the voltag of Pin 3 so that the voltage of Pin4 will be 6.0V DC.
 - 13.2. Measure the Pin 3.
14. Pin 14 open. VIF Input: 45.75MHz 100% APL 87.5% AM Modulation signal amplitude 50mVp-p measure the detected output voltage (white peak to SYNC TIP)
15. PIN14: Op en. SG1 :45.75MHz CW 100mvrms. SG2 :41.25MHz CW 25mVrms. Measre SIF(4.5MHz) output voltage at Pin12.
16. SIF input: f=4.5MHz FM fMOD=400Hzm $\Delta f=+-25kHz$
 - 16.1. Adjust SIF input level 100mVp-p and measure the detected output level V_{os} .
 - 16.2. Then decrease the i nput level so that the detected output level will be 3dB down of V_{os} and measure the input level.
17. SIF input: f=4.5MHz, FM fMOD=400Hz $\Delta f=+-25kHz$. AM 30%,input level $V_{ins}=80dB\mu$.
18. SIF input: f=4.5MHz, fM fMOD=400Hz $\Delta f=+-25kHz$. Input level $V_{ins}=80dB\mu$
19. SIF input: f=4.4~4.6MHz variable or sweep measure the outjput DC voltage change.
20. SIF input : f=4.5MHz, FM FMOD=400Hz $\Delta f=+-25kHz$, input level $V_{ins}=80dB\mu$.
 - 20.1. Measure the detected output voltagae v_{OA} with $R_x=$.
 - 20.2. Then, adjust R_x so that the d etected output voltage will be $v_{OA}/2$ and measure R_x .

1. DC TEST CIRCUIT



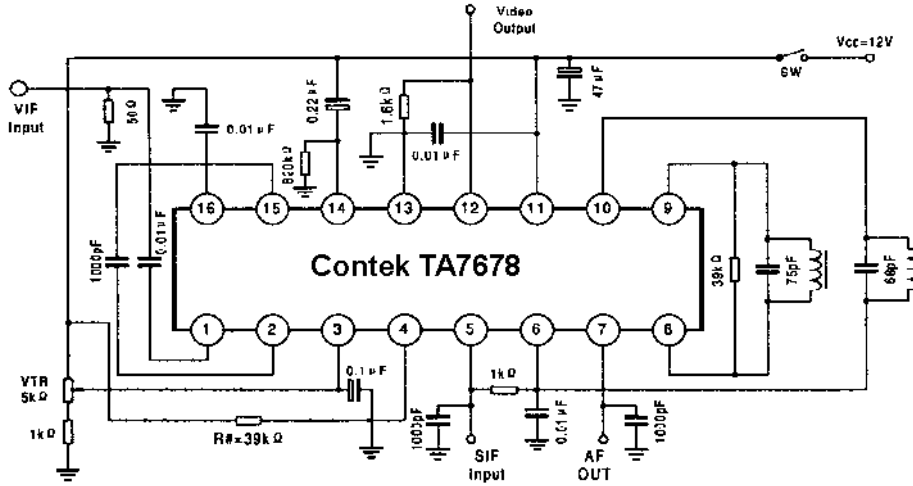
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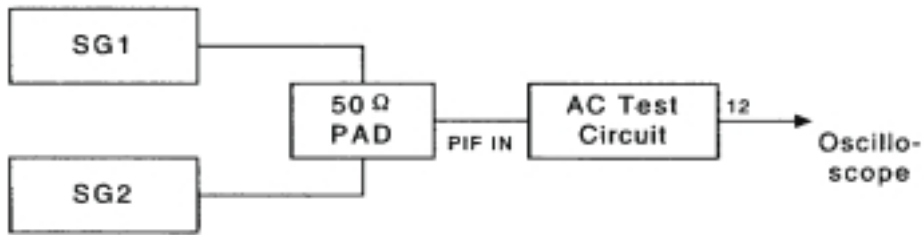
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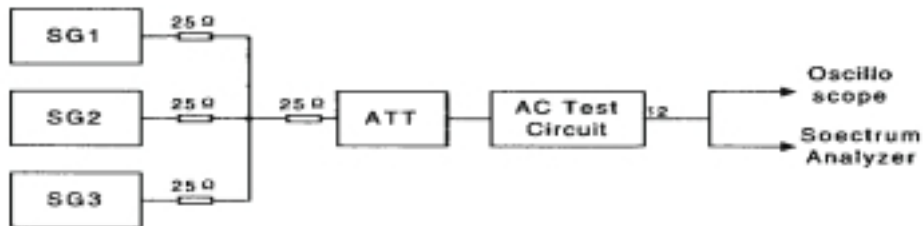
2. AC TESTS CIRCUIT



3. VIDEO FREQUENCY RESPONSE & SIF OUTPUT VOLTAGE TEST CIRCUIT



4. INTER MODULATION TEST CIRCUIT



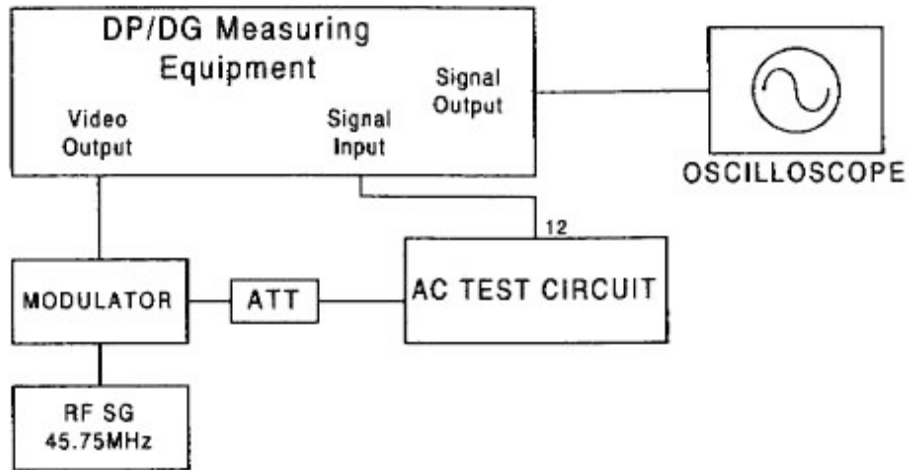
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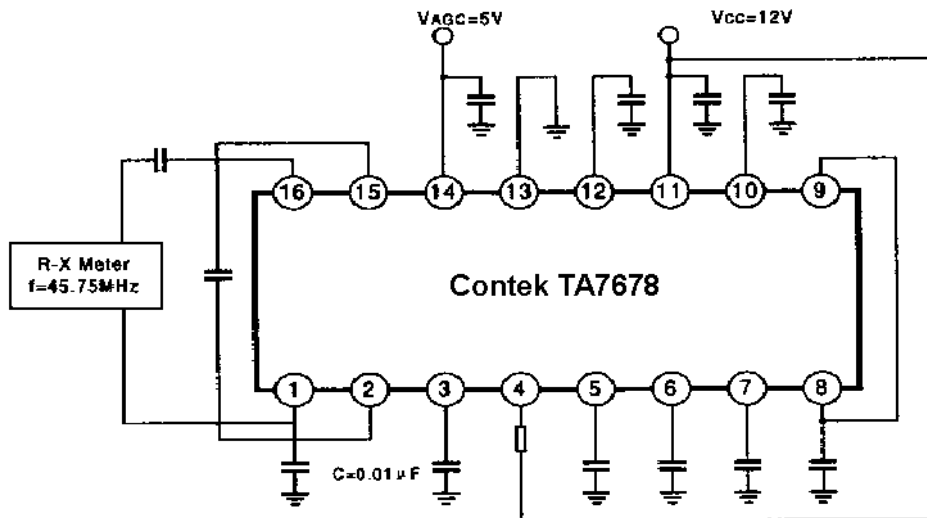
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5. DG,DP TEST CIRCUIT



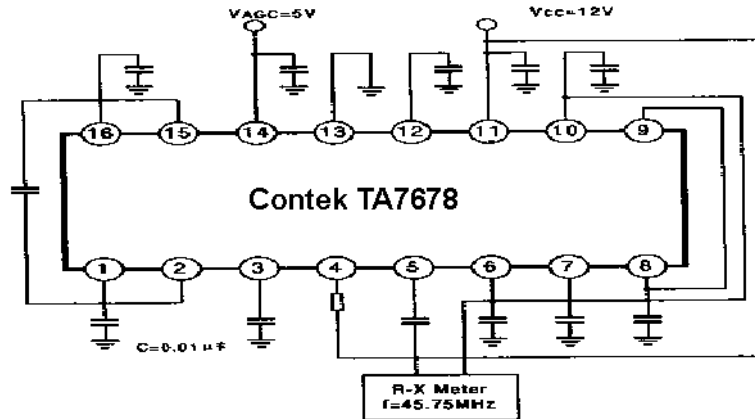
5. INPUT IMPEDANCE TEST CIRCUIT



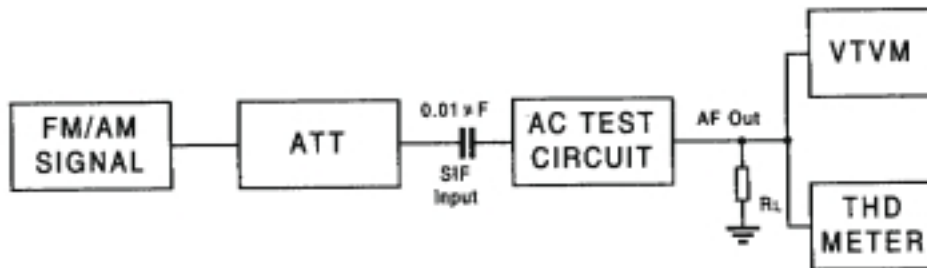
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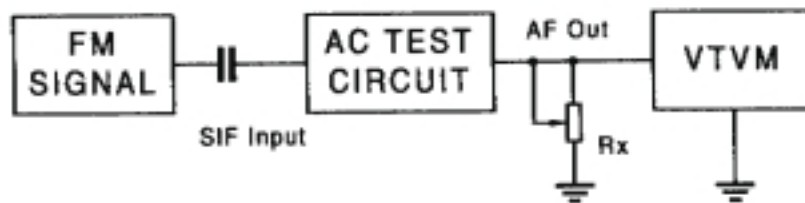
7. SIF INPUT IMPEDANCE TEST CIRCUIT



8. $V_{IN(LIM)}$, AMR, V_{OD} , THD, V_{OM} TEST CIRCUIT



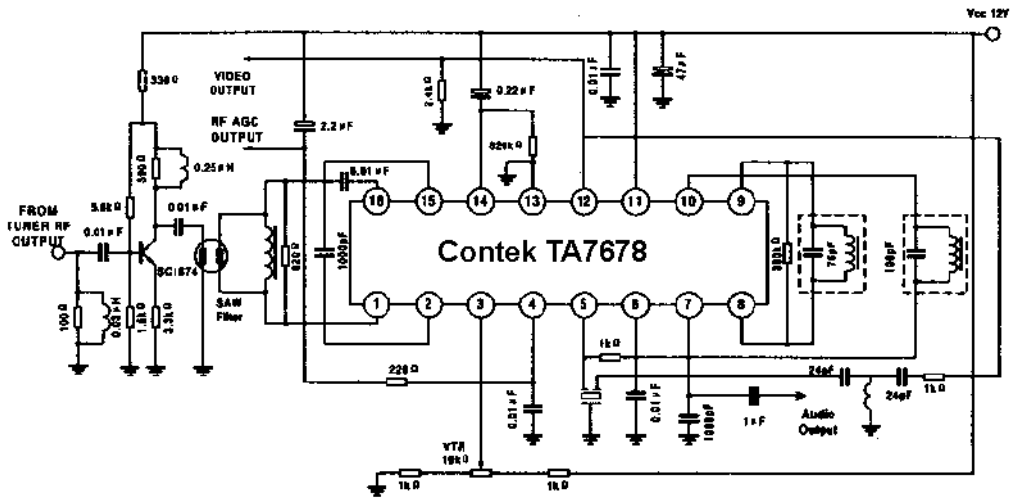
9. AUDIO OUTPUT IMPEDANCE TEST CIRCUIT



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TYPICAL APPLICATION CIRCUIT



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