



STD3NC50

N - CHANNEL 500V - 2.4Ω - 3A TO-251/TO-252 PowerMESH™ II MOSFET

PRELIMINARY DATA

TYPE	V _{DSS}	R _{DS(on)}	I _D
STD3NC50	500 V	< 2.7 Ω	3 A

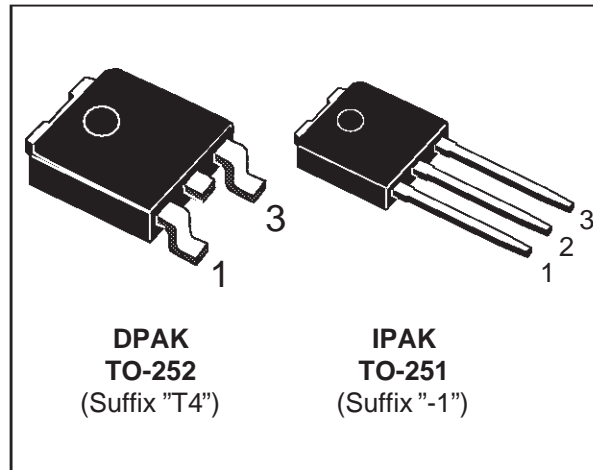
- TYPICAL R_{DS(on)} = 2.4 Ω
- EXTREMELY HIGH dv/dt CAPABILITY
- 100% AVALANCHE TESTED
- NEW HIGH VOLTAGE BENCHMARK
- GATE CHARGE MINIMIZED
- ADD SUFFIX "T4" FOR ORDERING IN TAPE & REEL.

DESCRIPTION

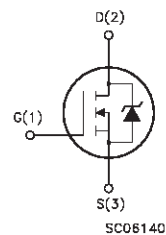
The PowerMESH™ II is the evolution of the first generation of MESH OVERLAY™. The layout refinements introduced greatly improve the Ron*area figure of merit while keeping the device at the leading edge for what concerns switching speed, gate charge and ruggedness.

APPLICATIONS

- HIGH CURRENT, HIGH SPEED SWITCHING
- SWITCH MODE POWER SUPPLIES (SMPS)
- DC-AC CONVERTERS FOR WELDING EQUIPMENT AND UNINTERRUPTIBLE POWER SUPPLIES AND MOTOR DRIVER



INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source Voltage (V _{GS} = 0)	500	V
V _{DGR}	Drain- gate Voltage (R _{GS} = 20 kΩ)	500	V
V _{GS}	Gate-source Voltage	± 30	V
I _D	Drain Current (continuous) at T _c = 25 °C	3.2	A
I _D	Drain Current (continuous) at T _c = 100 °C	2	A
I _{DM} (●)	Drain Current (pulsed)	12.8	A
P _{tot}	Total Dissipation at T _c = 25 °C	60	W
	Derating Factor	0.48	W/°C
dv/dt(1)	Peak Diode Recovery voltage slope	4	V/ns
T _{stg}	Storage Temperature	-65 to 150	°C
T _j	Max. Operating Junction Temperature	150	°C

(●) Pulse width limited by safe operating area

(1) I_{SD} ≤ 3 A, di/dt ≤ 100 A/μs, V_{DD} ≤ V_{(BR)DSS}, T_j ≤ T_{JMAX}

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THERMAL DATA

$R_{thj-case}$	Thermal Resistance Junction-case	Max	2.0	$^{\circ}C/W$
$R_{thj-amb}$	Thermal Resistance Junction-ambient	Max	100	$^{\circ}C/W$
$R_{thc-sink}$	Thermal Resistance Case-sink	Typ	1.5	$^{\circ}C/W$
T_I	Maximum Lead Temperature For Soldering Purpose		275	$^{\circ}C$

AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I_{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T_j max)	3	A
E_{AS}	Single Pulse Avalanche Energy (starting $T_j = 25^{\circ}C$, $I_D = I_{AR}$, $V_{DD} = 50$ V)	40	mJ

ELECTRICAL CHARACTERISTICS ($T_{case} = 25^{\circ}C$ unless otherwise specified)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	$I_D = 250 \mu A$ $V_{GS} = 0$	500			V
I_{DSS}	Zero Gate Voltage Drain Current ($V_{GS} = 0$)	$V_{DS} = \text{Max Rating}$ $V_{DS} = \text{Max Rating}$ $T_c = 125^{\circ}C$			1 50	μA μA
I_{GSS}	Gate-body Leakage Current ($V_{DS} = 0$)	$V_{GS} = \pm 30$ V			± 100	nA

ON (*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$ $I_D = 250 \mu A$	2	3	4	V
$R_{DS(on)}$	Static Drain-source On Resistance	$V_{GS} = 10$ V $I_D = 1.5$ A		2.4	2.7	Ω
$I_{D(on)}$	On State Drain Current	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$ $V_{GS} = 10$ V	3			A

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (*)	Forward Transconductance	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$ $I_D = 1.5$ A		2		S
C_{iss}	Input Capacitance	$V_{DS} = 25$ V $f = 1$ MHz $V_{GS} = 0$		400		pF
C_{oss}	Output Capacitance			62		pF
C_{rss}	Reverse Transfer Capacitance			7.5		pF

ELECTRICAL CHARACTERISTICS (continued)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Time	$V_{DD} = 300\text{ V}$ $I_D = 1.5\text{ A}$		11		ns
t_r	Rise Time	$R_G = 4.7\ \Omega$ $V_{GS} = 10\text{ V}$		8		ns
Q_g	Total Gate Charge	$V_{DD} = 480\text{ V}$ $I_D = 3\text{ A}$ $V_{GS} = 10\text{ V}$		15	21	nC
Q_{gs}	Gate-Source Charge			6.5		nC
Q_{gd}	Gate-Drain Charge			5		nC

SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{r(Voff)}$	Off-voltage Rise Time	$V_{DD} = 400\text{ V}$ $I_D = 3\text{ A}$		8		ns
t_f	Fall Time	$R_G = 4.7\ \Omega$ $V_{GS} = 10\text{ V}$		5		ns
t_c	Cross-over Time			14		ns

SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				3	A
$I_{SDM}(\bullet)$	Source-drain Current (pulsed)				12	A
$V_{SD}(\ast)$	Forward On Voltage	$I_{SD} = 3\text{ A}$ $V_{GS} = 0$			1.6	V
t_{rr}	Reverse Recovery Time	$I_{SD} = 3\text{ A}$ $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 100\text{ V}$ $T_j = 150\text{ }^\circ\text{C}$		245		ns
Q_{rr}	Reverse Recovery Charge			980		μC
I_{RRM}	Reverse Recovery Current			8		A

(*) Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %

(•) Pulse width limited by safe operating area

Fig. 1: Unclamped Inductive Load Test Circuit

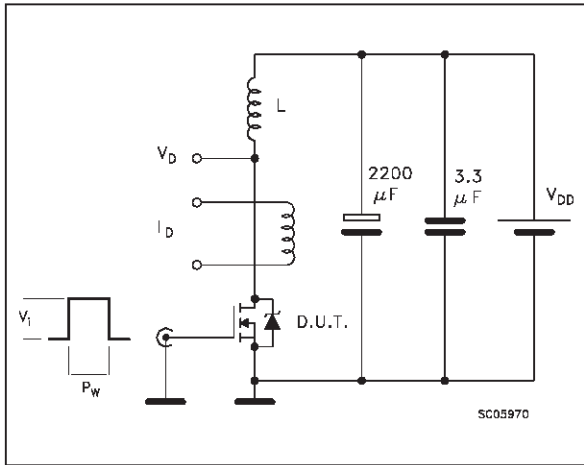


Fig. 2: Unclamped Inductive Waveform

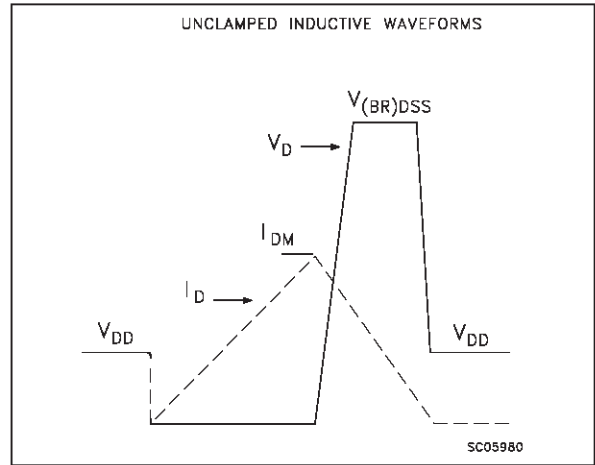


Fig. 3: Switching Times Test Circuits For Resistive Load

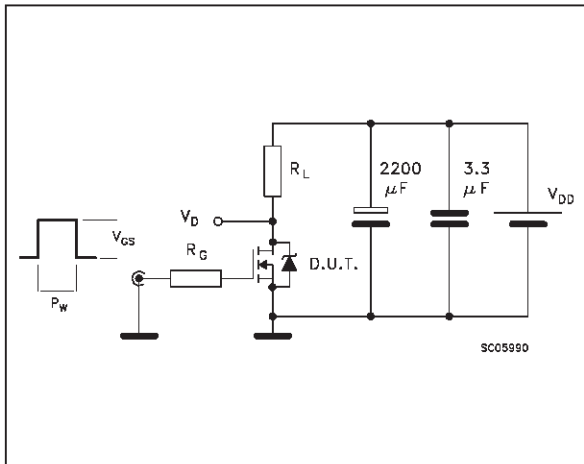


Fig. 4: Gate Charge test Circuit

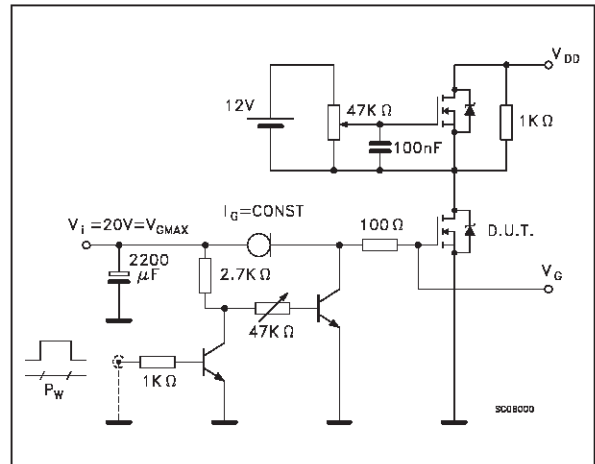
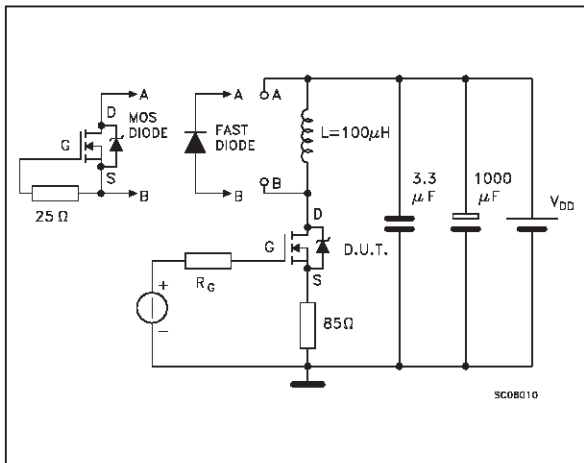
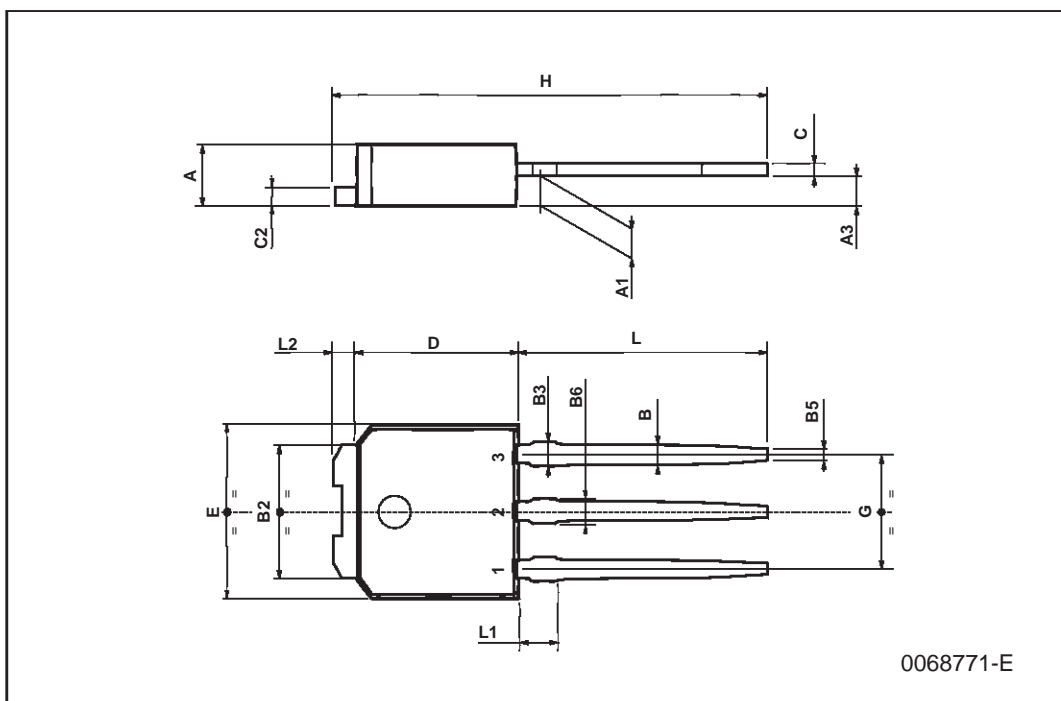


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



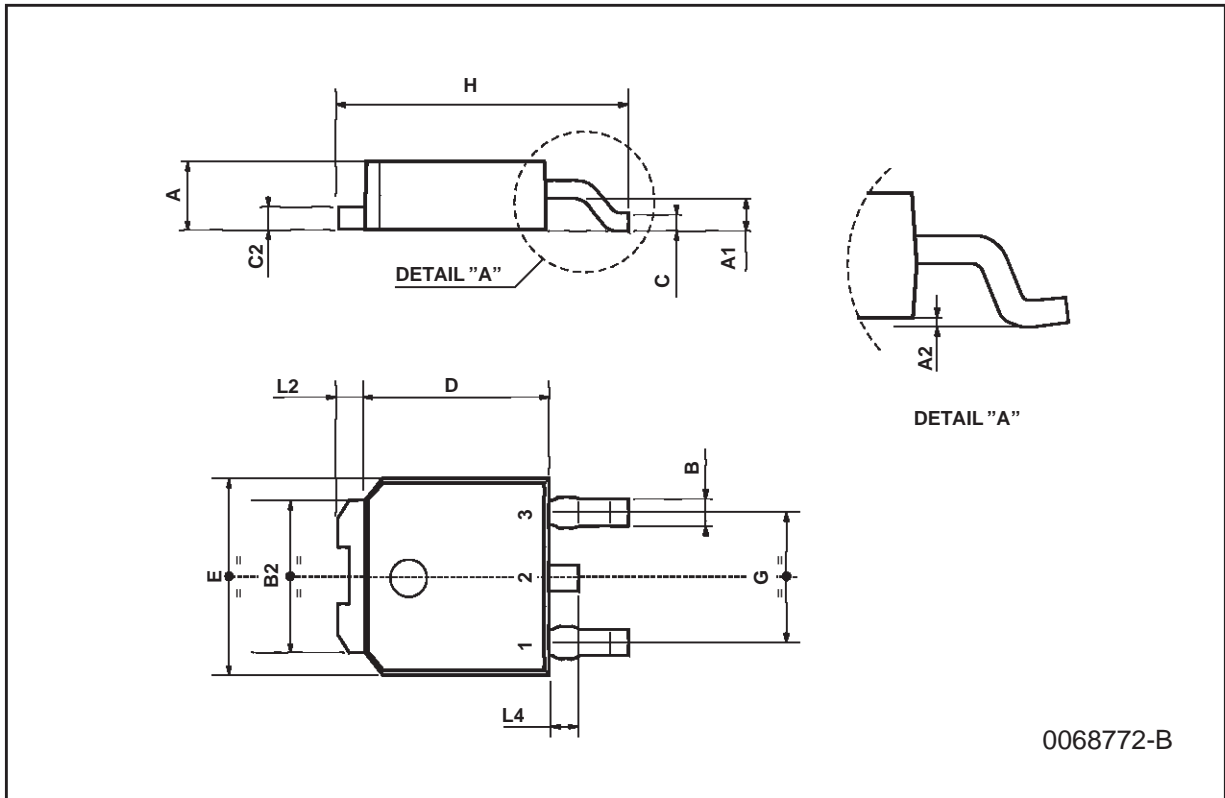
TO-251 (IPAK) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A3	0.7		1.3	0.027		0.051
B	0.64		0.9	0.025		0.031
B2	5.2		5.4	0.204		0.212
B3			0.85			0.033
B5		0.3			0.012	
B6			0.95			0.037
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
E	6.4		6.6	0.252		0.260
G	4.4		4.6	0.173		0.181
H	15.9		16.3	0.626		0.641
L	9		9.4	0.354		0.370
L1	0.8		1.2	0.031		0.047
L2		0.8	1		0.031	0.039



TO-252 (DPAK) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.64		0.9	0.025		0.035
B2	5.2		5.4	0.204		0.212
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
E	6.4		6.6	0.252		0.260
G	4.4		4.6	0.173		0.181
H	9.35		10.1	0.368		0.397
L2		0.8			0.031	
L4	0.6		1	0.023		0.039



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