Ordering number: EN 5633

CMOS LSI

LC865032A, 865028A, 865024A

8-Bit Single-Chip Microcontroller

Overview

The LC865032A/28A/24A microcontrollers are 8-bit single-chip microcontrollers with the following on-chip functional blocks :

- CPU : Operable at a minimum bus cycle time of 0.5 µs (microsecond)
- On-chip ROM capacity : Up to 32K bytes
- On-chip RAM capacity : 512 bytes (LC865032A/28A/24A)
- 16-bit timer/counter (or two 8-bit timers)
- 16-bit timer/PWM (or two 8-bit timers)
- 8-channel × 8-bit A/D converter
- Two 8-bit synchronous serial-interface circuits
- 13-source 10-vectored interrupt system

All of the functions above are fabricated on a single chip.

Features

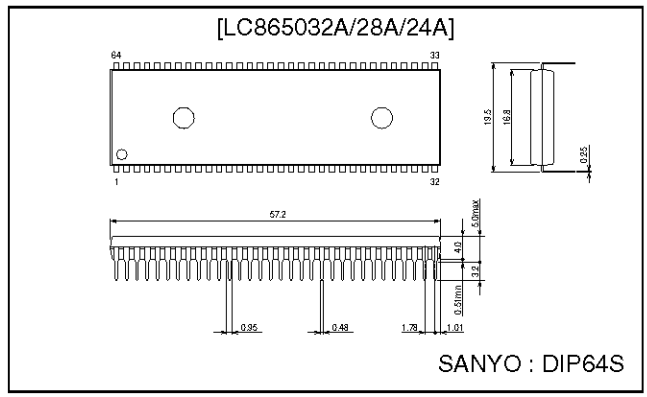
(1) Read-Only Memory (ROM) :
LC865032A 32512 × 8 bits
LC865028A 28672 × 8 bits
LC865024A 24576 × 8 bits

(2) Random Access Memory (RAM) :
LC865032A/28A/24A 512 × 8 bits

Package Dimensions

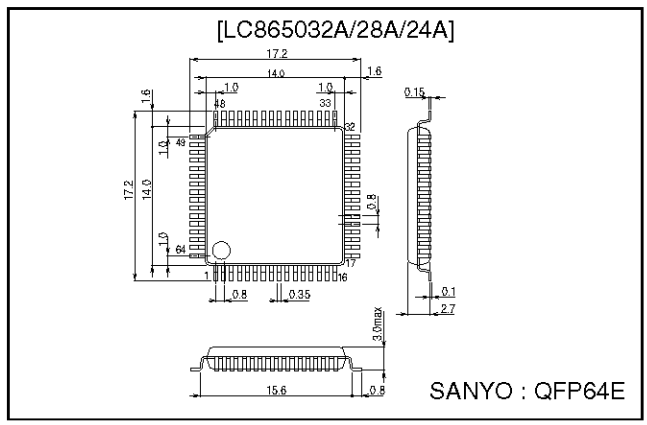
unit : mm

3071-DIP64S



unit : mm

3159-QFP64E



(3) Bus cycle time / Instruction cycle time

The LC865032A/28A/24A microcontrollers are constructed to read ROM twice within one instruction cycle. This results in 1.7 times better performance within the same instruction cycle compared to our 4-bit microcontrollers (the LC66000 series). Bus cycle time indicates the speed to read ROM.

Bus cycle time	Cycle time	System clock oscillation	Oscillation frequency	Supply voltage
0.5 µs	1 µs	Ceramic resonator	12 MHz	4.5 to 6.0V
2 µs	4 µs	Ceramic resonator	3 MHz	2.7 to 6.0V
7.5 µs	15 µs	RC oscillator	800 kHz	2.7 to 6.0V
183 µs	366 µs	Crystal oscillator	32.768 kHz	2.7 to 6.0V

(4) Ports

- Input/output ports : 6 ports (42 pins)
  Input/output port programmable in nibble units : 1 port (8 pins)
  (However, when N-channel open-drain output is selected, bit-unit input is possible.)
  Input/output port each bit programmable : 5 ports (34 pins)
  Include 15 V withstand N-channel open drain output port : 3 ports (18 pins)
- Input ports : 2 ports (13 pins)

(5) A/D converter

- 8-channel × 8-bit A/D converter

(6) Serial-interface

- Two 8-bit serial-interface circuits
  LSB first / MSB first functions switchable
- Internal 8-bit band-rate generator in common with two serial-interface circuits

(7) Timer

- Timer 0
  16-bit timer/counter
  2-bit prescaler + 8-bit programmable prescaler
  Mode 0 : Two 8-bit timers with programmable prescaler
  Mode 1 : 8-bit timer with programmable prescaler + 8-bit counter
  Mode 2 : 16-bit timer with programmable prescaler
  Mode 3 : 16-bit counter
  The resolution of Timer is fixed to tCYC. (tCYC : cycle time)
- Timer 1
  16-bit timer/PWM
  Mode 0 : Two 8-bit timers
  Mode 1 : 8-bit timer + 8-bit PWM
  Mode 2 : 16-bit timer
  Mode 3 : Variable-bit PWM (9 to 16 bits)
  In Mode 0 and Mode1, the resolution of Timer and PWM is fixed to tCYC.
  In Mode 2 and Mode 3, the resolution of Timer and PWM can be programmed to be tCYC or 1/2 tCYC
- Base timer
  Every 500 ms overflow system for clock applications (using 32.768 kHz crystal oscillator for Base timer clock)
  Every 976 µs, 3.9 ms, 15.6 ms, 62.5 ms overflow system (using 32.768 kHz crystal oscillator for Base timer clock)
- Base timer clock selectable
  32.768 kHz crystal oscillator, system clock, and programmable prescaler output of Timer 0

(8) Buzzer output
- The buzzer sound frequency is selectable ; 4 kHz, 2 kHz (using 32.768 kHz crystal oscillator for base timer clock)

(9) Remote-controlled receiver circuit (shares P73/INT3/T0IN pin)
- Noise rejection function
- Polarity switching

(10) Watchdog timer
- RC external watchdog timer
- Watchdog timer operation can be selected : Interrupt/reset

(11) Interrupt system
- 13-source 10-vectored interrupts :
  1. External interrupt INT0 (including watchdog timer)
  2. External interrupt INT1
  3. External interrupt INT2, Timer/counter T0L (lower 8 bits)
  4. External interrupt INT3, base timer
  5. Timer/counter T0H (upper 8-bits)
  6. Timer T1L, timer T1H
  7. Serial-interface SIO0
  8. Serial-interface SIO1
  9. A/D converter
  10. Port 0
- Built-in interrupt priority control register
  Microcontroller supports 3 levels of multiple interrupt; low level, high level, and highest level. For the 11 interrupt requests from INT2 through Port 0, high/low level interrupt priority can be specified using the priority control register. Also, for INT0 and INT1, highest/low level interrupt priority can be specified.

(12) Real-time service operation
Synchronizing with the interrupt request signals, the real-time service starts a 4-byte data transfer between which special function registers within 1-instruction cycle after the request signal occurs, and then completes its operation within 5-instruction cycles. This operation is performed in parallel with CPU operation.

(13) Subroutine stack
- 128 levels (Max.) : The stack is located in RAM.

(14) Multiplication and division
16 bits × 8 bits (7-instruction cycles)
16 bits / 8 bits (7-instruction cycles)

(15) 3 oscillation circuits
- On-chip RC oscillator circuit for the system clock
- On-chip CF oscillator circuit for the system clock
- On-chip crystal oscillator circuit for the system clock and the time-base clock
  XT1 pin can be used as $\overline{P74}$.

(16) Standby function

- HALT mode
  HALT mode is used to reduce power dissipation. In this mode, program execution is stopped. This mode can be released by an interrupt request signal or initial system reset request signal.
- HOLD mode
  The HOLD mode is used to stop all oscillators RC (internal), CR and Crystal. This mode can be released by the following operations
  • Set Low level to Reset pin ($\overline{\text{RES}}$).
  • Set predefined level to P70/INT0, P71/INT1 pins (programmable).
  • Set Low level to Port 0 pin/pins (programmable).

(17) Factory shipment

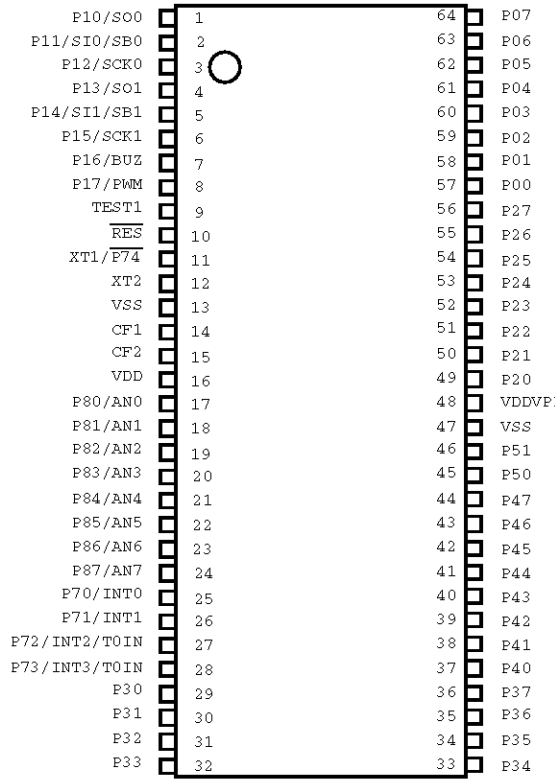
• DIP64S , QFP64E delivery form

(18) Development support tools

Evaluation (EVA) chip	:	LC866098
EPROM version	:	LC86E5032
One time ROM version	:	LC86P5032
Emulator	:	EVA-86000 + ECB866600 (Evaluation chip board) + POD865000 (POD for DIP64S) / + POD865010 (POD for QFP64E)

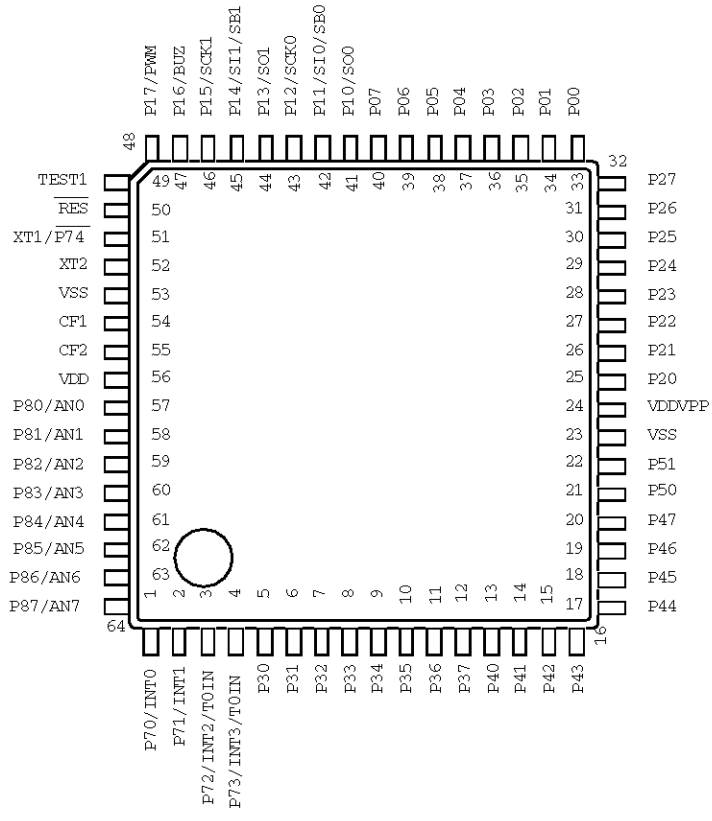
Pin Assignments

DIP64S



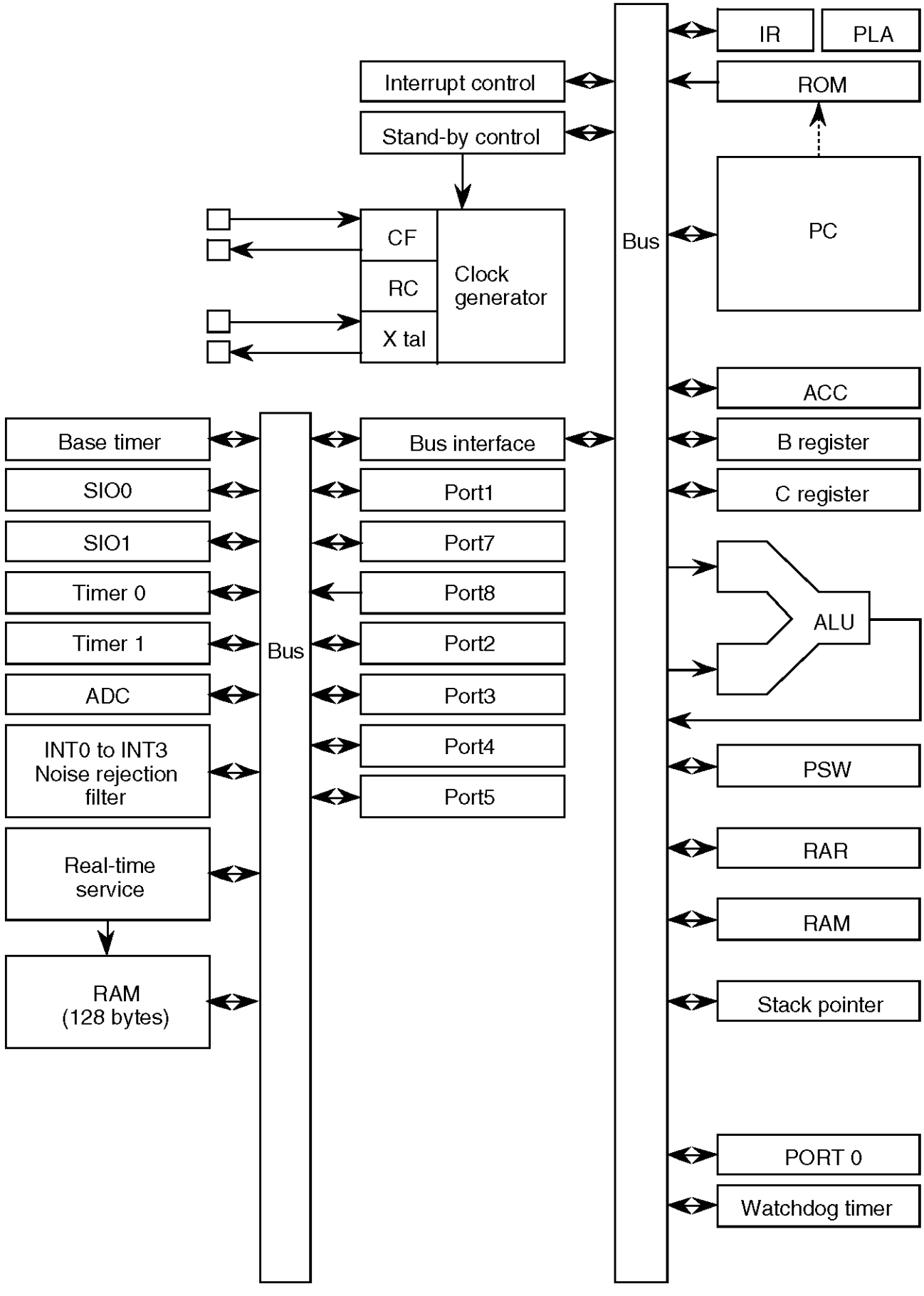
Top view

QFP64E



Top view

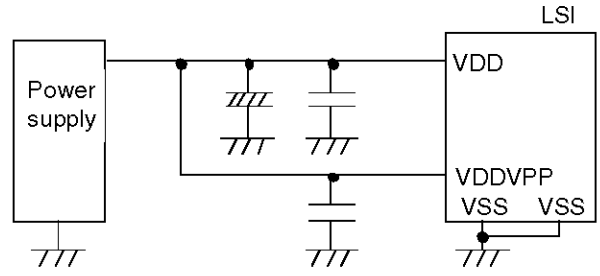
System Block Diagram



Pin Description

Pin name	I/O	Function description	Option
VSS		Power supply (–)	
VDD		Power supply (+)	
VDDVPP*		Power supply (+)	
PORT0 P00 to P07	I/O	• 8-bit input/output port • Input for port 0 interrupt • Data direction programmable in nibble units • Input for HOLD release	• Pull-up resistor : Present / Not present • Output form : CMOS/N-channel open-drain
PORT1 P10 to P17	I/O	• 8-bit input/output port • Data direction can be specified for each bit. • Other pin functions P10 SIO0 data output P11 SIO0 data input /bus input/output P12 SIO0 clock input/output P13 SIO1 data output P14 SIO1 data input /bus input/output P15 SIO1 clock input/output P16 Buzzer output P17 Timer1 output (PWM output)	• Output form : CMOS/N-channel open-drain
PORT2 P20 to P27	I/O	• 8-bit input/output port • Input/output in bit units	Output form : CMOS/N-channel open-drain
PORT3 P30 to P37	I/O	• 8-bit input/output port • Input/output in bit units • 15 V withstand at N-channel open-drain output	• Pull-up resistor : Present / Not present • Output form : CMOS/N-channel open-drain
PORT4 P40 to P47	I/O	• 8-bit input/output port • Input/output in bit units • 15 V withstand at N-channel open-drain output	• Pull-up resistor : Present / Not present • Output form : CMOS/N-channel open-drain
PORT5 P50 , P51	I/O	• 2-bit input/output port • Input/output in bit units • 15 V withstand at N-channel open-drain output	• Pull-up resistor : Present / Not present • Output form : CMOS/N-channel open-drain

* Connect as in the following figure to reduce noise into VDD.
Short-circuit the V_{DD} terminal to the VDDVPP pin.
Short-circuit the two VSS pins.



<table>
<tr><th>Pin name</th><th>I/O</th><th>Function description</th><th>Option</th></tr>
<tr><td>PORT7

P70

P71 to $\overline{P74}$</td><td>

I/O

I</td><td>• 5-bit input port
• Other pin functions
P70: INT0 input / HOLD release
/ N-channel Tr. output for watchdog timer
P71: INT1 input / HOLD release input
P72: INT2 input / timer 0 event input
P73: INT3 input with noise filter/timer 0 event input
$\overline{P74}$: XT1 input pin for 32.768 kHz crystal
oscillator
• Interrupt received form, vector address
<table>
<tr><th></th><th>Rising</th><th>Falling</th><th>Rising & falling</th><th>High level</th><th>Low level</th><th>Vector</th></tr>
<tr><td>INT0</td><td>Enable</td><td>Enable</td><td>Disable</td><td>Enable</td><td>Enable</td><td>03H</td></tr>
<tr><td>INT1</td><td>Enable</td><td>Enable</td><td>Disable</td><td>Enable</td><td>Enable</td><td>0BH</td></tr>
<tr><td>INT2</td><td>Enable</td><td>Enable</td><td>Enable</td><td>Disable</td><td>Disable</td><td>13H</td></tr>
<tr><td>INT3</td><td>Enable</td><td>Enable</td><td>Enable</td><td>Disable</td><td>Disable</td><td>1BH</td></tr>
</table></td><td>Pull-up resistor :
Present / Not present
(P70,71,72,73)
* $\overline{P74}$ does not have pull-up resistor option.</td></tr>
<tr><td>PORT8
P80 to P87</td><td>I</td><td>• 8-bit input port
• Other function
A/D input port (8 port pins)</td><td></td></tr>
<tr><td>$\overline{RES}$</td><td>I</td><td>Reset pin with pull-up resistor</td><td></td></tr>
<tr><td>TEST1</td><td>O</td><td>• Test pin
Should be left open.
• Output fixed HIGH</td><td></td></tr>
<tr><td>XT1/$\overline{P74}$</td><td>I</td><td>• Input pin for 32.768 kHz crystal oscillator
• Other function
Input port $\overline{P74}$
When not in use, connect to V_{DD}.</td><td></td></tr>
<tr><td>XT2</td><td>O</td><td>Output pin for 32.768 kHz crystal oscillator
When not in use, should be left open.</td><td></td></tr>
<tr><td>CF1</td><td>I</td><td>Input pin for ceramic resonator oscillator</td><td></td></tr>
<tr><td>CF2</td><td>O</td><td>Output pin for ceramic resonator oscillator</td><td></td></tr>
</table>

• All port options can be specified for each bit.

• State of pins at reset

Pin name	Input/output mode	State of pull-up resistor specified at pull-up option
Port 0 P70, 71, 72, 73	Input	Fixed pull-up resistor exist
Ports 1, 2 Ports 3, 4, 5	Input	Programmable pull-up resistor OFF

Specifications

1. Absolute Maximum Ratings at Ta = 25°C , V_{SS} = 0 V

Parameter		Symbol	Pins	Conditions		Ratings			Unit
					V_{DD}[V]	min	typ	max	
Supply voltage		V_{DD} max	VDD, VDDVPP	VDD = VDDVPP		–0.3		+7.0	V
Input voltage		V_I(1)	• P71, 72, 73, $\overline{74}$ • Port 8 • $\overline{RES}$			–0.3		V_{DD}+0.3	
Input/output voltage		V_{IO}(1)	• Ports 0, 1, 2 • Ports 3, 4, 5 at CMOS output option			–0.3		V_{DD}+0.3	
		V_{IO}(2)	P 3, 4, 5 at N-ch open-drain output option			–0.3		+15	
High-level output current	Peak output current	I_{OPH}(1)	Ports 0, 1, 2, 3, 4, 5	CMOS output at each pin		–4			mA
	Total output current	ΣI_{OAH}(1)	Ports 0, 1	Total of all pins		–20			
		ΣI_{OAH}(2)	Ports 2, 3, 4, 5	Total of all pins		–20			
Low-level output current	Peak output current	I_{OPL}(1)	Ports 0, 1, 2, 3, 4, 5	At each pin				20	
		I_{OPL}(2)	P70	At each pin				15	
	Total output current	ΣI_{OAL}(1)	Port 0 P70	Total of all pins				40	
		ΣI_{OAL}(2)	Port 2	Total of all pins				40	
		ΣI_{OAL}(3)	Ports 3, 4, 5	Total of all pins				80	
Power dissipation (max.)		Pd max (1)	DIP64S	Ta = –30 to +70°C				700	mW
		Pd max (2)	QFP64E	Ta = –30 to +70°C				420	
Operating temperature range		Topr				–30		+70	°C
Storage temperature range		Tstg				–65		+150	

2. Recommended Operating Ranges at Ta = –30°C to +70°C, V_{SS} = 0 V

Parameter	Symbol	Pins	Conditions		Ratings			Unit
				V_{DD}[V]	min	typ	max	
Operating voltage range	V_{DD}(1)	VDD	0.98 µs ≤ tCYC tCYC ≤ 400 µs		4.5		6.0	V
	V_{DD}(2)		3.9 µs ≤ tCYC tCYC ≤ 400 µs		2.7		6.0	
HOLD voltage	V_{HD}	VDD	RAM and Registers hold voltage at HOLD mode.		2.0		6.0	
Input high-level voltage	V_{IH}(1)	Port 0 (Schmitt)	Output disable	2.7 to 6.0	0.4V_{DD} +0.9		V_{DD}	
	V_{IH}(2)	• Ports 1, 2 • P72, 73 (Schmitt)	Output disable	2.7 to 6.0	0.75V_{DD}		V_{DD}	
	V_{IH}(3)	• P70 Port input/interrupt • P71 • $\overline{RES}$ (Schmitt)	Output N-channel transistor OFF	2.7 to 6.0	0.75V_{DD}		V_{DD}	
	V_{IH}(4)	P70 Watchdog timer	Output N-channel transistor OFF	2.7 to 6.0	0.9V_{DD}		V_{DD}	
	V_{IH}(5)	• $\overline{P74}$ • Port 8	Output N-channel transistor OFF	27 to 6.0	0.75V_{DD}		V_{DD}	
	V_{IH}(6)	Ports 3, 4, 5 of CMOS output (Schmitt)	Output disable	4.0 to 6.0	0.75V_{DD}		V_{DD}	
				2.7 to 4.0	0.8V_{DD}		V_{DD}	
	V_{IH}(7)	Ports 3, 4, 5 of open-drain output (Schmitt)	Output disable	4.0 to 6.0	0.75V_{DD}		13.5	
				2.7 to 4.0	0.8V_{DD}		13.5	
Input low-level voltage	V_{IL}(1)	Port 0 (Schmitt)	Output disable	2.7 to 6.0	V_{SS}		0.2V_{DD}	
	V_{IL}(2)	• Ports 1, 2, 3, 4, 5 • P72, 73 (Schmitt)	Output disable	2.7 to 6.0	V_{SS}		0.25V_{DD}	
	V_{IL}(3)	• P70 Port input/interrupt • P71 • RES (Schmitt)	N-channel transistor OFF	2.7 to 6.0	V_{SS}		0.25V_{DD}	
	V_{IL}(4)	P70 Watchdog timer	N-channel transistor OFF	2.7 to 6.0	V_{SS}		0.8V_{DD} –1.0	
	V_{IL}(5)	• $\overline{P74}$ • Port 8	Output N-channel transistor OFF	2.7 to 6.0	V_{SS}		0.25V_{DD}	
Operating cycle time	tCYC			4.5 to 6.0	0.98		400	µs
				2.7 to 6.0	3.9		400	

Parameter	Symbol	Pins	Conditions	Ratings				Unit
				V_{DD}[V]	min	typ	max	
Oscillation frequency range (Note 1)	FmCF(1)	CF1, CF2	• 12 MHz (ceramic resonator oscillation). • Refer to Figure 1.	4.5 to 6.0	11.76	12	12.24	MHz
	FmCF(2)	CF1, CF2	• 3 MHz (ceramic resonator oscillation). • Refer to Figure 1.	2.7 to 6.0	2.94	3	3.06	
	FmRC		RC oscillation	2.7 to 6.0	0.4	0.8	3.0	
	FsXtal	XT1, XT2	• 32.768 kHz (crystal oscillation). • Refer to Figure 2.	2.7 to 6.0		32.768		kHz
Oscillation stable time period (Note 1)	tmsCF(1)	CF1, CF2	• 12 MHz (ceramic resonator oscillation). • Refer to Figure 3.	4.5 to 6.0		0.03	0.5	ms
	tmsCF(2)	CF1, CF2	• 3 MHz (ceramic resonator oscillation). • Refer to Figure 3.	4.5 to 6.0		0.2	2	
				2.7 to 6.0		0.2	6	
	tssXtal	XT1, XT2	• 32.768 kHz (crystal oscillation). • Refer to Figure 3.	4.5 to 6.0		1	1.5	s
				2.7 to 6.0		1	3	

(Note 1) Refer to Table 1 and Table 2 for oscillation constant.

3. Electrical Characteristics at Ta = –30°C to +70°C, V_{SS} = 0 V

Parameter	Symbol	Pins	Conditions	V_{DD}[V]	Ratings min	Ratings typ	Ratings max	Unit
Input high-level current	I_{IH}(1)	Ports 3, 4, 5 of open-drain output	• Output disabled • V_{IN} = 13.5 V (including off-state leak current of the output transistor)	2.7 to 6.0			5	µA
	I_{IH}(2)	• Port 0 without pull-up MOS transistor • Ports 1, 2, 3, 4, 5	• Output disabled • Pull-up MOS transistor OFF. V_{IN} = V_{DD} (including off-state leak current of the output transistor)	2.7 to 6.0			1	
	I_{IH}(3)	• P70, 71, 72, 73 without pull-up MOS transistor • Port 8	V_{IN} = V_{DD}	2.7 to 6.0			1	
	I_{IH}(4)	$\overline{RES}$	V_{IN} = V_{DD}	2.7 to 6.0			1	
Input low-level current	I_{IL}(1)	• Ports 1, 2, 3, 4, 5 • Port 0 without pull-up MOS transistor	• Output disabled • Pull-up MOS transistor OFF. V_{IN} = V_{SS} (including off-state leak current of the output transistor)	2.7 to 6.0	–1			
	I_{IL}(2)	• P70, 71, 72, 73 without pull-up MOS transistor • Port 8	V_{IN} = V_{SS}	2.7 to 6.0	–1			
	I_{IL}(3)	$\overline{RES}$	V_{IN} = V_{SS}	2.7 to 6.0	–1			
Output high-level voltage	V_{OH}(1)	Ports 1, 2, 3, 4, 5 of CMOS output	I_{OH} = –1 mA	4.5 to 6.0	V_{DD}–1			V
	V_{OH}(2)		I_{OH} = –0.1 mA	2.7 to 6.0	V_{DD}–0.5			
Output low-level voltage	V_{OL}(1)	Ports 1, 2, 3, 4, 5	I_{OL} = 10 mA	4.5 to 6.0			1.5	
	V_{OL}(2)		I_{OL} = 1.6 mA	4.5 to 6.0			0.4	
	V_{OL}(3)		• I_{OL} = 1.0 mA • The current of any unmeasured pin is 1 mA or less.	2.7 to 6.0			0.4	
	V_{OL}(4)	P70	I_{OL} = 1 mA	4.5 to 6.0			0.4	
	V_{OL}(5)		I_{OL} = 0.5 mA	2.7 to 6.0			0.4	
Pull-up MOS transistor resistor	Rpu	• Ports 1, 2, 3, 4, 5 • P70, 71, 72, 73	V_{OH} = 0.9 V_{DD}	4.5 to 6.0	15	40	70	kΩ
				2.7 to 4.5	25	70	150	
Hysteresis voltage	V_{HIS}	• Ports 1, 2, 3, 4, 5 • P70, 71, 72, 73 • $\overline{RES}$	Output disable	2.7 to 6.0		0.1V_{DD}		V
Pin capacitance	CP	All pins	• f = 1 MHz Unmeasured input pins are set to V_{SS} level. • Ta = 25°C	2.7 to 6.0		10		pF

4. Serial Input/Output Characteristics at Ta = –30°C to +70°C, V_{SS} = 0 V

Parameter			Symbol	Pins	Conditions	Ratings				Unit
						V_{DD}[V]	min	typ	max	
Serial clock	Input clock	Cycle	tCKCY(1)	SCK0, SCK1	Refer to Figure 5.	2.7 to 6.0	2			tCYC
		Low-level pulse width	tCKL(1)			2.7 to 6.0	1			
		High-level pulse width	tCKH(1)			2.7 to 6.0	1			
	Output clock	Cycle	tCKCY(2)	SCK0, SCK1	• Use an external pull-up resistor (1 kΩ) with open-drain output. • Refer to Figure 5.	2.7 to 6.0	2			
		Low-level pulse width	tCKL(2)			2.7 to 6.0		1/2tCKCY		
		High-level pulse width	tCKH(2)			2.7 to 6.0		1/2tCKCY		
Serial input	Data setup time		tICK	• SI0, SI1 • SB0, SB1	• Set to the rise of SCK0, SCK1. • Refer to Figure 5.	4.5 to 6.0	0.1			µs
						2.7 to 6.0	0.4			
	Data hold time		tCKI			4.5 to 6.0	0.1			
						2.7 to 6.0	0.4			
Serial output	Output delay time (Serial clock is extrnal clock.)		tCKO(1)	• SO0, SO1 • SB0, SB1	• Use an external pull-up resistor (1 kΩ) with open-drain output.	4.5 to 6.0			7/12tCYC +0.2	
						2.7 to 6.0			7/12tCYC +1	
	Output delay time (Serial clock is internal clock.)		tCKO(2)		• Set to the fall of SCK0, SCK1. • Refer to Figure 5.	4.5 to 6.0			1/3tCYC +0.2	
						2.7 to 6.0			1/3tCYC +1	

5. Pulse Input Conditions at Ta = –30°C to +70°C, V_{SS} = 0 V

Parameter	Symbol	Pins	Conditions	Ratings				Unit
				V_{DD}[V]	min	typ	max	
High/low-level pulse width	tPIH(1) tPIL(1)	• INT0, INT1 • INT2/T0IN • INT3	• Interrupt acceptable • Timer/counter 0 pulse countable	2.7 to 6.0	1			tCYC
	tPIH(2) tPIL(2)	INT3/T0IN (Noise rejection filter time constant is 1/1.)	Interrupt acceptable	2.7 to 6.0	2			
	tPIH(3) tPIL(3)	INT3/T0IN (Noise rejection filter time constant is 1/16.)	Interrupt acceptable	2.7 to 6.0	32			
	tPIL(4)	$\overline{RES}$	Reset acceptable	2.7 to 6.0	200			µs

6. A/D Converter Characteristics at Ta = –30°C to +70°C, V_{SS} = 0 V

Parameter	Symbol	Pins	Conditions	Ratings				Unit
				V_{DD}[V]	min	typ	max	
Resolution	N			4.5 to 6.0		8		bit
Absolute precision	ET		(Note 2)	4.5 to 6.0			±1.5	LSB
Conversion time	tCAD		A/D conversion time = 16 × tCYC (ADCR2 = 0) (Note 3)	4.5 to 6.0	15.68 (tCYC = 0.98 µs)		65.28 (tCYC = 4.08 µs)	µs
			A/D conversion time = 32 × tCYC (ADCR2 = 1) (Note 3)		31.36 (tCYC = 0.98 µs)		130.56 (tCYC = 4.08 µs)	
Analog input voltage range	V_{AIN}	AN0 to AN7		4.5 to 6.0	V_{SS}		V_{DD}	V
Analog port input current	I_{AINH}		V_{AIN} = V_{DD}	4.5 to 6.0			+1	µA
	I_{AINL}		V_{AIN} = V_{SS}	4.5 to 6.0	–1			

(Note 2) Quantizing error (±1/2 LSB) is not included.

(Note 3) Conversion time is the period from execution of instruction starting the conversion to completion of shifting the A/D converted value to the register.

7. Current Drain Characteristics at Ta = –30°C to +70°C, V_{SS} = 0 V

Parameter	Symbol	Pins	Conditions	Ratings				Unit
				V_{DD}[V]	min	typ	max	
Current drain during basic operation (Note 4)	I_{DDOP}(1)	VDD	• FmCF = 12 MHz for ceramic resonator oscillation. • FsXtal = 32.768 kHz for crystal oscillator. • System clock : CF oscillator • Internal RC oscillator stopped.	4.5 to 6.0		10	20	mA
	I_{DDOP}(2)		• FmCF = 3 MHz for ceramic resonator oscillation. • FsXtal = 32.768 kHz for crystal oscillator. • System clock : CF oscillator • Internal RC oscillator stopped.	4.5 to 6.0		3	7	
	I_{DDOP}(3)			2.7 to 4.5		1.5	5	
	I_{DDOP}(4)		• FmCF = 0 Hz (when oscillator stops). • FsXtal = 32.768 kHz for crystal oscillator. • System clock : RC oscillator	4.5 to 6.0		0.7	3.0	
	I_{DDOP}(5)			2.7 to 4.5		0.4	2.5	
	I_{DDOP}(6)		• FmCF = 0 Hz (when oscillator stops). • FsXtal = 32.768 kHz for crystal oscillator. • System clock : 32.768 kHz • Internal RC oscillator stopped.	4.5 to 6.0		35	100	µA
	I_{DDOP}(7)			2.7 to 4.5		15	50	

Parameter	Symbol	Pins	Conditions	Ratings				Unit
				V_{DD}[V]	min	typ	max	
Current drain at HALT mode (Note 4)	I_{DDHALT}(1)	VDD	• HALT mode • FmCF = 12 MHz for ceramic resonator oscillation. • FsXtal = 32.768 kHz for crystal oscillatior. • System clock : CF oscillator. • Internal RC oscillator stopped.	4.5 to 6.0		5	10	mA
	I_{DDHALT}(2)		• HALT mode FmCF = 3 MHz for ceramic resonator oscillation. • FsXtal = 32.768 kHz for crystal oscillator. • System clock : CF oscillator. • Internal RC oscillator stopped.	4.5 to 6.0		2.2	4.6	
	I_{DDHALT}(3)			2.7 to 4.5		0.8	2.5	
	I_{DDHALT}(4)		• HALT mode FmCF = 0 Hz (when oscillator stops). • FsXtal = 32.768 kHz for crystal oscillator. • System clock : RC oscillator	4.5 to 6.0		400	1000	µA
	I_{DDHALT}(5)			2.7 to 4.5		200	750	
	I_{DDHALT}(6)		• HALT mode FmCF = 0 Hz (when oscillator stops). • FsXtal = 32.768 kHz for crystal oscillator. • System clock : 32.768 kHz • Internal RC oscillator stopped.	4.5 to 6.0		25	100	
	I_{DDHALT}(7)			2.7 to 4.5		8	40	
Current drain at HOLD mode (Note 4)	I_{DDHOLD}(1)	VDD	HOLD mode	4.5 to 6.0		0.05	30	
	I_{DDHOLD}(2)			2.7 to 4.5		0.02	20	

(Note 4) The currents to output transistors and pull-up MOS transistors are ignored.

Oscillation type	Supplier	Oscillator	C1	C2
12 MHz ceramic resonator oscillation	Murata	CSA12.0MTZ	33 pF	33 pF
		CST12.0MTW	On chip	
	Kyocera	KBR-12.0M	33 pF	33 pF
3 MHz ceramic resonator oscillation	Murata	CSA3.00MG040	100 pF	100 pF
		CST3.00MGW040	On chip	
	Kyocera	KBR-3.0MS	47 pF	47 pF

* K rank (±10%) and SL characteristics must be used for C1 and C2.

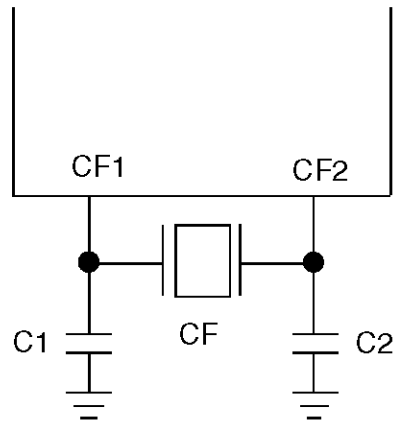
Table 1. Ceramic Resonator Oscillation Guaranteed Constants (Main clock)

Oscillation type	Supplier	Oscillator	C3	C4
32.768 kHz crystal oscillation	Kyocera	KF-38G-13P0200	18 pF	18 pF

* J rank (±5%) and CH characteristics must be used for C3 and C4.
(For applications which do not need high precision, use K rank (±10%) and SL characteristics.)

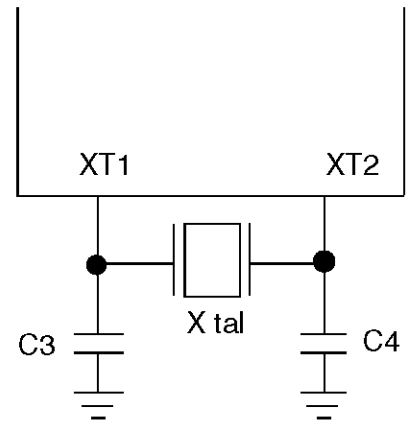
Table 2. Crystal Oscillation Guaranteed Constants (Sub-clock)

Notes
- Since the circuit pattern affects the oscillation frequency, place the oscillation-related parts as close to the oscillator pins as possible with the shortest pattern length.
- If other oscillators are used, we provide no guarantee for the characteristics.



Main-clock circuit

Figure 1 Ceramic Resonator Oscillator



Sub-clock circuit

Figure 2 Crystal Oscillator

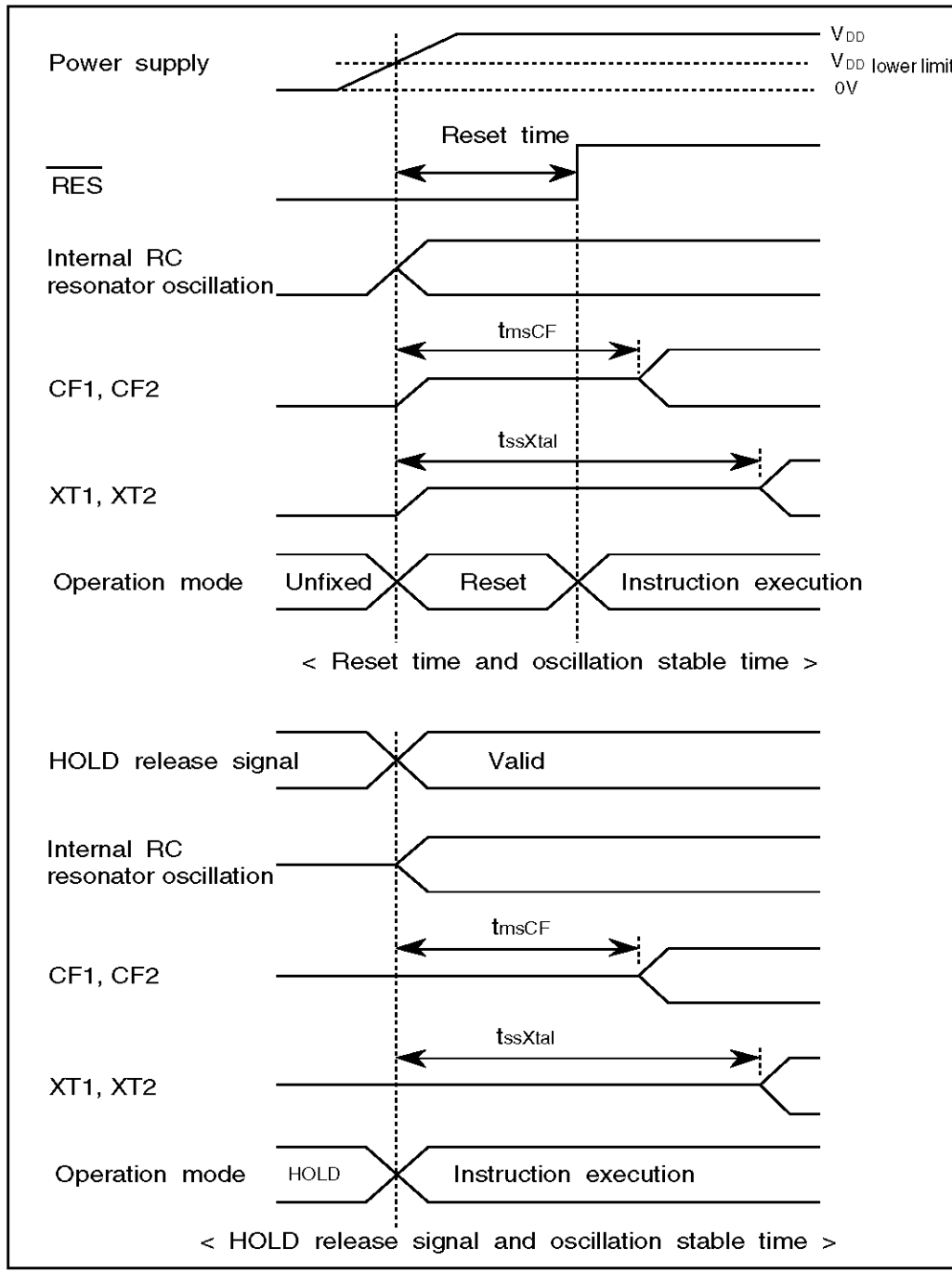
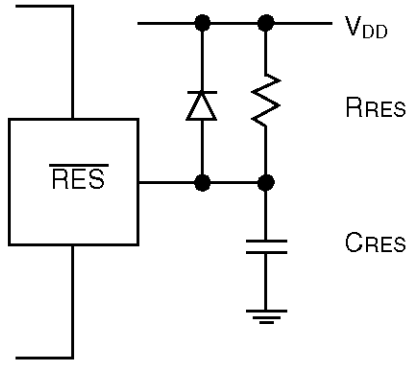


Figure 3 Oscillation Stable Time



(Note) Set the values of C_{RES}, R_{RES} so that the reset time is 200 µs or longer.

Figure 4 Reset Circuit

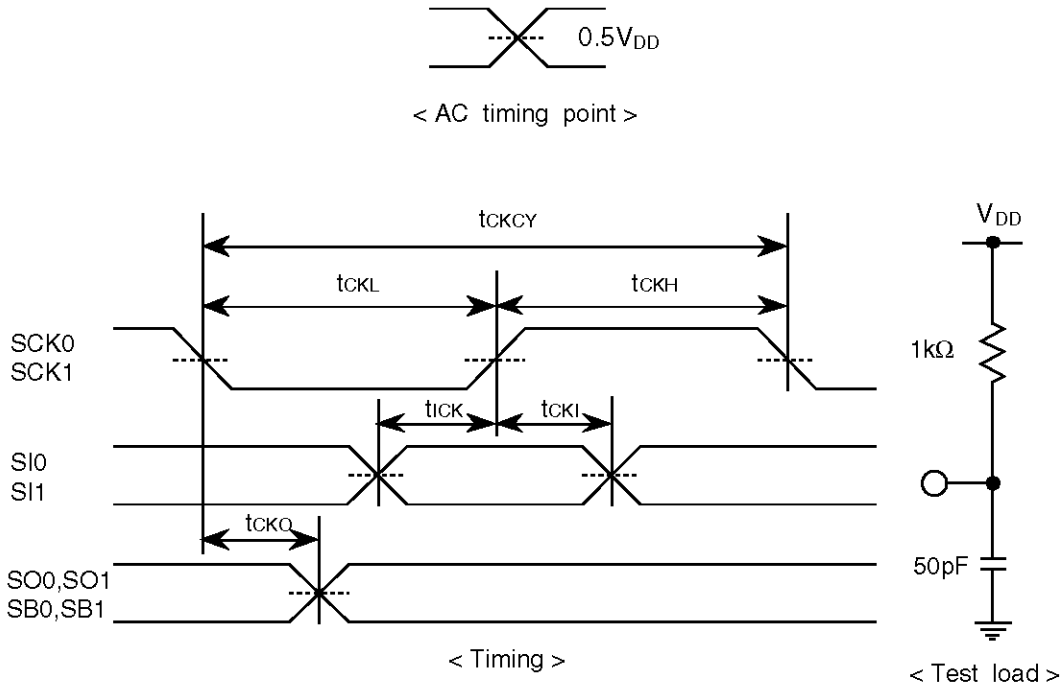


Figure 5 Serial Input/Output Test Conditions

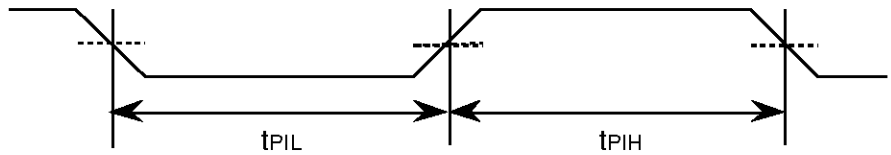


Figure 6 Pulse Input Timing Conditions