Data Sheet June 1999 File Number 3143.2

16-Channel, 8-Channel, Differential 8-Channel and Differential 4-Channel, CMOS Analog MUXs with Active Overvoltage Protection

The HI-506A, HI-507A, HI-508A and HI-509A are analog multiplexers with active overvoltage protection. Analog input levels may greatly exceed either power supply without damaging the device or disturbing the signal path of other channels. Active protection circuitry assures that signal fidelity is maintained even under fault conditions that would destroy other multiplexers. Analog inputs can withstand constant $70V_{P-P}$ levels with ±15V supplies. Digital inputs will also sustain continuous faults up to 4V greater than either supply. In addition, signal sources are protected from short circuiting should multiplexer supply loss occur. Each input presents 1kΩ of resistance under this condition. These features make the HI-506A, HI-507A, HI-508A and HI-509A ideal for use in systems where the analog inputs originate from external equipment, or separately powered circuitry. All devices are fabricated with 44V dielectrically isolated CMOS technology. The HI-506A is a single 16-Channel multiplexer, the HI-507A is an 8-Channel differential multiplexer, the HI-508A is a single 8-Channel multiplexer and the HI-509A is a differential 4-Channel multiplexer. If input overvoltage protection is not needed the HI-506/507/508/509 multiplexers are recommended. For further information see Application Notes AN520 and AN521.

Features

- Analog Overvoltage . . . . . $70V_{P-P}$
- No Channel Interaction During Overvoltage
- Maximum Power Supply 44V
- Fail Safe with Power Loss (No Latch-Up)
- Break-Before-Make Switching
- Analog Signal Range . . . . . ±15V
- Access Time 500ns
- Power Dissipation 7.5mW

Applications

- Data Acquisition Systems
- Industrial Controls
- Telemetry

Ordering Information

PART NUMBER	TEMP. RANGE (^oC)	PACKAGE	PKG. NO.
HI1-0506A-2	-55 to 125	28 Ld CERDIP	F28.6
HI1-0506A-5	0 to 75	28 Ld CERDIP	F28.6
HI1-0506A-8	-55 to 125 + 160 Hour Burn-In	28 Ld CERDIP	F28.6
HI3-0506A-5	0 to 75	28 Ld PDIP	E28.6
HI1-0507A-8	-55 to 125 + 160 Hour Burn-In	28 Ld CERDIP	F28.6
HI3-0507A-5	0 to 75	28 Ld PDIP	E28.6
HI1-0508A-7	0 to 75 + 96 Hour Burn-In	16 Ld CERDIP	F16.3
HI1-0508A-8	-55 to 125 + 160 Hour Burn-In	16 Ld CERDIP	F16.3
HI3-0508A-5	+0 to 75	16 Ld PDIP	E16.3
HI1-0509A-2	-55 to 125	16 Ld CERDIP	F16.3
HI1-0509A-5	0 to 75	16 Ld CERDIP	F16.3
HI1-0509A-8	-55 to 125 + 160 Hour Burn-In	16 Ld CERDIP	F16.3
HI3-0509A-5	0 to 75	16 Ld PDIP	E16.3

CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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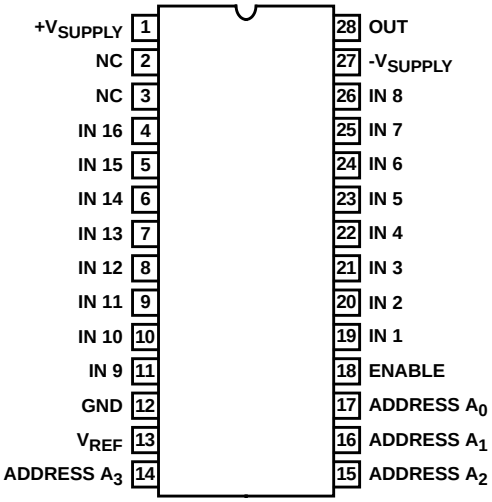
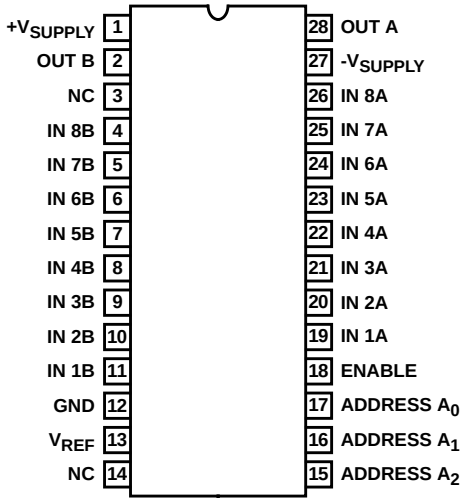
Pinouts

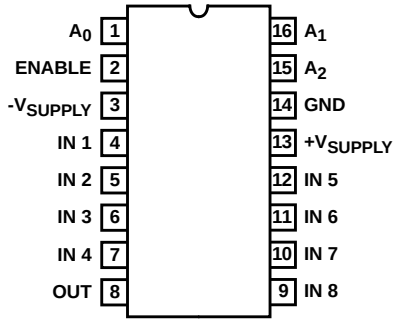
HI-506A (CERDIP, PDIP)
TOP VIEW



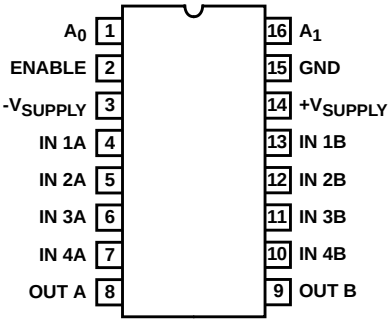
HI-507A (CERDIP, PDIP)
TOP VIEW



HI-508A (CERDIP, PDIP)
TOP VIEW



HI-509A (CERDIP, PDIP)
TOP VIEW



Truth Tables

HI-506A

A_3	A_2	A_1	A_0	EN	"ON" CHANNEL
X	X	X	X	L	None
L	L	L	L	H	1
L	L	L	H	H	2
L	L	H	L	H	3
L	L	H	H	H	4
L	H	L	L	H	5
L	H	L	H	H	6
L	H	H	L	H	7
L	H	H	H	H	8
H	L	L	L	H	9
H	L	L	H	H	10
H	L	H	L	H	11
H	L	H	H	H	12
H	H	L	L	H	13
H	H	L	H	H	14
H	H	H	L	H	15
H	H	H	H	H	16

HI-507A

A_2	A_1	A_0	EN	"ON" CHANNEL PAIR
X	X	X	L	None
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

HI-508A

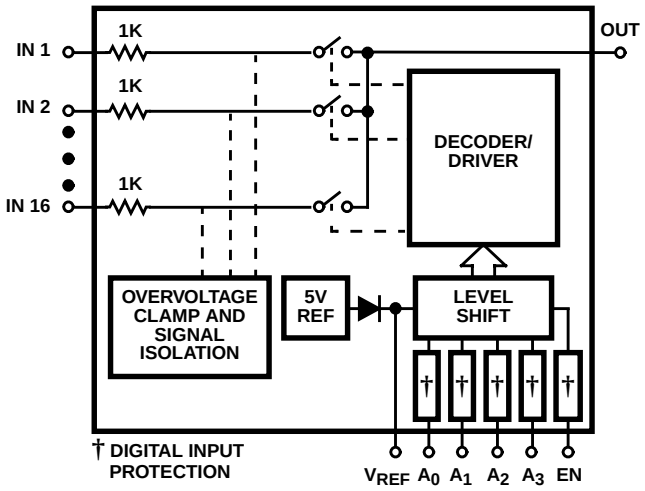
A_2	A_1	A_0	EN	"ON" CHANNEL
X	X	X	L	None
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

HI-509A

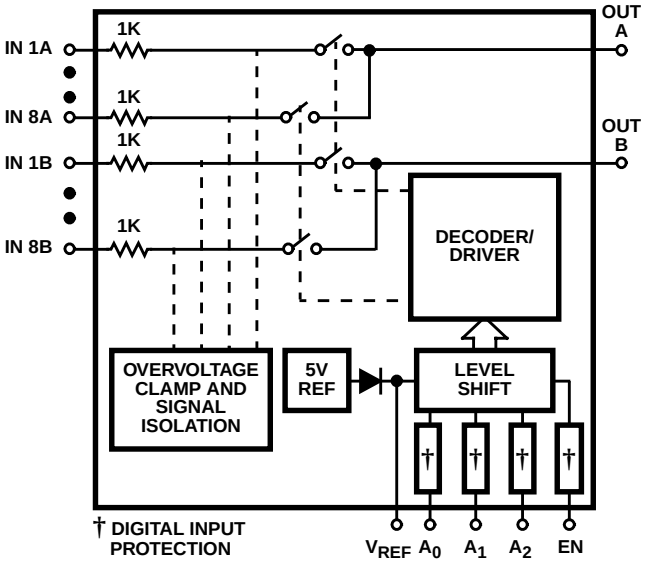
A_1	A_0	EN	"ON" CHANNEL PAIR
X	X	L	None
L	L	H	1
L	H	H	2
H	L	H	3
H	H	H	4

Functional Diagrams

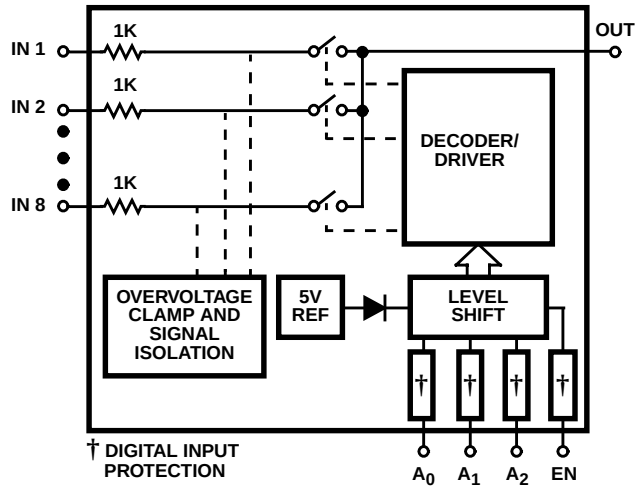
HI-506A



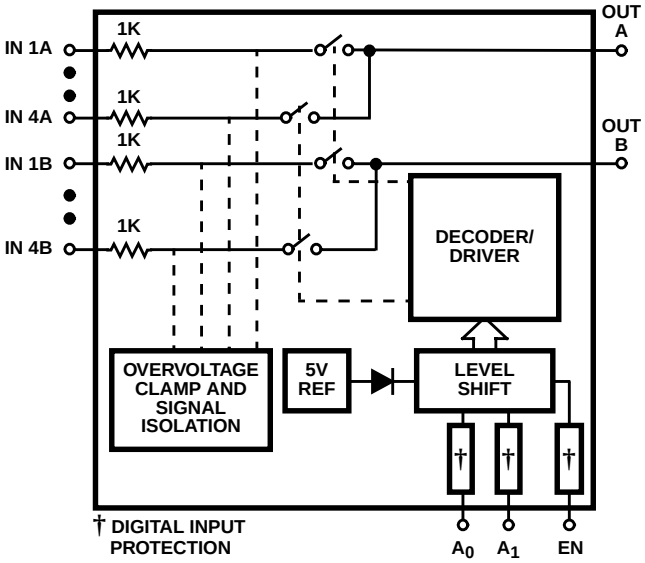
HI-507A



HI-508A

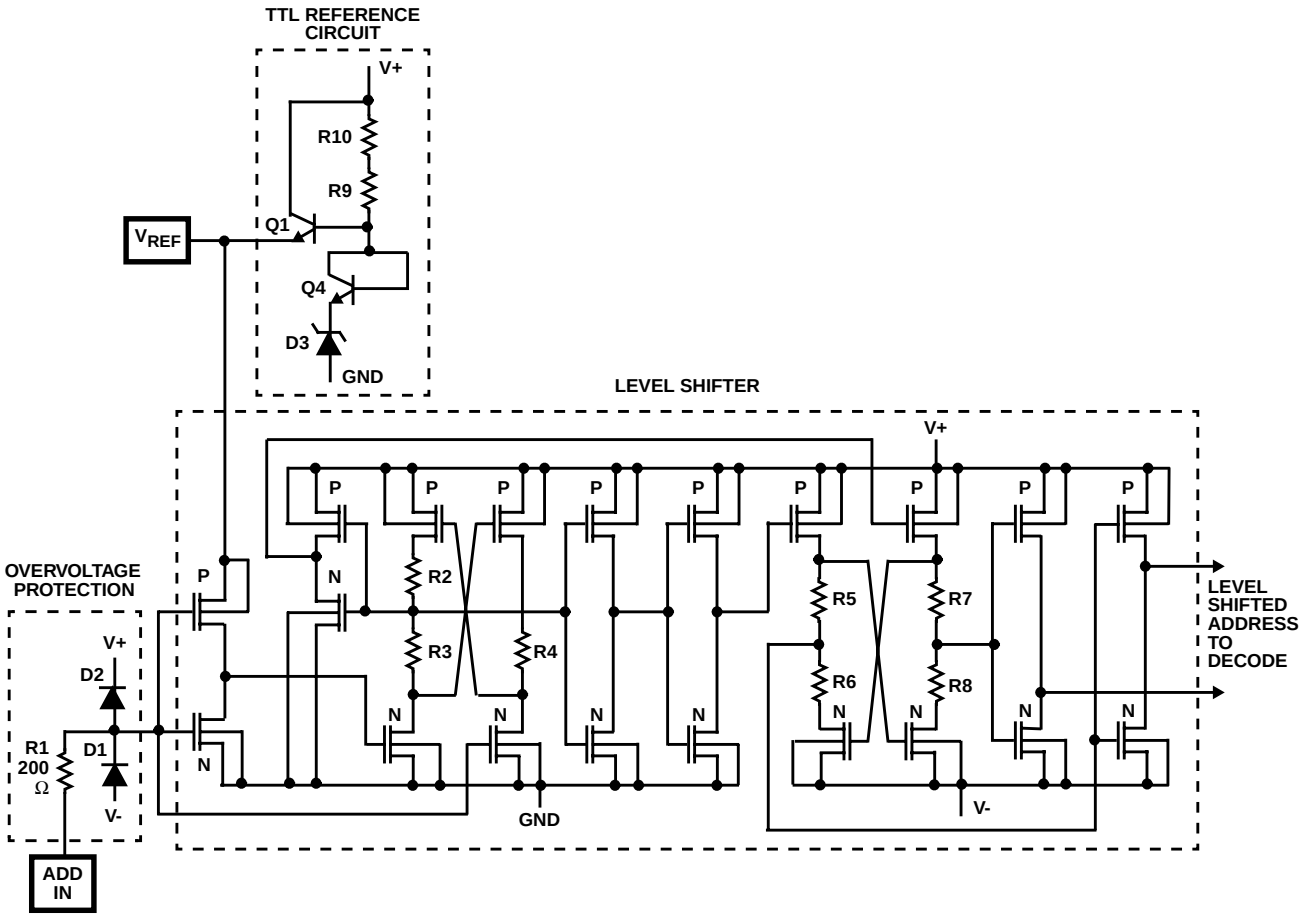


HI-509A

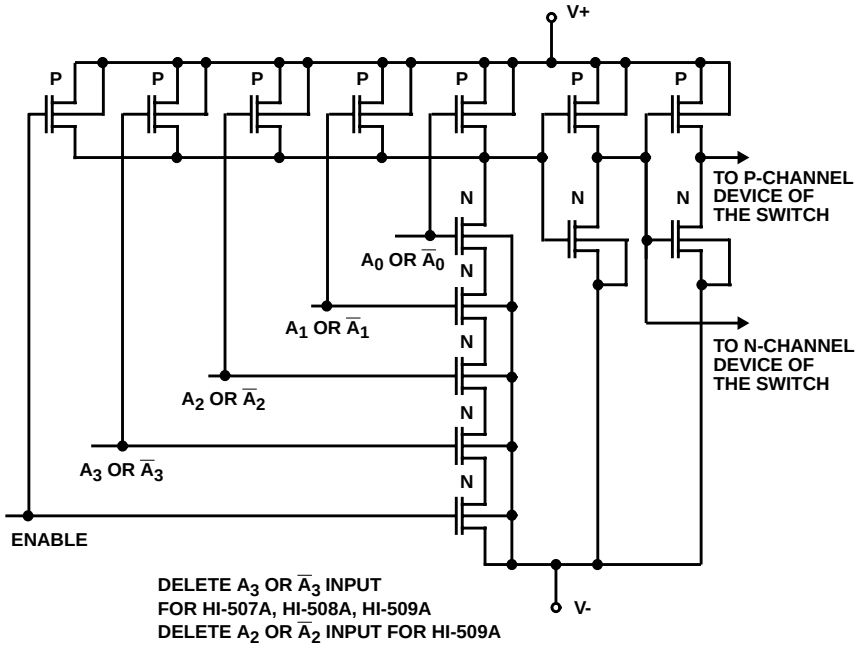


Schematic Diagrams

ADDRESS INPUT BUFFER AND LEVEL SHIFTER

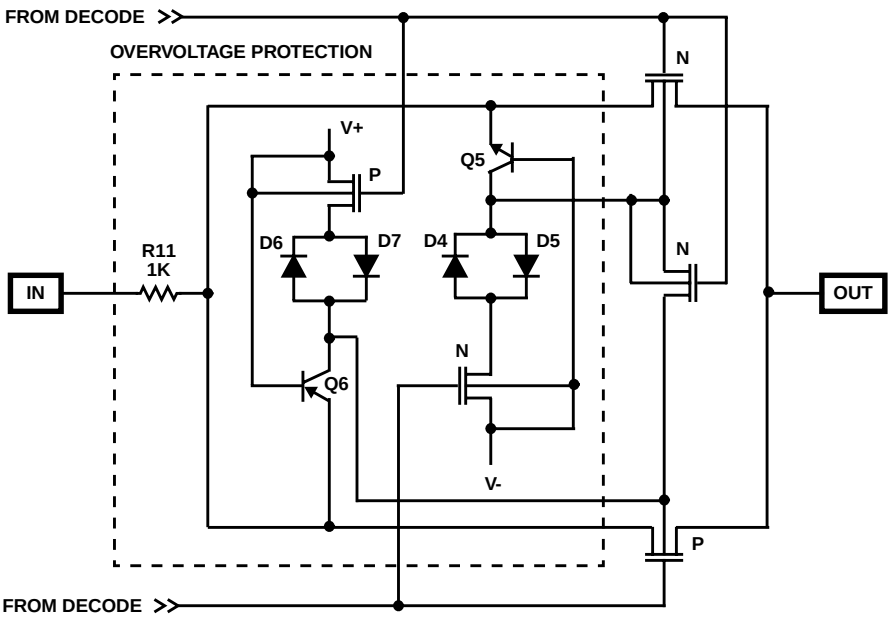


ADDRESS DECODER



Schematic Diagrams (Continued)

MULTIPLEX SWITCH



Absolute Maximum Ratings

V+ to V- . . . . . +44V
V+ to GND . . . . . +22V
V- to GND. . . . . -25V
Digital Input Voltage (V_{EN}, V_A) . . . . . (V-) -4V to (V+) +4V
or 20mA, Whichever Occurs First
Analog Signal (V_{IN}, V_{OUT}). . . . . (V-) -20V to (V+) +20V
Continuous Current, IN or OUT 20mA
Peak Current, IN or OUT, Pulsed 1ms, 10% Duty Cycle (Max). . 40mA

Operating Conditions

Temperature Ranges
HI-506A/507A/508A/509A-2, -8 . . . . . -55^oC to 125^oC
HI-506A/507A/508A/509A-5, -7 . . . . . 0^oC to 75^oC

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)	θ_{JC} ($^oC/W$)
28 Ld CERDIP Package	55	18
16 Ld CERDIP Package	85	32
28 Ld PDIP Package	60	N/A
16 Ld PDIP Package	90	N/A

Maximum Junction Temperature
CERDIP Packages . . . . . 175^oC
PDIP Packages . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

Supplies = +15V, -15V; V_{REF} Pin = Open; V_{AH} (Logic Level High) = 4V; V_{AL} (Logic Level Low) = 0.8V, Unless Otherwise Specified. For Test Conditions, Consult Test Circuits Section

PARAMETER	TEST CONDITIONS	TEMP (^oC)	-2, -8			-5, -7			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
DYNAMIC CHARACTERISTICS									
Access Time, t_A	Note 2	25	-	0.5	-	-	0.5	-	µs
		Full	-	-	1.0	-	-	1.0	µs
Break-Before-Make Delay, t_{OPEN}	Note 2	25	25	80	-	25	80	-	ns
Enable Delay (ON), $t_{ON(EN)}$	Note 2	25	-	300	500	-	300	-	ns
		Full	-	-	1000	-	-	1000	ns
Enable Delay (OFF), $t_{OFF(EN)}$	Note 2	25	-	300	500	-	300	-	ns
		Full	-	-	1000	-	-	1000	ns
Settling Time, t_S									
HI-506A and HI-507A	To 0.1%	25	-	1.2	-	-	1.2	-	µs
	To 0.01%	25	-	3.5	-	-	3.5	-	µs
HI-508A and HI-509A	To 0.1%	25	-	1.2	-	-	1.2	-	µs
	To 0.01%	25	-	3.5	-	-	3.5	-	µs
Off Isolation	Note 7	25	50	68	-	50	68	-	dB
Channel Input Capacitance, $C_{S(OFF)}$		25	-	10	-	-	10	-	pF
Channel Output Capacitance, $C_{D(OFF)}$									
HI-506A		25	-	52	-	-	52	-	pF
HI-507A		25	-	30	-	-	30	-	pF
HI-508A		25	-	25	-	-	25	-	pF
HI-509A		25	-	12	-	-	12	-	pF
Digital Input Capacitance, C_A		25	-	10	-	-	10	-	pF
Input to Output Capacitance, $C_{DS(OFF)}$		25	-	0.1	-	-	0.1	-	pF
DIGITAL INPUT CHARACTERISTICS									
Input Low Threshold, TTL Drive, V_{AL}	Note 2	Full	-	-	0.8	-	-	0.8	V
Input High Threshold, V_{AH} (Note 9)	Note 2	Full	4.0	-	-	4.0	-	-	V
Input Leakage Current (High or Low), I_A	Notes 2, 6	Full	-	-	1.0	-	-	1.0	µA

Electrical Specifications

Supplies = +15V, -15V; V_{REF} Pin = Open; V_{AH} (Logic Level High) = 4V; V_{AL} (Logic Level Low) = 0.8V, Unless Otherwise Specified. For Test Conditions, Consult Test Circuits Section **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP (^oC)	-2, -8			-5, -7			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
MOS Drive, V_{AL}, HI-506A/HI-507A	V_{REF} = +10V	25	-	-	0.8	-	-	0.8	V
MOS Drive, V_{AH}, HI-506A/HI-507A	V_{REF} = +10V	25	6.0	-	-	6.0	-	-	V
ANALOG CHANNEL CHARACTERISTICS									
Analog Signal Range, V_{IN}	Note 2	Full	-15	-	+15	-15	-	+15	V
On Resistance, r_{ON}	Notes 2, 3	25	-	1.2	1.5	-	1.5	1.8	kΩ
		Full	-	1.5	1.8	-	1.8	2.0	kΩ
Off Input Leakage Current, $I_{S(OFF)}$	Notes 2, 4	25	-	0.03	-	-	0.03	-	nA
		Full	-	-	50	-	-	50	nA
Off Output Leakage Current, $I_{D(OFF)}$	Notes 2, 4	25	-	0.1	-	-	0.1	-	nA
HI-506A		Full	-	-	300	-	-	300	nA
HI-507A		Full	-	-	200	-	-	200	nA
HI-508A		Full	-	-	200	-	-	200	nA
HI-509A		Full	-	-	100	-	-	100	nA
$I_{D(OFF)}$ With Input Overvoltage Applied	Note 5	25	-	4.0	-	-	4.0	-	nA
		Full	-	-	2.0	-	-	-	µA
On Channel Leakage Current, $I_{D(ON)}$	Notes 2, 4	25	-	0.1	-	-	0.1	-	nA
HI-506A		Full	-	-	300	-	-	300	nA
HI-507A		Full	-	-	200	-	-	200	nA
HI-508A		Full	-	-	200	-	-	200	nA
HI-509A		Full	-	-	100	-	-	100	nA
Differential Off Output Leakage Current, I_{DIFF}, (HI-507A, HI-509A Only)		Full	-	-	50	-	-	50	nA
POWER SUPPLY CHARACTERISTICS									
Current, I+	Notes 2, 8	Full	-	0.5	2.0	-	0.5	2.0	mA
Current, I-	Notes 2, 8	Full	-	0.02	1.0	-	0.02	1.0	mA
Power Dissipation, P_D		Full	-	7.5	-	-	7.5	-	mW

NOTES:

2. 100% tested for Dash 8. Leakage currents not tested at -55^oC.
3. V_{OUT} = ±10V, I_{OUT} = $\bar{+}$100µA.
4. 10nA is the practical lower limit for high speed measurement in the production test environment.
5. Analog Overvoltage = ±33V.
6. Digital input leakage is primarily due to the clamp diodes (see Schematic). Typical leakage is less than 1nA at 25^oC.
7. V_{EN} = 0.8V, R_L = 1K, C_L = 15pF, V_S = $7V_{RMS}$, f = 100kHz.
8. V_{EN}, V_A = 0V or 4V.
9. To drive from DTL/TTL Circuits, 1kΩ pull-up resistors to +5V supply are recommended.

Test Circuits and Waveforms

$T_A = 25^oC$, $V_{SUPPLY} = \pm15V$, $V_{AH} = 4V$, $V_{AL} = 0.8V$, V_{REF} = Open, Unless Otherwise Specified

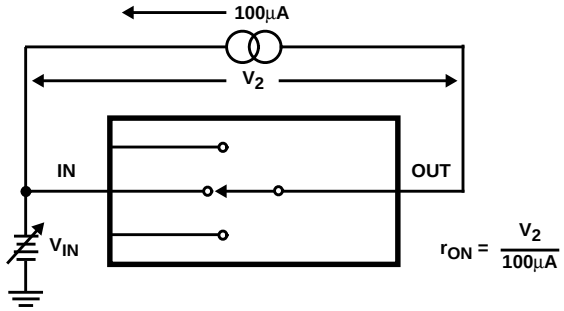


FIGURE 1A. TEST CIRCUIT

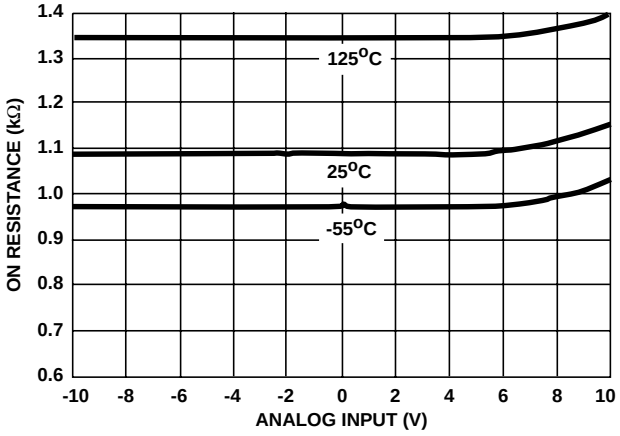


FIGURE 1B. ON RESISTANCE vs ANALOG INPUT VOLTAGE

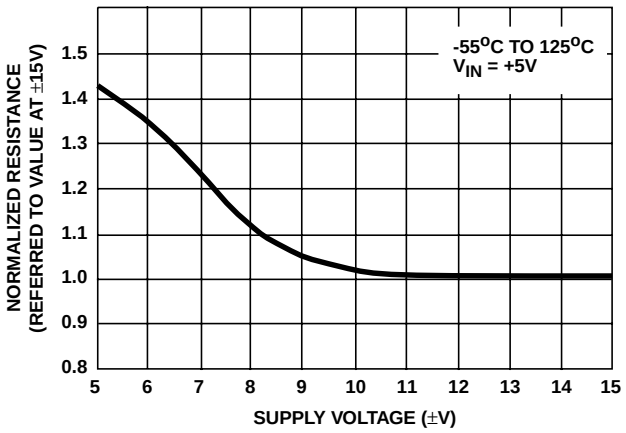


FIGURE 1C. NORMALIZED ON RESISTANCE vs SUPPLY VOLTAGE

FIGURE 1. ON RESISTANCE

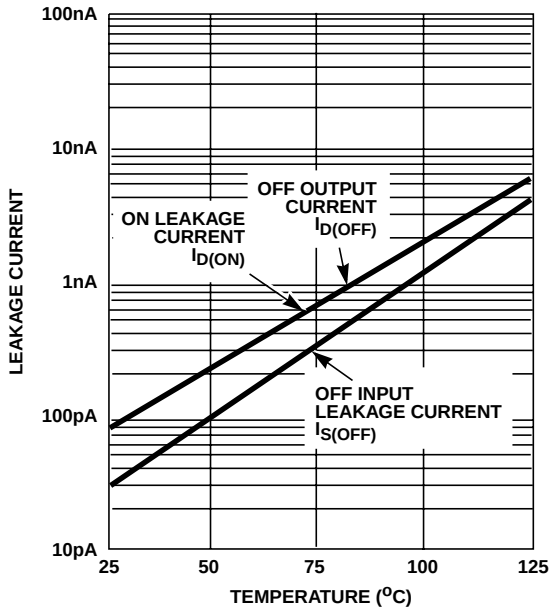


FIGURE 2A. LEAKAGE CURRENT vs TEMPERATURE

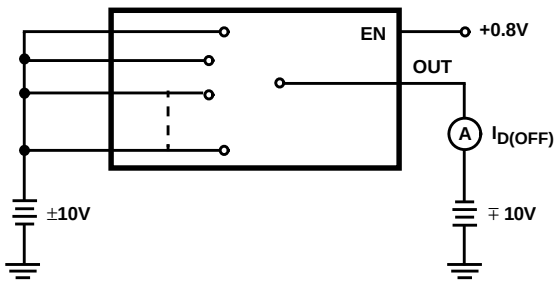


FIGURE 2B. $I_{D(OFF)}$ TEST CIRCUIT (NOTE 10)

Test Circuits and Waveforms

$T_A = 25^oC$, $V_{SUPPLY} = \pm15V$, $V_{AH} = 4V$, $V_{AL} = 0.8V$, V_{REF} = Open, Unless Otherwise Specified **(Continued)**

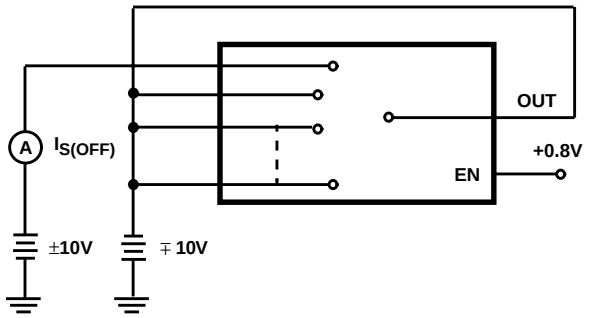


FIGURE 2C. $I_{S(OFF)}$ TEST CIRCUIT (NOTE 10)

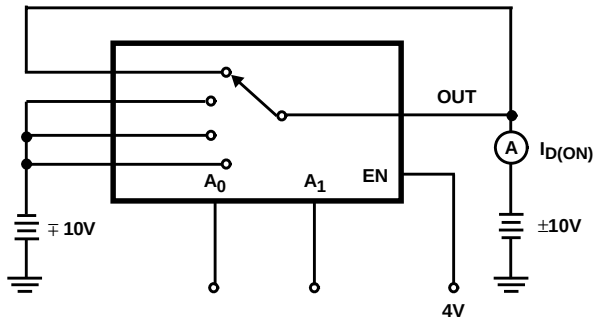


FIGURE 2D. $I_{D(On)}$ TEST CIRCUIT (NOTE 10)

NOTE:

10. Two measurements per channel: ±10V and ∓10V. (Two measurements per device for $I_{D(OFF)}$ ±10V and ∓10V.)

FIGURE 2. LEAKAGE CURRENTS

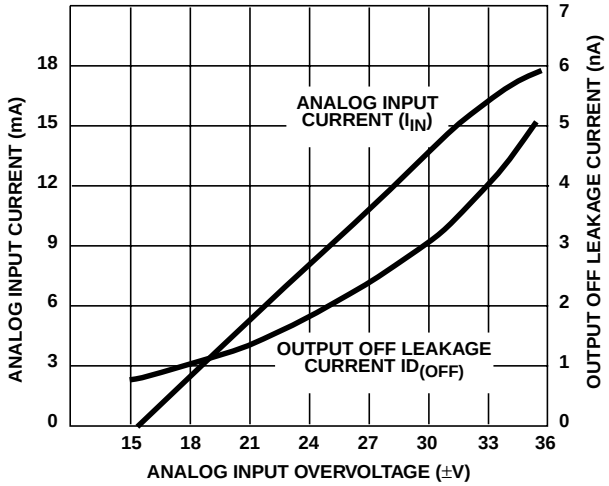


FIGURE 3A. ANALOG INPUT OVERVOLTAGE CHARACTERISTICS

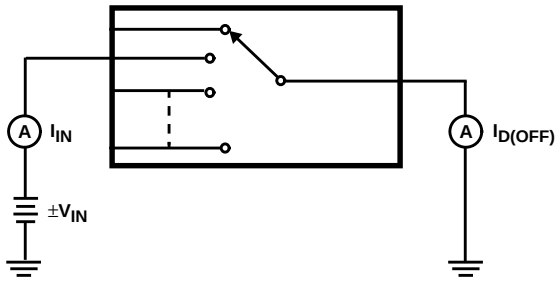


FIGURE 3B. TEST CIRCUIT

FIGURE 3. ANALOG INPUT OVERVOLTAGE CHARACTERISTICS

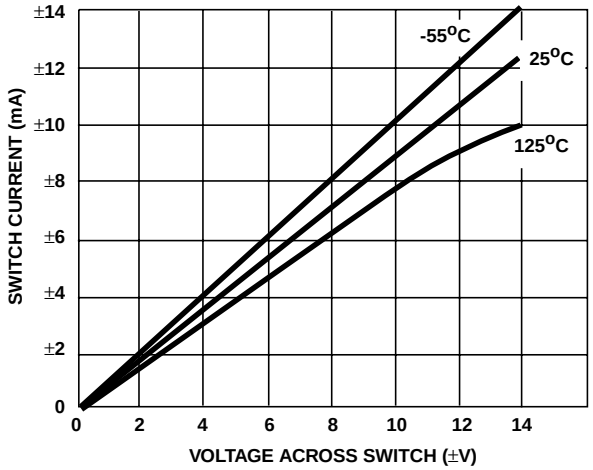


FIGURE 4A. ON CHANNEL CURRENT vs VOLTAGE

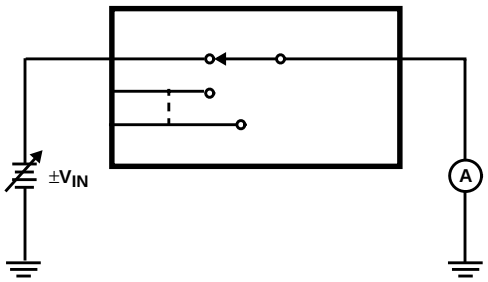


FIGURE 4B. TEST CIRCUIT

FIGURE 4. ON CHANNEL CURRENT

Test Circuits and Waveforms

$T_A = 25^oC$, $V_{SUPPLY} = \pm15V$, $V_{AH} = 4V$, $V_{AL} = 0.8V$, V_{REF} = Open, Unless Otherwise Specified **(Continued)**

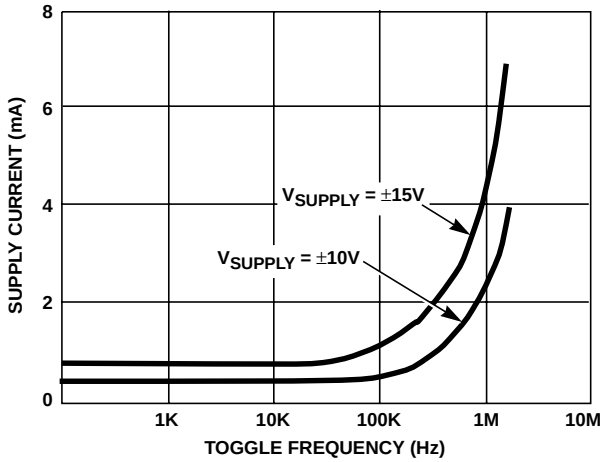
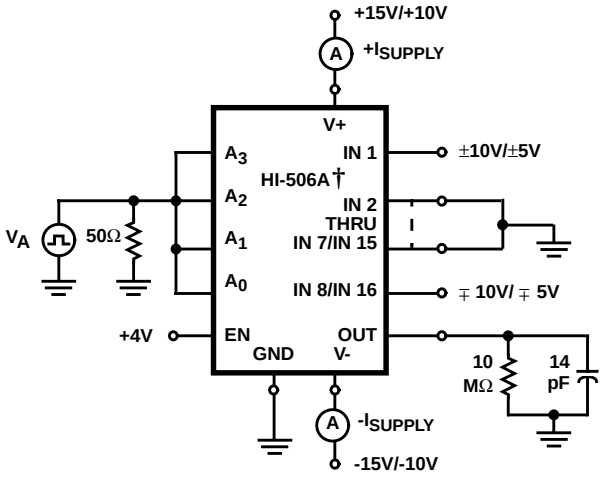


FIGURE 5A. SUPPLY CURRENT vs TOGGLE FREQUENCY



†Similar connection for HI-507A/HI-508A/HI-509A

FIGURE 5B. TEST CIRCUIT

FIGURE 5. DYNAMIC SUPPLY CURRENT

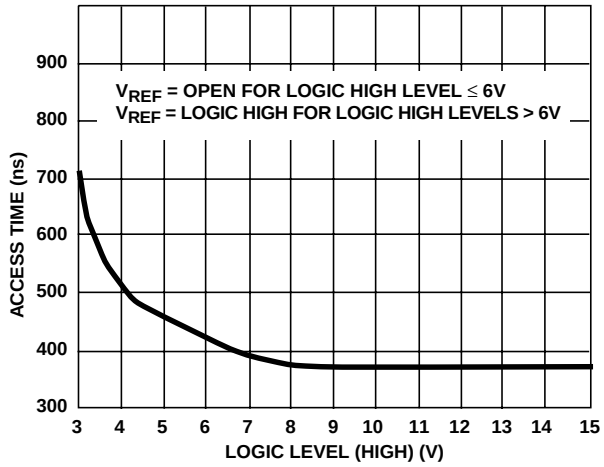
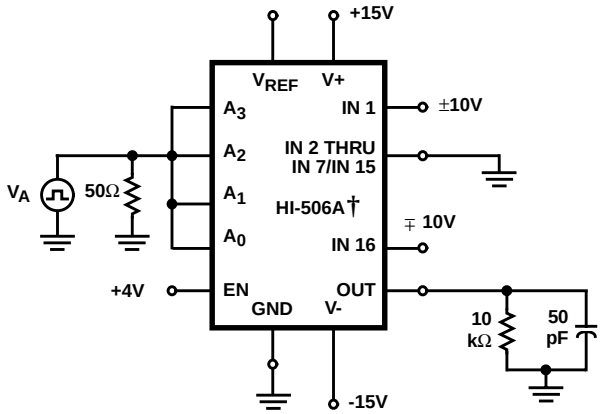


FIGURE 6A. ACCESS TIME vs LOGIC LEVEL (HIGH)



†Similar connection for HI-507A/HI-580A/HI-509A

FIGURE 6B. TEST CIRCUIT

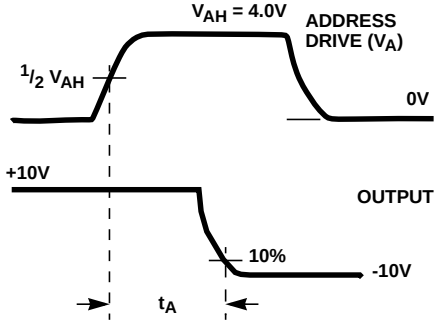


FIGURE 6C. MEASUREMENT POINTS

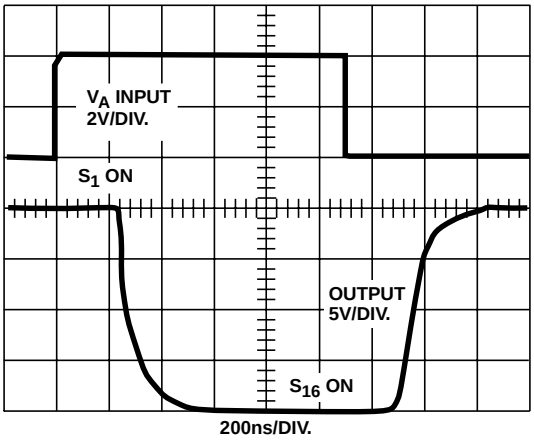
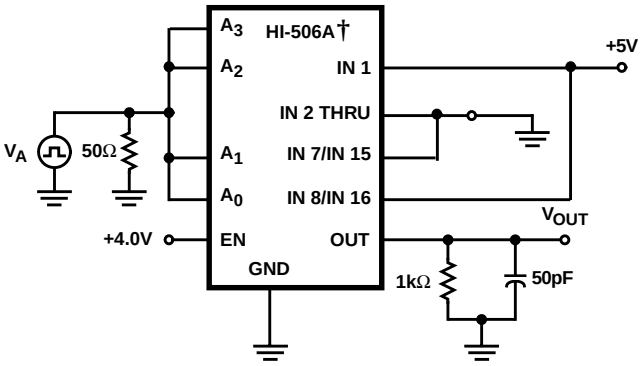


FIGURE 6D. WAVEFORMS

FIGURE 6. ACCESS TIME

Test Circuits and Waveforms

$T_A = 25^oC$, $V_{SUPPLY} = \pm15V$, $V_{AH} = 4V$, $V_{AL} = 0.8V$, V_{REF} = Open, Unless Otherwise Specified **(Continued)**



†Similar connection for HI-507A/HI-508A/HI-509A

FIGURE 7A. TEST CIRCUIT

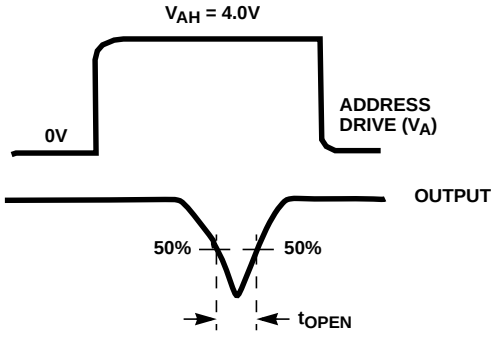


FIGURE 7B. MEASUREMENT POINTS

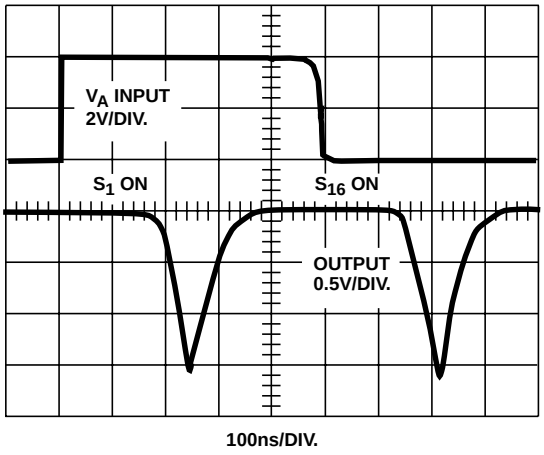
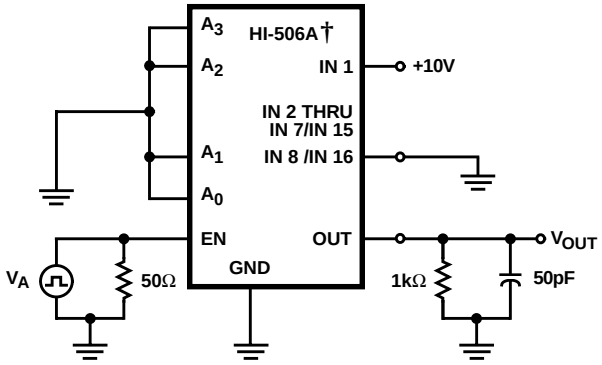


FIGURE 7C. WAVEFORMS

FIGURE 7. BREAK-BEFORE-MAKE DELAY

Test Circuits and Waveforms

$T_A = 25^oC$, $V_{SUPPLY} = \pm15V$, $V_{AH} = 4V$, $V_{AL} = 0.8V$, V_{REF} = Open, Unless Otherwise Specified **(Continued)**



†Similar connection for HI-507A//HI-508A/HI-509A

FIGURE 8A. TEST CIRCUIT

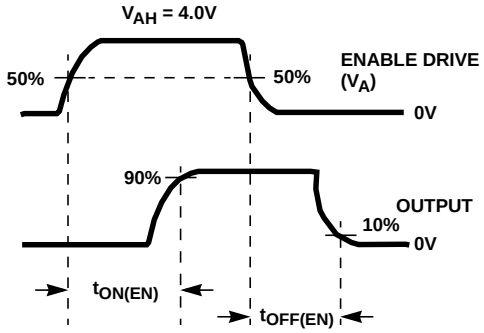


FIGURE 8B. MEASUREMENT POINTS

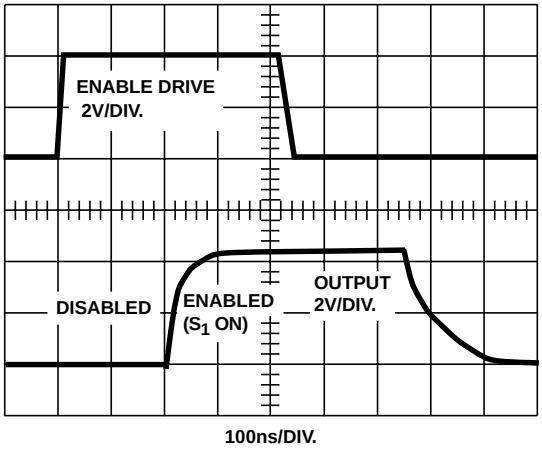


FIGURE 8C. WAVEFORMS

FIGURE 8. ENABLE DELAYS

Die Characteristics

DIE DIMENSIONS:

159 mils x 83.9 mils

METALLIZATION:

Type: CuAl
Thickness: 16kÅ ±2kÅ

SUBSTRATE POTENTIAL (NOTE):

$-V_{SUPPLY}$

PASSIVATION:

Silox: 12kÅ ±2kÅ
Nitride: 3.5kÅ ±1kÅ

WORST CASE CURRENT DENSITY:

1.4×10^5 A/cm^2

TRANSISTOR COUNT:

485

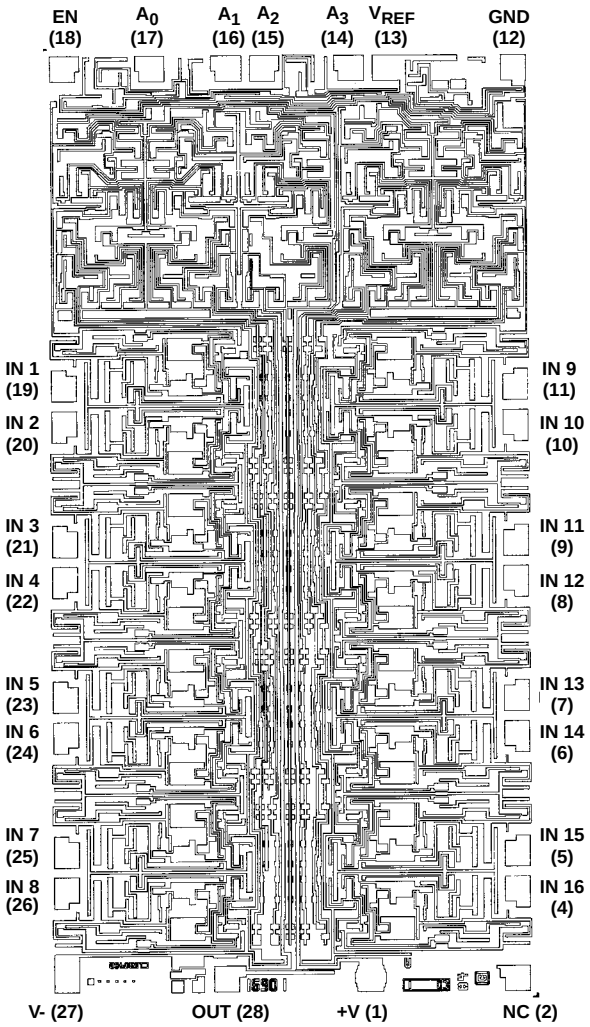
PROCESS:

CMOS-DI

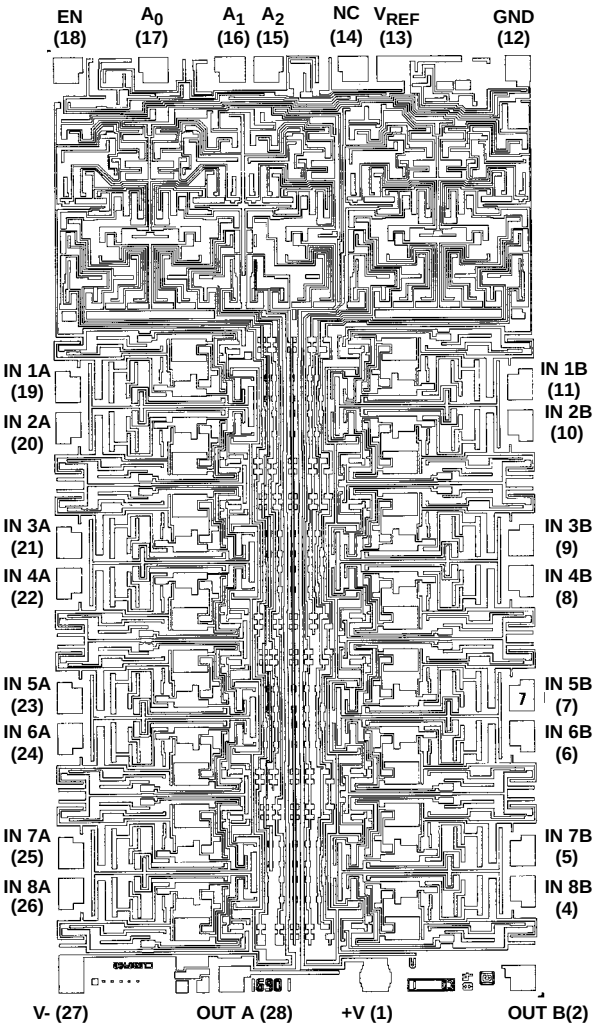
NOTE: The substrate appears resistive to the $-V_{SUPPLY}$ terminal, therefore it may be left floating (Insulating Die Mount) or it may be mounted on a conductor at $-V_{SUPPLY}$ potential.

Metallization Mask Layouts

HI-506A



HI-507A



Die Characteristics

DIE DIMENSIONS:

108 mils x 83 mils

METALLIZATION:

Type: CuAl
Thickness: 16kÅ ±2kÅ

SUBSTRATE POTENTIAL (NOTE):

$-V_{SUPPLY}$

PASSIVATION:

Silox: 12kÅ ±2kÅ
Nitride: 3.5kÅ ±1kÅ

WORST CASE CURRENT DENSITY:

1.4×10^5 A/cm^2

TRANSISTOR COUNT:

253

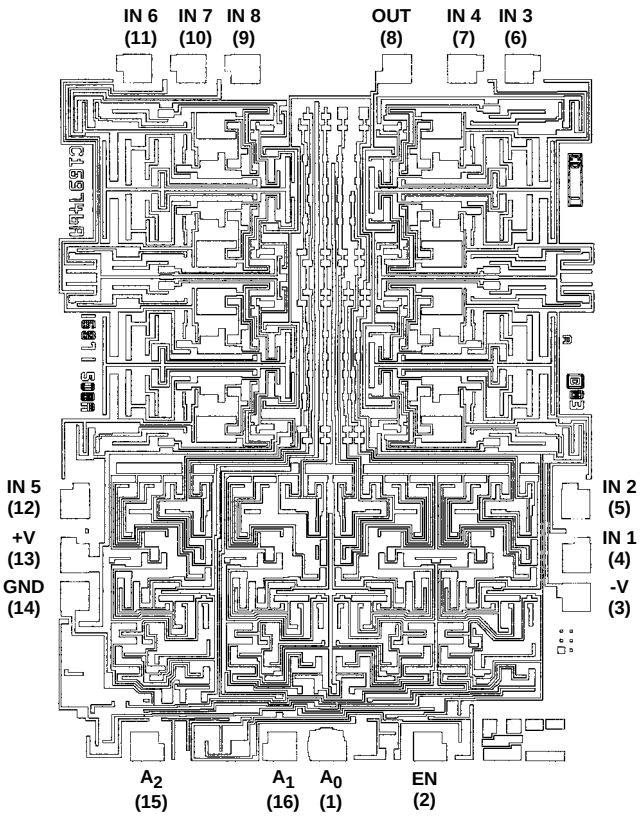
PROCESS:

CMOS-DI

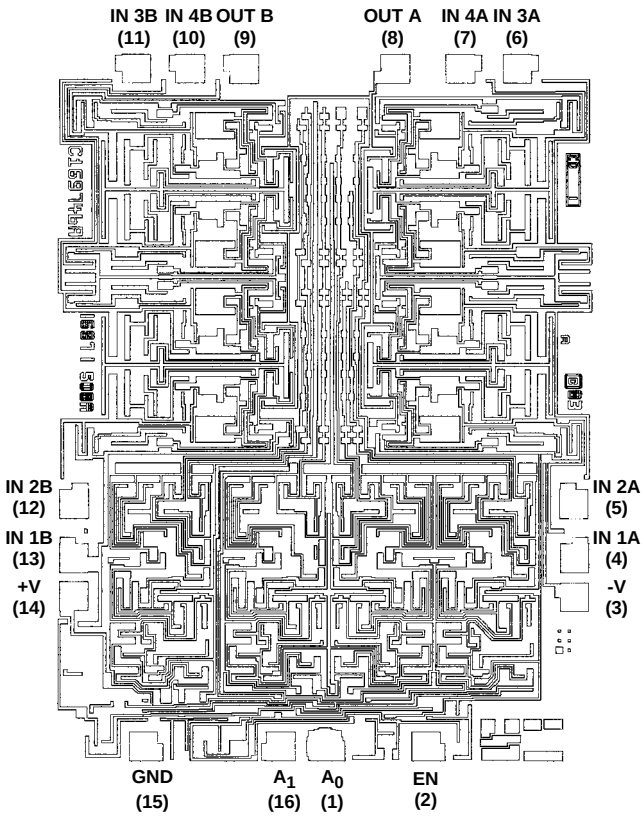
NOTE: The substrate appears resistive to the $-V_{SUPPLY}$ terminal, therefore it may be left floating (Insulating Die Mount) or it may be mounted on a conductor at $-V_{SUPPLY}$ potential.

Metallization Mask Layouts

HI-508A



HI-509A



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