HARRIS Semiconductor

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or email: centapp@harris.com

HC-55564

Continuously Variable Slope Delta-Modulator (CVSD)

February 1999

Features

- **All Digital**
- **Requires Few External Parts**
- **Low Power Drain: 1.5mW Typical From Single 4.5V To 6V Supply**
- **Time Constants Determined by Clock Frequency; No Calibration or Drift Problems: Automatic Offset Adjustment**
- **Half Duplex Operation Under Digital Control**
- **Filter Reset Under Digital Control**
- **Automatic Overload Recovery**
- **Automatic "Quiet" Pattern Generation**
- **AGC Control Signal Available**

Applications

- **Voice Transmission Over Data Channels (Modems)**
- **Voice/Data Multiplexing (Pair Gain)**
- **Voice Encryption/Scrambling**
- **Voicemail**
- **Audio Manipulations: Delay Lines, Time Compression, Echo Generation/Suppression, Special Effects, etc.**
- **Pagers/Satellites**
- **Data Acquisition Systems**
- **Voice I/O for Digital Systems and Speech Synthesis Requiring Small Size, Low Weight, and Ease of Reprogrammability**
- **Related Literature**
  - **AN607, Delta Modulation for Voice Transmission**

Description

The HC-55564 is a half duplex modulator/demodulator CMOS intergrated circuit used to convert voice signals into serial NRZ digital data and to reconvert that data into voice. The conversion is by delta-modulation, using the Continuously Variable Slope (CVSD) method of modulation/demodulation.

While the signals are compatible with other CVSD circuits, the internal design is unique. The analog loop filters have been replaced by very low power digital filters which require no external timing components. This approach allows inclusion of many desirable features which would be difficult to implement using other approaches.

The fundamental advantages of delta-modulation, along with its simplicity and serial data format, provide an efficient (low data rate/low memory requirements) method for voice digitization.

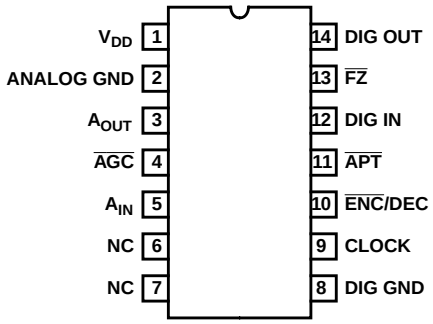
The HC-55564 is usable from 9kbits/s to above 64kbps. See the Harris Military databook for a MIL-STD-883C compliant CVSD. Application Note 607.

Ordering Information

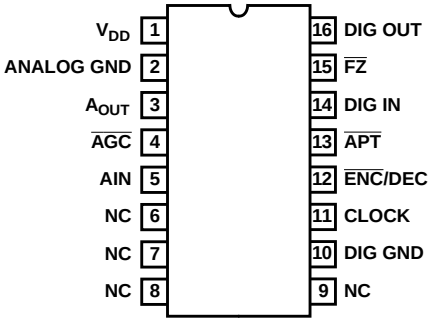
PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
HC1-55564-2	-55 to 125	14 Ld CERDIP	F14.3
HC1-55564-5	0 to 75	14 Ld CERDIP	F14.3
HC1-55564-9	-40 to 85	14 Ld CERDIP	F14.3
HC3-55564-5	0 to 75	14 Ld PDIP	E14.3
HC9P55564-5	0 to 75	16 Ld Plastic SOIC (W)	M16.3

Pinouts

HC-55564
(PDIP, CERDIP)
TOP VIEW



HC-55564
(SOIC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **2889.5**

Absolute Maximum Ratings

Voltage at Any Pin . . . . . GND -0.3V to V_{DD} 0.3V
Maximum V_{DD} Voltage 7.0V
Junction Temperature . . . . . 175^{o}C

Operating Conditions

Temperature Range
HC-55564-5, -7 . . . . . 0^{o}C to 75^{o}C
HC-55564-9 . . . . . -40^{o}C to 85^{o}C
HC-55564-2 . . . . . -55^{o}C to 125^{o}C
Operating V_{DD} . . . . . 4.5V to 6.0V

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (^{o}C/W)
CERDIP Package	70
PDIP Package	85
SOIC Package	98

Maximum Junction Temperature (Plastic Package) . . . . . 150^{o}C
Maximum Storage Temperature Range . . . . . -65^{o}C to 150^{o}C
Maximum Lead Temperature (Soldering 10s) . . . . . 300^{o}C

Die Characteristics

Transistor Count 1897
Die Dimensions . . . . . 147 x 82
Substrate Potential . . . . . +V_{DD}
Process . . . . . BiMOSE

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

Unless Otherwise Specified, typical parameters are at 25^{o}C, Min-Max are over operating temperature ranges. V_{DD} = 5.0V, Sampling Rate = 16Kbps, AG = DG = 0V, A_{IN} = 1.2V_{RMS}

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Sampling Rate	CLK	Note 2	9	16	64	kbps
Supply Current	I_{DD}		-	0.3	1.5	mA
Logic '1' Input	V_{IH}	Note 3	3.5	-	-	V
Logic '0' Input	V_{IL}	Note 3	-	-	1.5	V
Logic '1' Output	V_{OH}	Note 4	4.0	-	-	V
Logic '0' Output	V_{OL}	Note 4	-	-	0.4	V
Clock Duty Cycle			30	-	70	%
Audio Input Voltage	A_{IN}	AC Coupled (Note 5)	-	0.5	1.2	V_{RMS}
Audio Output Voltage	A_{OUT}	AC Coupled (Note 6)	-	0.5	1.2	V_{RMS}
Audio Input Impedance	Z_{IN}	Note 7	-	280	-	kΩ
Audio Output Impedance	Z_{OUT}	Note 7	-	150	-	kΩ
Transfer Gain	A_{E-D}	No Load, Audio In to Audio Out.	-2.0	-	+2.0	dB
Syllabic Filter Time Constant	t_{SF}	Note 8	-	4.0	-	ms
Signal Estimate Filter Time Constant	t_{SE}	Note 8	1.0	-	-	ms
Enc Threshold		AIN at 100Hz (Note 9), (Typ) 0.3% = 15mV_{RMS}	-	6	-	mV_{PEAK}
Minimum Step Size	MSS	Note 10	-	0.1	-	$\%V_{DD}$
Quieting Pattern Amplitude	V_{QP}	$\overline{FZ}$ = 0V or $\overline{APT}$ = 0V (Note 11)	-	10	-	mV_{P-P}
AGC Threshold	V_{ATH}	Note 12	-	0.1	-	F.S.
Clamping Threshold	V_{CTH}	Note 13	-	0.75	-	F.S.

NOTES:

2. There is one NRZ (Non-Return Zero) data bit per clock period. Data is clocked out on the negative clock edge. Data is clocked into the CVSD on the positive going edge (see Figure 2). Clock may be run at less than 9kbps and greater than 64kbps.
3. Logic inputs are CMOS compatible at supply voltage and are diode protected. Digital data input is NRZ at clock rate.
4. Logic outputs are CMOS compatible at supply voltage and will withstand short-circuits to V_{DD} or ground. Digital data output is NRZ and changes with negative clock transitions. Each output will drive one LS TTL load.
5. Recommended voice input range for best voice performance. Should be externally AC coupled.
6. May be used for side-tone in encode mode. Should be externally AC coupled. Varies with audio input level by ±2dB.
7. Presents series impedance with audio signal. Zero signal reference is approximately $V_{DD}/2$.
8. Note that filter time constants are inversely proportional to clock rate. Both filters approximate single pole responses.
9. The minimum audio input voltage above which encoding takes place.
10. The minimum audio output voltage change that can be produced by the internal DAC.
11. Settled value, the "quieting" pattern or idle-channel audio output steps at one-half the bit rate, changing state on negative clock transitions.
12. A logic "0" will appear at the AGC output pin when the recovered signal reaches one-half of full-scale value (positive or negative), i.e., at $V_{DD}/2$ ±25% of V_{DD}.
13. The recovered signal will be clamped, and the computation will be inhibited, when the recovered signal reaches three-quarters of full-scale value, and will unclamp when it falls below this value (positive or negative).

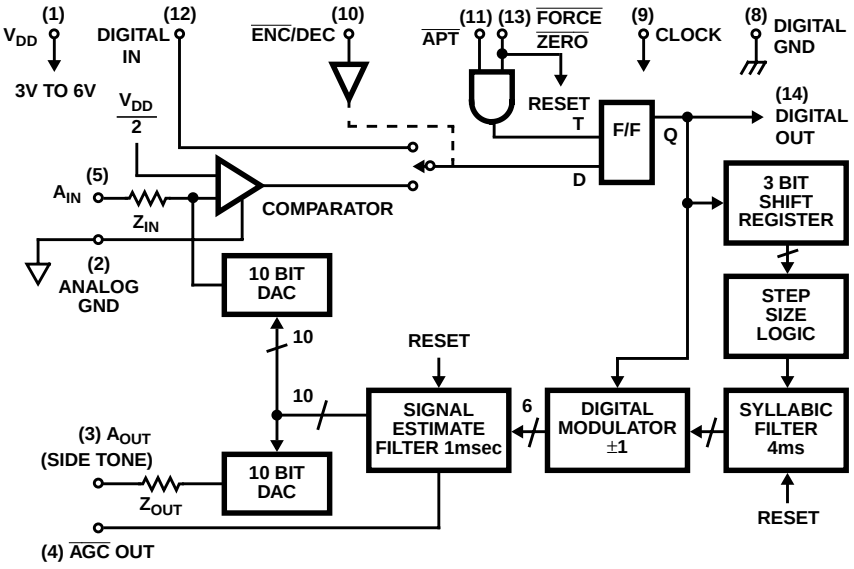
Pin Descriptions

PIN NUMBER 14 LEAD DIP	SYMBOL	DESCRIPTION
1	V_{DD}	Positive Supply Voltage. Voltage range is 4.5V to 6.0V.
2	Analog GND	Analog Ground connection to D/A ladders and comparator.
3	A_{OUT}	Audio Out recovered from 10-bit DAC. May be used as side tone at the transmitter. Presents approximately 150kΩ source with DC offset of $V_{DD}/2$. Within ±2dB of Audio Input. Should be externally AC coupled.
4	$\overline{AGC}$	Automatic Gain Control output. A logic low level will appear at this output when the recovered signal excursion reaches one-half of full scale value. In each half cycle full scale is $V_{DD}/2$. The mark-space ratio is proportional to the average signal level.
5	A_{IN}	Audio Input to comparator. Should be externally AC coupled. Presents approximately 280kΩ in series with $V_{DD}/2$.
6, 7	NC	No internal connection is made to these pins.
8	Digital GND	Logic ground. 0V reference for all logic inputs and outputs.
9	Clock	Sampling rate clock. In the decode mode, must be synchronized with the digital input data such that the data is valid at the positive clock transition. In the encode mode, the digital data is clocked out on the negative going clock transition. The clock rate equals the data rate.
10	$\overline{Encode}$/ Decode	A single CVSD can provide half-duplex operation. The encode or decode function is selected by the logic level applied to this input. A low level selects the encode mode, a high level the decode mode.
11	$\overline{APT}$	Alternate Plain Text input. Activating this input caused a digital quieting pattern to be transmitted, however; internally the CVSD is still functional and a signal is still available at the A_{OUT} port. Active low.
12	Digital In	Input for the received digital NRZ data.
13	$\overline{FZ}$	Force Zero input. Activating this input resets the internal logic and forces the digital output and the recovered audio output into the “quieting” condition. An alternating 1-0 pattern appears at the digital output at 1/2 the clock rate. When this is decoded by a receive CVSD, a $10mV_{P-P}$ inaudible signal appears at audio output. Active low.
14	Digital Out	Output for transmitted digital NRZ data.

NOTE:

14. No active input should be left in a “floating condition.”

Functional Diagram (DIP Pin Numbers Shown)



Timing Waveforms

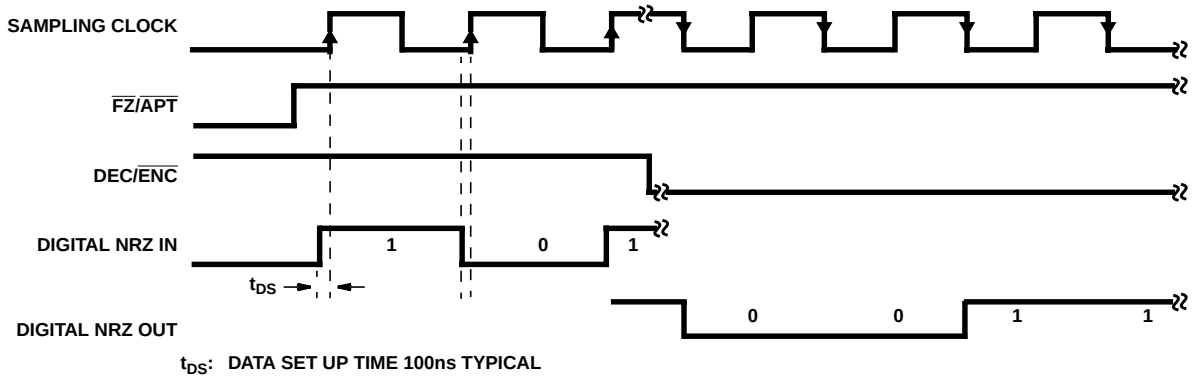
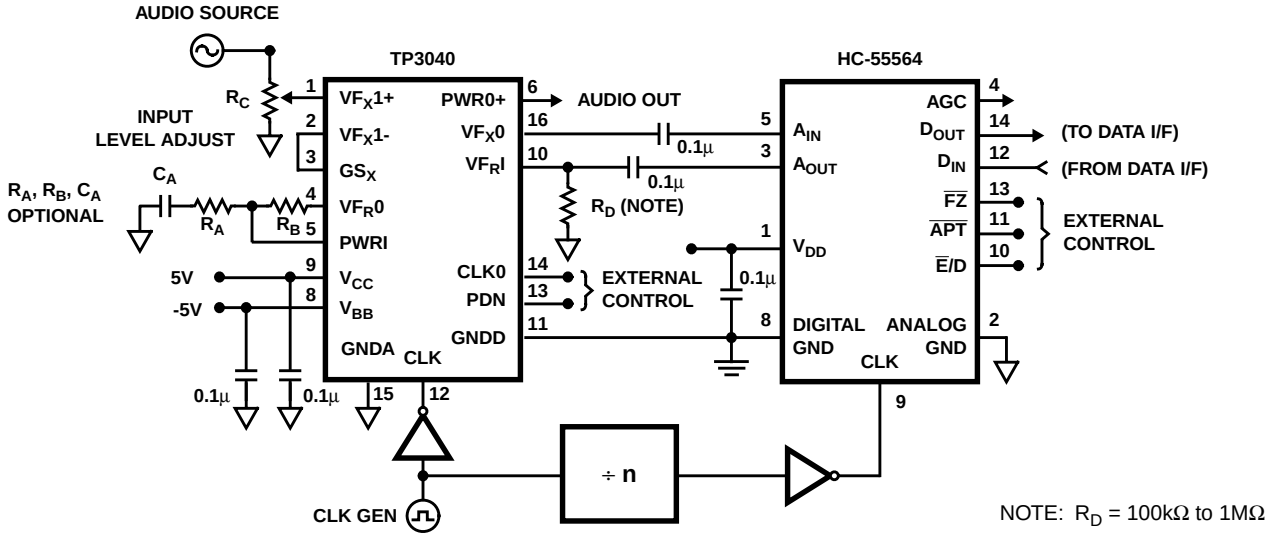


FIGURE 2. CVSD TIMING DIAGRAM

Interface Circuit for HC-55564 CVSD (DIP Pin Numbers Shown)

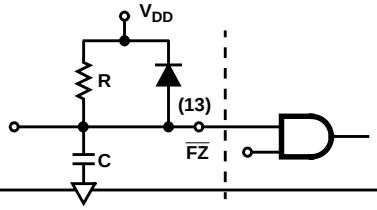


CVSD Hookup for Evaluation

The circuit in Figure 3 is sufficient to evaluate the voice quality of the CVSD, since when encoding, the feedback signal at the audio output pin is the reconstructed audio input signal.

CVSD design considerations are as follows:

1. Care should be taken in layout to maintain isolation between analog and digital signal paths for proper noise consideration.
2. Power supply decoupling is necessary as close to the device as possible. A 0.1µF should be sufficient.
3. Ground, then power, must be present before any input signals are applied to the CVSD. Failure to observe this may cause a latchup condition which may be destructive. Latchup may be removed by cycling the power off/on. A power-up reset circuit may be used that strobes Force Zero (Pin 13) during power-up as follows:
4. Analog (signal) ground (Pin 2) should be externally tied to Digital GND (Pin 8) and power supply ground. It is recommended that the A_{IN} and A_{OUT} ground returns connect only to Pin 2.
5. Digital inputs and outputs are compatible with standard CMOS logic using the same supply voltage. All unused logic inputs must be tied to the appropriate logic level for desired operation. It is recommended that unused inputs tied high be done so through a pull-up resistor (1kΩ to 10kΩ). TTL outputs will require 1kΩ pull-up resistors. Pins 4 and 14 will each drive CMOS logic or one low power TTL input.
6. Since the Audio Out pins are internally DC biased to $V_{DD}/2$, AC coupling is required. In general, a value of 0.1µF is sufficient for AC coupling of the CVSD audio pins to a filter circuit.
7. The AGC output may be externally integrated to drive an AGC pre-amp, or it could drive an LED indicator through a buffer to indicate proper speaking volume.



Figures 4, 5, and 6 illustrate the typical frequency response of the HC-55564 for varying input levels and for varying sampling rates. To prevent slope overload (slew limiting), the 0dB boundary should not be exceeded. The frequency response is directly proportional to the sampling clock rate. The flat bandwidth at 0dB doubles for every doubling in sampling rate. The output levels were measured in the encode mode, without filtering, from A_{IN} to A_{OUT}, at V_{DD} = 5V. 0dB = 1.2V_{RMS}.

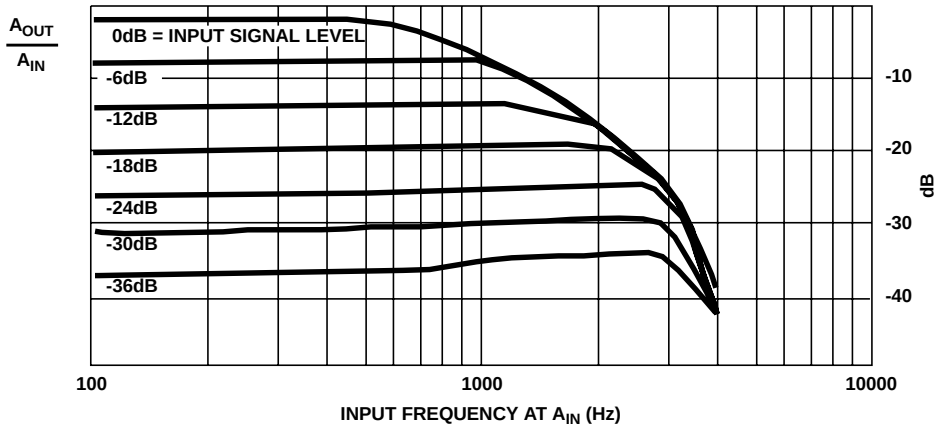


FIGURE 4. 16kbps

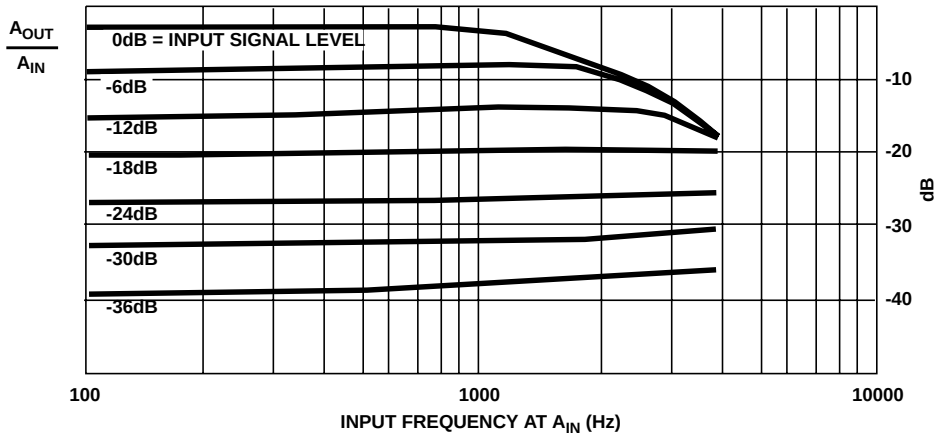


FIGURE 5. 32kbps

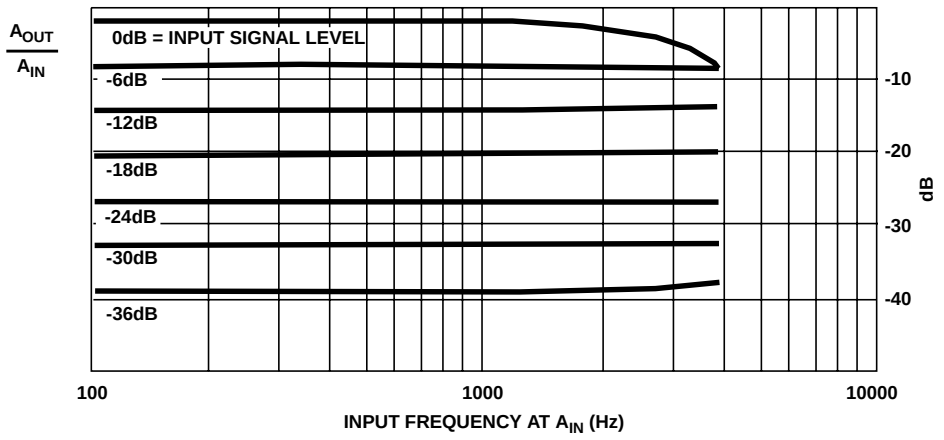


FIGURE 6. 64kbps

The following typical performance distortion graphs were realized with the test configuration of Figure 7. The measurement vehicle for Total Harmonic Distortion (THD) was an HP-339A distortion measurement set, and for 2nd and 3rd harmonic distortion, an HP-3582A spectrum analyzer. All measurement conditions were at V_{DD} = 5V, and 2nd and 3rd harmonic distortion measurements were C-message filtered. 0dB = 1.2V_{RMS}.

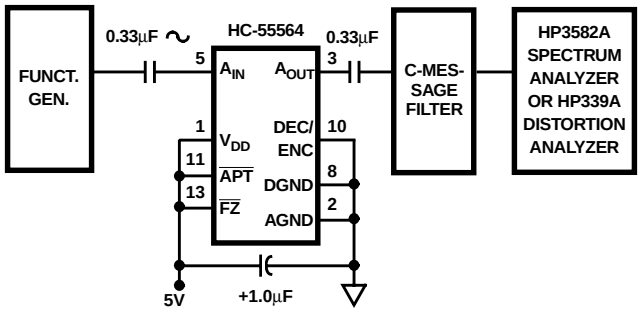


FIGURE 7. TEST AND MEASUREMENT CIRCUIT

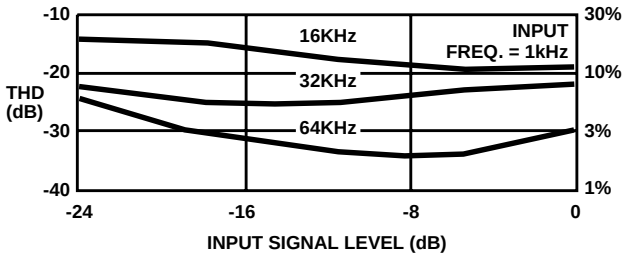


FIGURE 8. CVSD SIGNAL LEVEL vs TOTAL HARMONIC DISTORTION

CVSD INPUT LEVEL vs 2ND AND 3RD HARMONIC DISTORTION
C-MESSAGE WEIGHTED

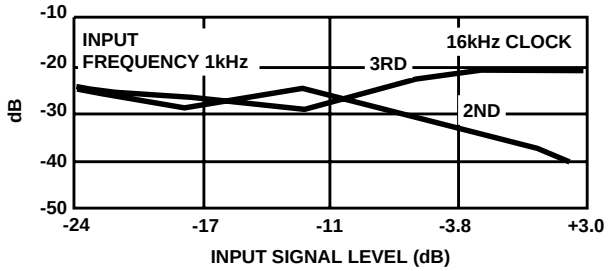


FIGURE 9A.

CVSD SIGNAL TO 2ND AND 3RD HARMONIC DISTORTION
C-MESSAGE WEIGHTED

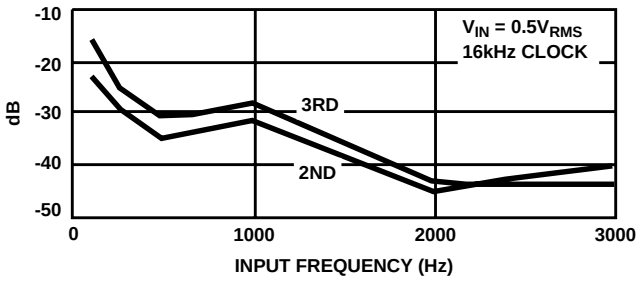


FIGURE 10A.

CVSD INPUT LEVEL vs 2ND AND 3RD HARMONIC DISTORTION
C-MESSAGE WEIGHTED

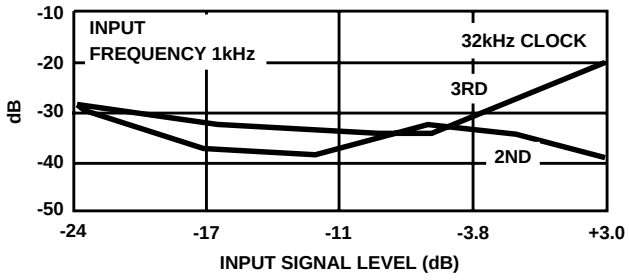


FIGURE 9B.

CVSD SIGNAL TO 2ND AND 3RD HARMONIC DISTORTION
C-MESSAGE WEIGHTED

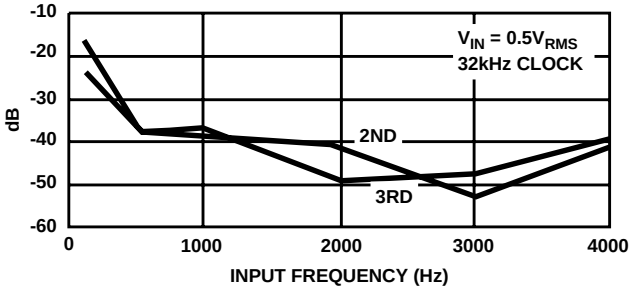


FIGURE 10B.

CVSD INPUT LEVEL vs 2ND AND 3RD HARMONIC DISTORTION
C-MESSAGE WEIGHTED

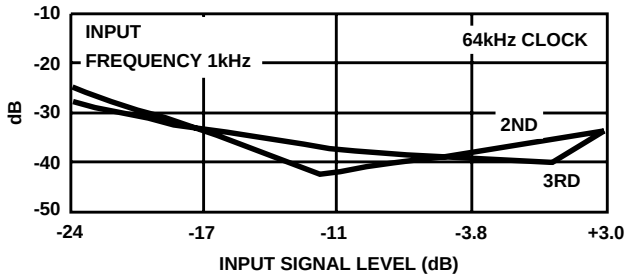


FIGURE 9C.

CVSD SIGNAL TO 2ND AND 3RD HARMONIC DISTORTION
C-MESSAGE WEIGHTED

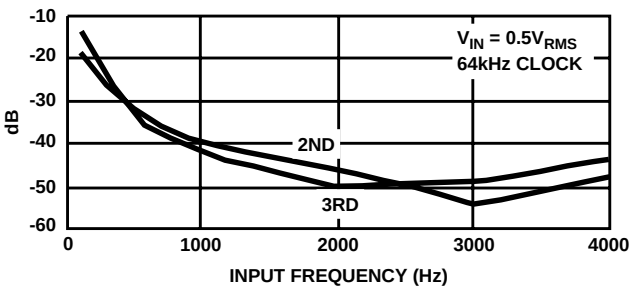
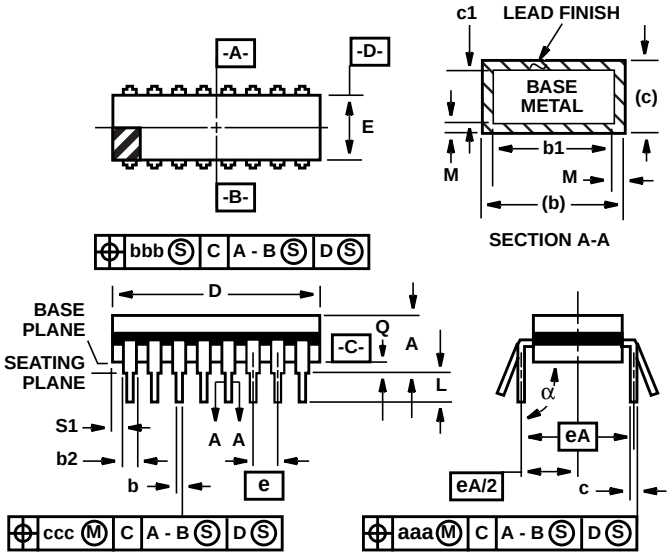


FIGURE 10C.

FIGURE 9. CVSD INPUT LEVEL vs 2ND AND 3RD HARMONIC DISTORTION

FIGURE 10. CVSD INPUT FREQUENCY vs 2ND AND 3RD HARMONIC DISTORTION

Ceramic Dual-In-Line Frit Seal Packages (CERDIP)



F14.3 MIL-STD-1835 GDIP1-T14 (D-1, CONFIGURATION A)
14 LEAD CERAMIC DUAL-IN-LINE FRIT SEAL PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.785	-	19.94	5
E	0.220	0.310	5.59	7.87	5
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	6
S1	0.005	-	0.13	-	7
α	90^o	105^o	90^o	105^o	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2, 3
N	14		14		8

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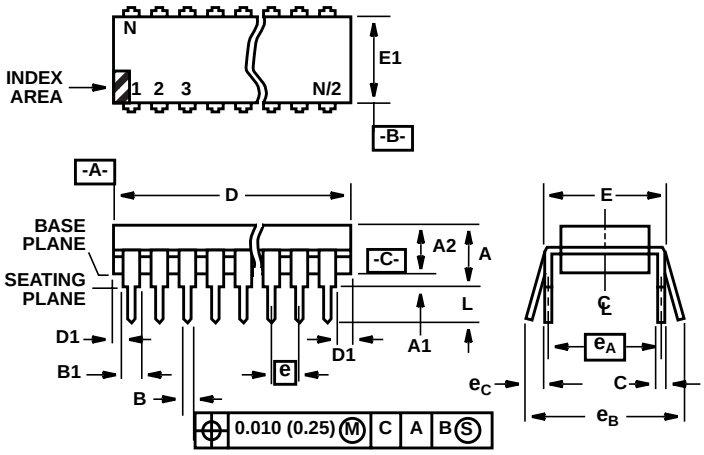
NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.

Dual-In-Line Plastic Packages (PDIP)



NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E14.3 (JEDEC MS-001-AA ISSUE D)
14 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8
C	0.008	0.014	0.204	0.355	-
D	0.735	0.775	18.66	19.68	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	14		14		9

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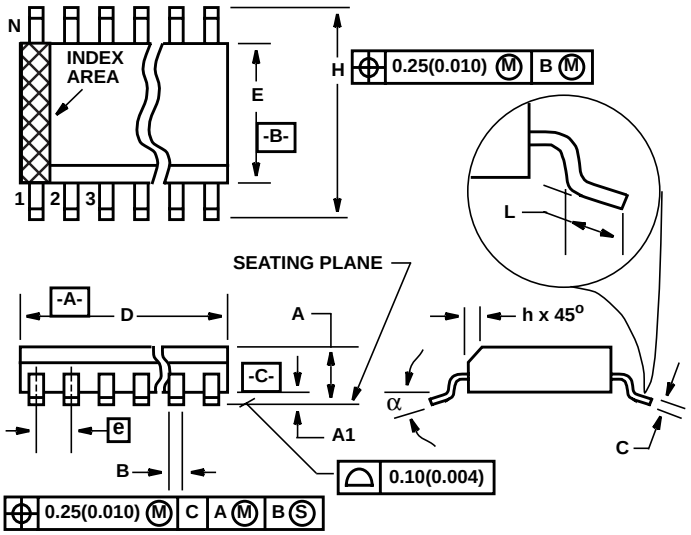
Small Outline Plastic Packages (SOIC)



NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M16.3 (JEDEC MS-013-AA ISSUE C)
16 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.0200	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.3977	0.4133	10.10	10.50	3
E	0.2914	0.2992	7.40	7.60	4
e	0.050 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	16		16		7
α	0^o	8^o	0^o	8^o	-

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