

# DATA SHEET

## **TDA8762A**

**10-bit high-speed low-power  
analog-to-digital converter**

Product specification  
Supersedes data of 1995 April 27  
File under Integrated Circuits, IC02

1996 Mar 21

# 10-bit high-speed low-power analog-to-digital converter

## TDA8762A

### FEATURES

- 10-bit resolution
- Sampling rate up to 80 MHz
- DC sampling allowed
- One clock cycle conversion only
- High signal-to-noise ratio over a large analog input frequency range (9.3 effective bits at 4.43 MHz full-scale input at  $f_{\text{clk}} = 80$  MHz)
- No missing codes guaranteed
- In range (IR) TTL output
- TTL compatible digital inputs and outputs
- Low-level AC clock input signal allowed
- External reference voltage regulator
- Power dissipation only 380 mW (typical)
- Low analog input capacitance, no buffer amplifier required
- No sample-and-hold circuit required.

### APPLICATIONS

High-speed analog-to-digital conversion for:

- Video data digitizing
- Radar pulse analysis
- Transient signal analysis
- High energy physics research
- $\Sigma\Delta$  modulators
- Medical imaging.

### GENERAL DESCRIPTION

The TDA8762A is a 10-bit high-speed analog-to-digital converter (ADC) for professional video and other applications. It converts the analog input signal into 10-bit binary-coded digital words at a maximum sampling rate of 80 MHz. All digital inputs and outputs are TTL compatible, although a low-level sine wave clock input signal is allowed.

### QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{\text{CCA}}$	analog supply voltage		4.75	5.0	5.25	V
$V_{\text{CCD}}$	digital supply voltage		4.75	5.0	5.25	V
$V_{\text{CCO}}$	output stages supply voltage		4.4	5.0	5.25	V
$I_{\text{CCA}}$	analog supply current		–	29	36	mA
$I_{\text{CCD}}$	digital supply current		–	24	30	mA
$I_{\text{CCO}}$	output stages supply current	$C_L = 15$ pF; ramp input	–	23	30	mA
INL	integral non-linearity	$f_{\text{clk}} = 80$ MHz; ramp input	–	$\pm 0.75$	$\pm 1.5$	LSB
DNL	differential non-linearity	$f_{\text{clk}} = 80$ MHz; ramp input	–	$\pm 0.3$	$\pm 0.7$	LSB
$f_{\text{clk(max)}}$	maximum clock frequency					
	TDA8762AM/6		60	–	–	MHz
	TDA8762AM/8		80	–	–	MHz
$P_{\text{tot}}$	total power dissipation		–	380	500	mW

### ORDERING INFORMATION

TYPE NUMBER	PACKAGE			SAMPLING FREQUENCY (MHz)
	NAME	DESCRIPTION	VERSION	
TDA8762AM/6	SSOP28	plastic shrink small outline package; 28 leads;	SOT341-1	60
TDA8762AM/8	SSOP28	body width 5.3 mm	SOT341-1	80

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## BLOCK DIAGRAM

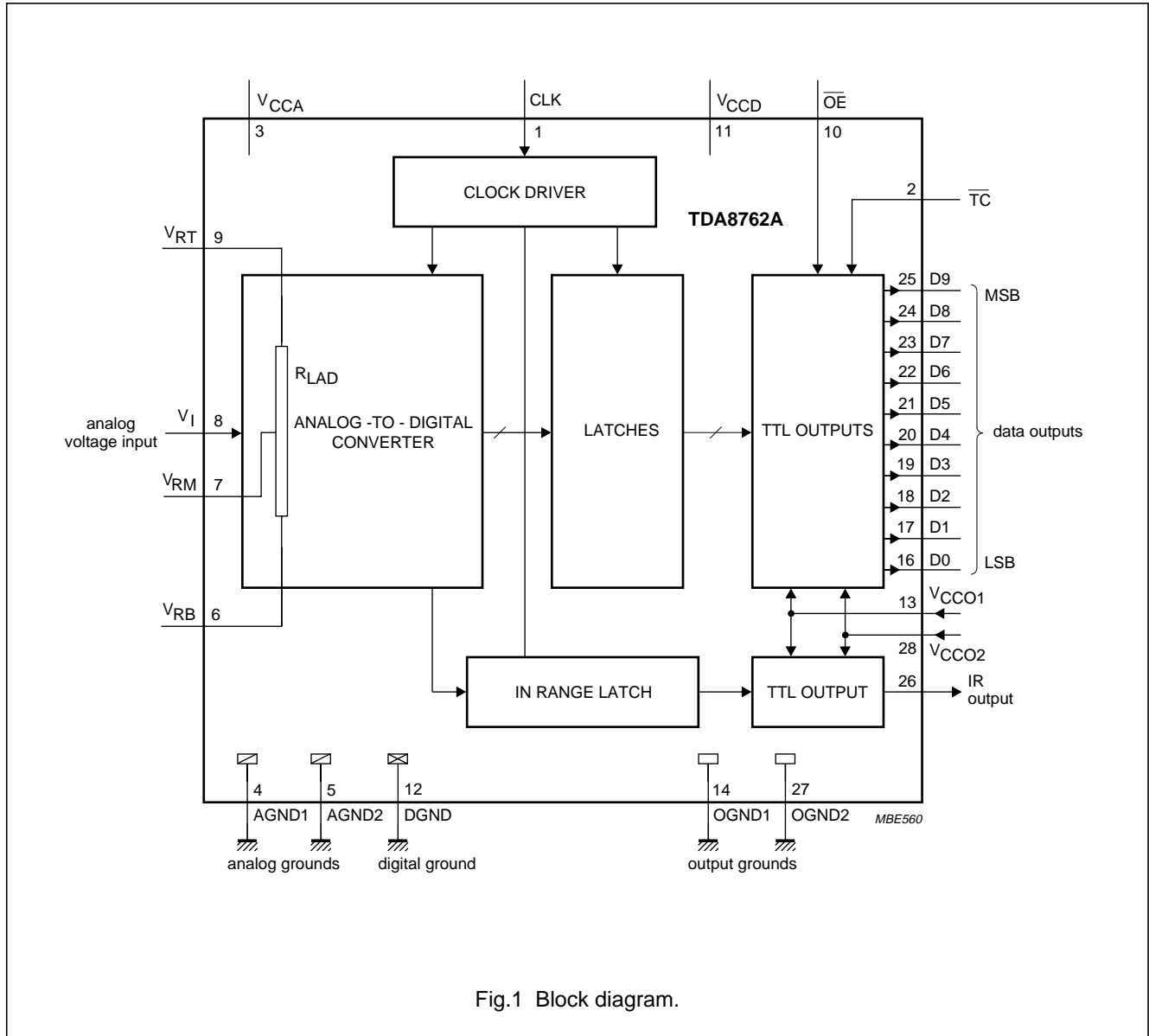


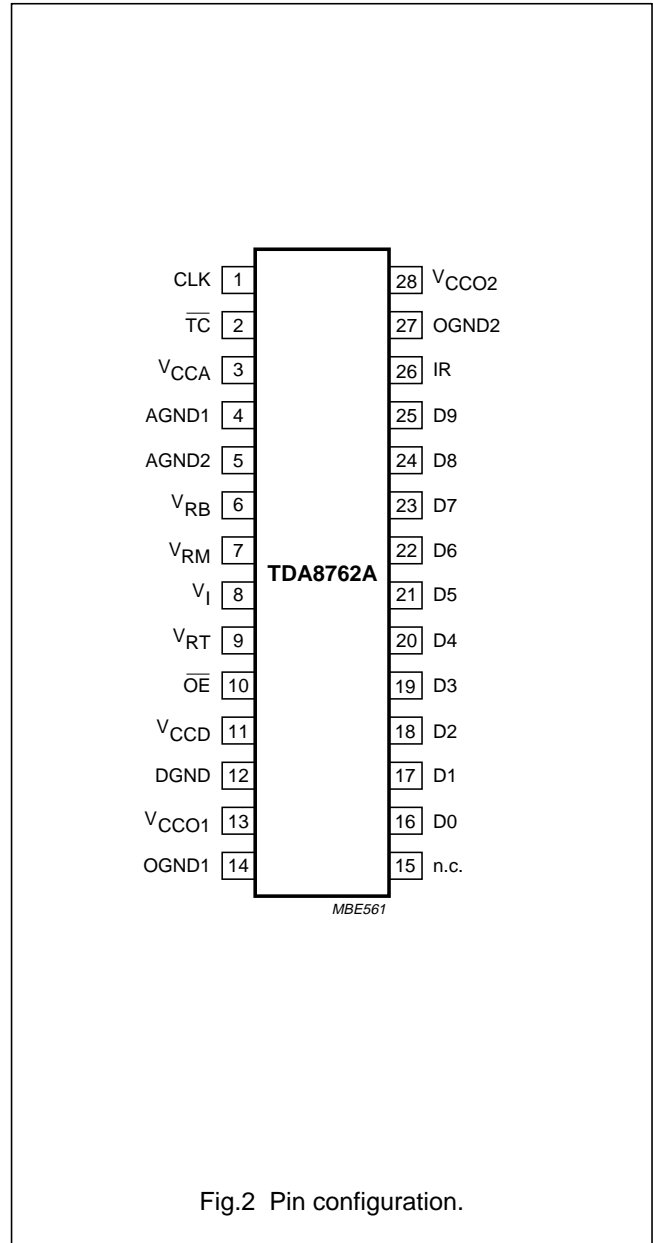
Fig.1 Block diagram.

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## PINNING

SYMBOL	PIN	DESCRIPTION
CLK	1	clock input
$\overline{TC}$	2	two's complement input (active LOW)
$V_{CCA}$	3	analog supply voltage (5 V)
AGND1	4	analog ground 1
AGND2	5	analog ground 2
$V_{RB}$	6	reference voltage BOTTOM input
$V_{RM}$	7	reference voltage MIDDLE
$V_I$	8	analog input voltage
$V_{RT}$	9	reference voltage TOP input
$\overline{OE}$	10	output enable input (TTL level input, active LOW)
$V_{CCD}$	11	digital supply voltage (5 V)
DGND	12	digital ground
$V_{CCO1}$	13	supply voltage for output stages 1 (5 V)
OGND1	14	output ground 1
n.c.	15	not connected
D0	16	data output; bit 0 (LSB)
D1	17	data output; bit 1
D2	18	data output; bit 2
D3	19	data output; bit 3
D4	20	data output; bit 4
D5	21	data output; bit 5
D6	22	data output; bit 6
D7	23	data output; bit 7
D8	24	data output; bit 8
D9	25	data output; bit 9 (MSB)
IR	26	in range data output
OGND2	27	output ground 2
$V_{CCO2}$	28	supply voltage for output stages 2 (5 V)



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## LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{CCA}$	analog supply voltage	note 1	-0.3	+7.0	V
$V_{CCD}$	digital supply voltage	note 1	-0.3	+7.0	V
$V_{CCO}$	output stages supply voltage	note 1	-0.3	+7.0	V
$\Delta V_{CC}$	supply voltage difference				
	$V_{CCA} - V_{CCD}$		-1.0	+1.0	V
	$V_{CCA} - V_{CCO}$		-1.0	+1.0	V
	$V_{CCD} - V_{CCO}$		-1.0	+1.0	V
$V_I$	input voltage	referenced to AGND	-0.3	+7.0	V
$V_{clk(p-p)}$	AC input voltage for switching (peak-to-peak value)	referenced to DGND	-	$V_{CCD}$	V
$I_O$	output current		-	10	mA
$T_{stg}$	storage temperature		-55	+150	°C
$T_{amb}$	operating ambient temperature		0	+70	°C
$T_j$	junction temperature		-	+150	°C

### Note

- The supply voltages  $V_{CCA}$ ,  $V_{CCD}$  and  $V_{CCO}$  may have any value between -0.3 and +7.0 V provided that the supply voltage differences  $\Delta V_{CC}$  are respected.

## HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

## THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient in free air	110	K/W

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## CHARACTERISTICS

$V_{CCA} = V_3$  to  $V_4$  and  $V_5 = 4.75$  to  $5.25$  V;  $V_{CCD} = V_{11}$  to  $V_{12} = 4.75$  to  $5.25$  V;  $V_{CCO} = V_{13}$  and  $V_{28}$  to  $V_{14}$  and  $V_{27} = 4.4$  to  $5.25$  V; AGND and DGND shorted together;  $T_{amb} = 0$  to  $+70$  °C; typical values measured at  $V_{CCA} = V_{CCD} = V_{CCO} = 5$  V;  $V_{I(p-p)} = 2.0$  V;  $C_L = 15$  pF and  $T_{amb} = 25$  °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Supply</b>						
$V_{CCA}$	analog supply voltage		4.75	5.0	5.25	V
$V_{CCD}$	digital supply voltage		4.75	5.0	5.25	V
$V_{CCO}$	output stages supply voltage		4.4	5.0	5.25	V
$\Delta V_{CC}$	voltage difference					
	$V_{CCA} - V_{CCD}$		-0.25	-	+0.25	V
	$V_{CCA} - V_{CCO}$		-0.4	-	+0.4	V
	$V_{CCD} - V_{CCO}$		-0.4	-	+0.4	V
$I_{CCA}$	analog supply current		-	29	36	mA
$I_{CCD}$	digital supply current		-	24	30	mA
$I_{CCO}$	output stages supply current	$C_L = 15$ pF; ramp input	-	23	30	mA
<b>Inputs</b>						
CLOCK INPUT CLK (REFERENCED TO DGND); note 1						
$V_{IL}$	LOW level input voltage		0	-	0.8	V
$V_{IH}$	HIGH level input voltage		2.0	-	$V_{CCD}$	V
$I_{IL}$	LOW level input current	$V_{clk} = 0.4$ V	-1	0	+1	$\mu$ A
$I_{IH}$	HIGH level input current	$V_{clk} = 2.7$ V	-	-	20	$\mu$ A
$Z_i$	input impedance	$f_{clk} = 80$ MHz	-	2	-	k $\Omega$
$C_i$	input capacitance	$f_{clk} = 80$ MHz	-	2	-	pF
INPUTS $\overline{OE}$ AND $\overline{TC}$ (REFERENCED TO DGND); see Table 2						
$V_{IL}$	LOW level input voltage		0	-	0.8	V
$V_{IH}$	HIGH level input voltage		2.0	-	$V_{CCD}$	V
$I_{IL}$	LOW level input current	$V_{IL} = 0.4$ V	-400	-	-	$\mu$ A
$I_{IH}$	HIGH level input current	$V_{IH} = 2.7$ V	-	-	20	$\mu$ A
$V_i$ (ANALOG INPUT VOLTAGE REFERENCED TO AGND)						
$I_{IL}$	LOW level input current	$V_i = 1.3$ V	-	0	-	$\mu$ A
$I_{IH}$	HIGH level input current	$V_i = 3.8$ V	-	70	-	$\mu$ A
$Z_i$	input impedance	$f_i = 4.43$ MHz	-	5	-	k $\Omega$
$C_i$	input capacitance	$f_i = 4.43$ MHz	-	8	-	pF

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Reference voltages for the resistor ladder; see Table 1</b>						
$V_{RB}$	reference voltage BOTTOM		1.2	1.3	–	V
$V_{RT}$	reference voltage TOP		–	3.8	$V_{CCA} - 0.8$ V	V
$V_{diff}$	differential reference voltage $V_{RT} - V_{RB}$		1.8	2.5	3.0	V
$I_{ref}$	reference current		–	28	–	mA
$R_{LAD}$	resistor ladder		–	90	–	$\Omega$
$TC_{RLAD}$	temperature coefficient of the resistor ladder		–	1860	–	ppm
				167		m $\Omega$ /K
$V_{osB}$	offset voltage BOTTOM	note 2	–	220	–	mV
$V_{osT}$	offset voltage TOP	note 2	–	220	–	mV
$V_{I(p-p)}$	analog input voltage (peak-to-peak value)	note 3	1.5	2.06	2.5	V
<b>Outputs</b>						
DIGITAL OUTPUTS D9 TO D0 AND IR (REFERENCED TO OGND)						
$V_{OL}$	LOW level output voltage	$I_O = 1$ mA	0	–	0.4	V
$V_{OH}$	HIGH level output voltage	$I_O = 0$ mA	2.7	–	$V_{CCO} - 0.5$	V
		$I_O = -0.4$ mA	2.7	–	$V_{CCO} - 1.3$	V
		$I_O = -1$ mA	2.4	–	$V_{CCO} - 1.4$	V
$I_{OZ}$	output current in 3-state mode	$0.4$ V < $V_O$ < $V_{CCO}$	–20	–	+20	$\mu$ A
<b>Switching characteristics</b>						
CLOCK INPUT CLK; see Fig.4; note 1						
$f_{clk(max)}$	maximum clock frequency TDA8762A/6 TDA8762A/8		60	–	–	MHz
			80	–	–	MHz
$t_{CPH}$	clock pulse width HIGH		5	–	–	ns
$t_{CPL}$	clock pulse width LOW		5	–	–	ns
<b>Analog signal processing</b>						
LINEARITY						
INL	integral non-linearity	$f_{clk} = 80$ MHz; ramp input	–	$\pm 0.75$	$\pm 1.5$	LSB
DNL	differential non-linearity	$f_{clk} = 80$ MHz; ramp input	–	$\pm 0.3$	$\pm 0.7$	LSB
OFER	offset error	middle code; $V_{RB} = 1.3$ V; $V_{RT} = 3.8$ V	–	$\pm 1$	–	LSB
GER	gain error (from device to device)	$V_{RB} = 1.3$ V; $V_{RT} = 3.8$ V; note 4	–	$\pm 0.1$	–	%

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
BANDWIDTH ( $f_{\text{clk}} = 80 \text{ MHz}$ )						
B	analog bandwidth	full-scale sine wave; note 5	–	40	–	MHz
		75% full-scale sine wave; note 5	–	55	–	MHz
		small signal at mid-scale; $V_I = \pm 10 \text{ LSB}$ at code 512; note 5	–	700	–	MHz
$t_{\text{STLH}}$	analog input settling time LOW-to-HIGH	full-scale square wave; see Fig.6; note 6	–	2.0	3	ns
$t_{\text{STHL}}$	analog input settling time HIGH-to-LOW	full-scale square wave; see Fig.6; note 6	–	2.5	3.5	ns
HARMONICS ( $f_{\text{clk}} = 80 \text{ MHz}$ )						
$h_1$	fundamental harmonics (full scale)	$f_i = 4.43 \text{ MHz}$	–	–	0	dB
$h_{\text{all}}$	harmonics (full scale); all components	$f_i = 4.43 \text{ MHz}$				
	second harmonics		–	–70	62	dB
	third harmonics		–	–75	67	dB
THD	total harmonic distortion	$f_i = 4.43 \text{ MHz}$	–	–68	–	dB
SIGNAL-TO-NOISE RATIO; see Fig.8; note 7						
S/N	signal-to-noise ratio (full scale)	without harmonics; $f_{\text{clk}} = 80 \text{ MHz}$ ; $f_i = 4.43 \text{ MHz}$	56	58	–	dB
EFFECTIVE BITS; see Figs 7, 8 and 9; note 7						
EB	effective bits TDA8762AM/6	$f_{\text{clk}} = 60 \text{ MHz}$				
		$f_i = 4.43 \text{ MHz}$	–	9.35	–	bits
		$f_i = 10 \text{ MHz}$	–	9.0	–	bits
	TDA8762AM/8	$f_i = 20 \text{ MHz}$	–	8.1	–	bits
		$f_{\text{clk}} = 80 \text{ MHz}$				
		$f_i = 4.43 \text{ MHz}$	–	9.3	–	bits
	$f_i = 10 \text{ MHz}$	–	8.9	–	bits	
	$f_i = 20 \text{ MHz}$	–	8.0	–	bits	
TWO-TONE; note 8						
TTIR	two-tone intermodulation rejection	$f_{\text{clk}} = 80 \text{ MHz}$	–	–68	–	dB
BIT ERROR RATE						
BER	bit error rate	$f_{\text{clk}} = 80 \text{ MHz}$ ; $f_i = 4.43 \text{ MHz}$ ; $V_I = \pm 16 \text{ LSB}$ at code 512	–	$10^{-13}$	–	times/sample



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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DIFFERENTIAL GAIN; note 9						
G <sub>diff</sub>	differential gain	f <sub>clk</sub> = 80 MHz; PAL modulated ramp	–	0.5	–	%
DIFFERENTIAL PHASE; note 9						
φ <sub>diff</sub>	differential phase	f <sub>clk</sub> = 80 MHz; PAL modulated ramp	–	0.5	–	deg
<b>Timing (f<sub>clk</sub> = 80 MHz; C<sub>L</sub> = 15 pF); see Fig.4; note 10</b>						
t <sub>ds</sub>	sampling delay time		–	–	2	ns
t <sub>h</sub>	output hold time		5	–	–	ns
t <sub>d</sub>	output delay time		–	9	13	ns
C <sub>L</sub>	digital output load capacitance		–	15	20	pF
<b>3-state output delay times; see Fig.5</b>						
t <sub>dZH</sub>	enable HIGH		–	45	50	ns
t <sub>dZL</sub>	enable LOW		–	25	35	ns
t <sub>dHZ</sub>	disable HIGH		–	12	15	ns
t <sub>dLZ</sub>	disable LOW		–	12	15	ns

Notes

- In addition to a good layout of the digital and analog ground, it is recommended that the rise and fall times of the clock must not be less than 0.5 ns.
- Analog input voltages producing code 0 up to and including code 1023:
  - V<sub>osB</sub> (voltage offset BOTTOM) is the difference between the analog input which produces data equal to 00 and the reference voltage BOTTOM (V<sub>RB</sub>) at T<sub>amb</sub> = 25 °C.
  - V<sub>osT</sub> (voltage offset TOP) is the difference between V<sub>RT</sub> (reference voltage TOP) and the analog input which produces data outputs equal to code 1023 at T<sub>amb</sub> = 25 °C.
- In order to ensure the optimum linearity performance of such converter architecture the lower and upper extremities of the converter reference resistor ladder (corresponding to output codes 0 and 1023 respectively) are connected to pins V<sub>RB</sub> and V<sub>RT</sub> via offset resistors R<sub>OB</sub> and R<sub>OT</sub> as shown in Fig.3.

a) The current flowing into the resistor ladder is  $I_L = \frac{V_{RT} - V_{RB}}{R_{OB} + R_L + R_{OT}}$  and the full-scale input range at the converter,

to cover code 0 to code 1023, is  $V_I = R_L \times I_L = \frac{R_L}{R_{OB} + R_L + R_{OT}} \times (V_{RT} - V_{RB}) = 0.824 \times (V_{RT} - V_{RB})$

b) Since R<sub>L</sub>, R<sub>OB</sub> and R<sub>OT</sub> have similar behaviour with respect to process and temperature variation, the ratio

$\frac{R_L}{R_{OB} + R_L + R_{OT}}$  will be kept reasonably constant from part to part. Consequently variation of the output codes

at a given input voltage depends mainly on the difference V<sub>RT</sub> – V<sub>RB</sub> and its variation with temperature and supply voltage. When several ADCs are connected in parallel and fed with the same reference source, the matching between each of them is then optimized.

4.  $GER = \frac{(V_{1023} - V_0) - 2 V}{2 V} \times 100$

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5. The analog bandwidth is defined as the maximum input sine wave frequency which can be applied to the device. No glitches greater than 2 LSBs, neither any significant attenuation are observed in the reconstructed signal.
6. The analog input settling time is the minimum time required for the input signal to be stabilized after a sharp full-scale input (square-wave signal) in order to sample the signal and obtain correct output data.
7. Effective bits are obtained via a Fast Fourier Transform (FFT) treatment taking 8K acquisition points per equivalent fundamental period. The calculation takes into account all harmonics and noise up to half of the clock frequency (NYQUIST frequency). Conversion to signal-to-noise ratio:  $S/N = EB \times 6.02 + 1.76$  dB.
8. Intermodulation measured relative to either tone with analog input frequencies of 4.43 MHz and 4.53 MHz. The two input signals have the same amplitude and the total amplitude of both signals provides full scale to the converter.
9. Measurement carried out using video analyser VM700A, where the video analog signal is reconstructed through a digital-to-analog converter.
10. Output data acquisition: the output data is available after the maximum delay time of  $t_d$ . In the event of a 80 MHz clock operation, the hardware design must take into account the  $t_d$  and  $t_h$  limits with respect to the input characteristics of the acquisition circuit; an external latch will ease the design if output data lines cannot be short to minimize capacitance.

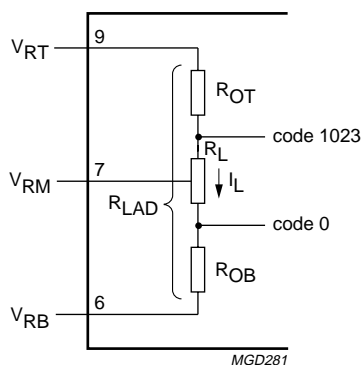


Fig.3 Explanation of note 3.

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**Table 1** Output coding and input voltage (typical values; referenced to AGND,  $V_{RB} = 1.3\text{ V}$ ,  $V_{RT} = 3.8\text{ V}$ )

STEP	$V_{I(p-p)}$	IR	BINARY OUTPUT BITS										TWO'S COMPLEMENT OUTPUT BITS															
			D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0						
U/F	<1.52	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	1.52	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	.	1	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
1022	.	1	1	1	1	1	1	1	1	1	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	
1023	3.58	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
O/F	>3.58	0	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	

**Table 2** Mode selection

$\overline{\text{TC}}$	$\overline{\text{OE}}$	D9 TO D0	IR
X	1	high impedance	high impedance
0	0	active; two's complement	active
1	0	active; binary	active

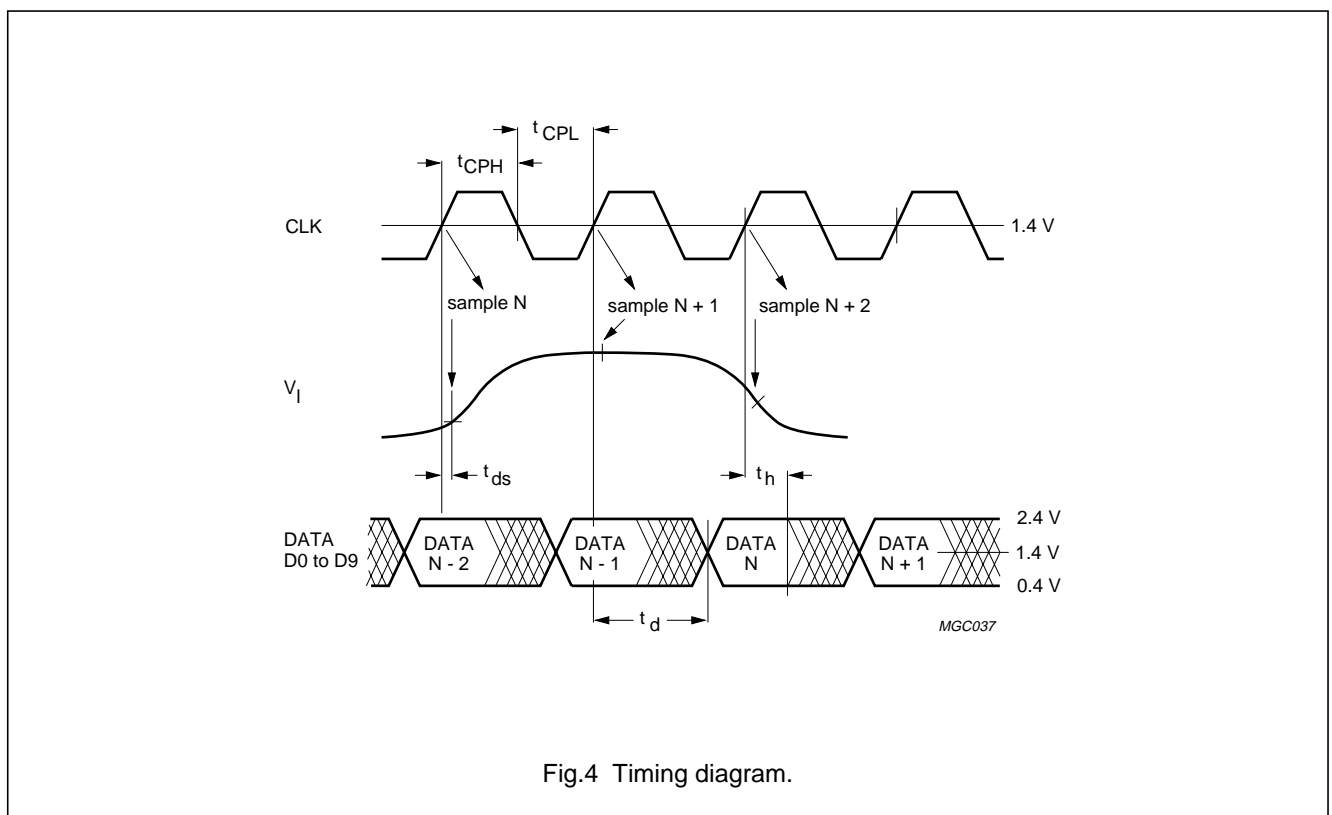
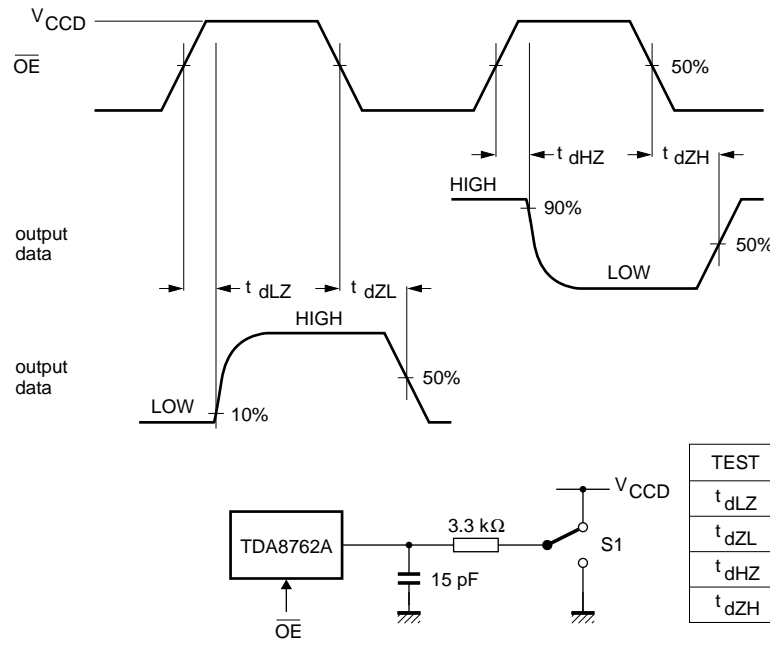


Fig.4 Timing diagram.

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$f_{\overline{OE}} = 100 \text{ kHz}$ .

Fig.5 Timing diagram and test conditions of 3-state output delay time.

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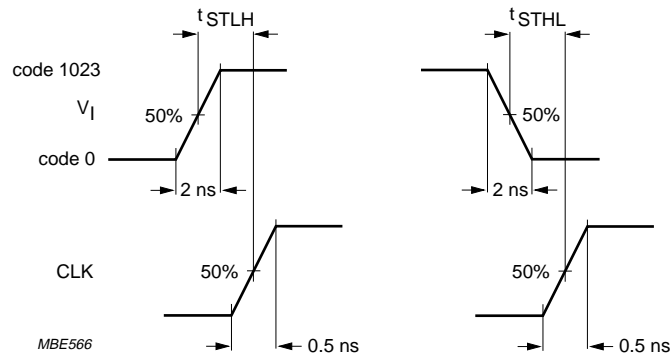
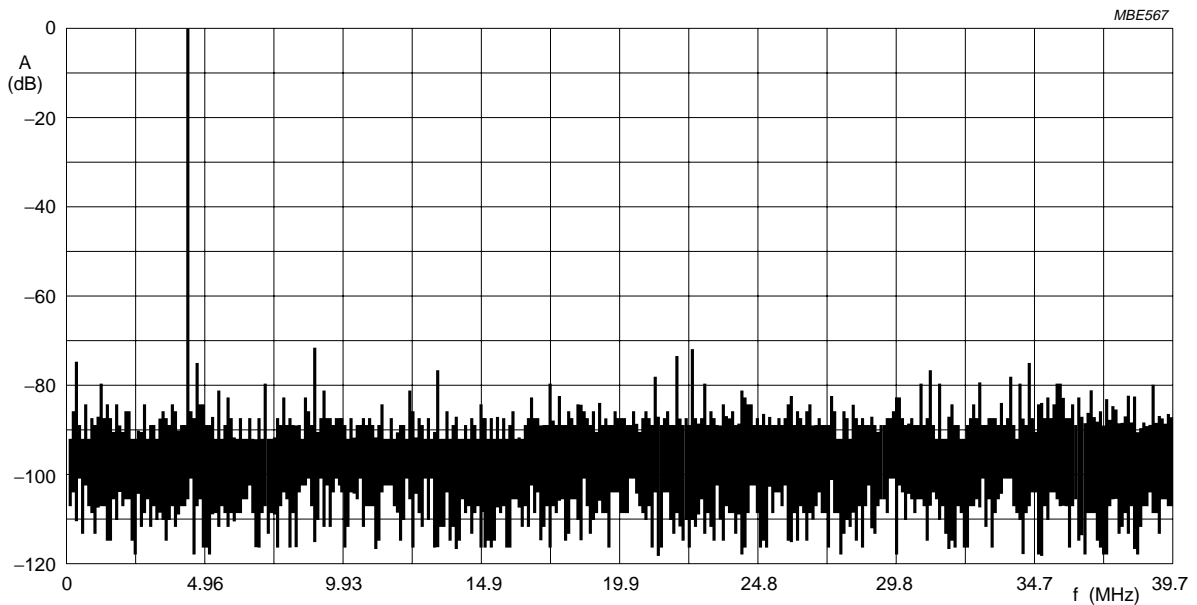


Fig.6 Analog input settling-time diagram.

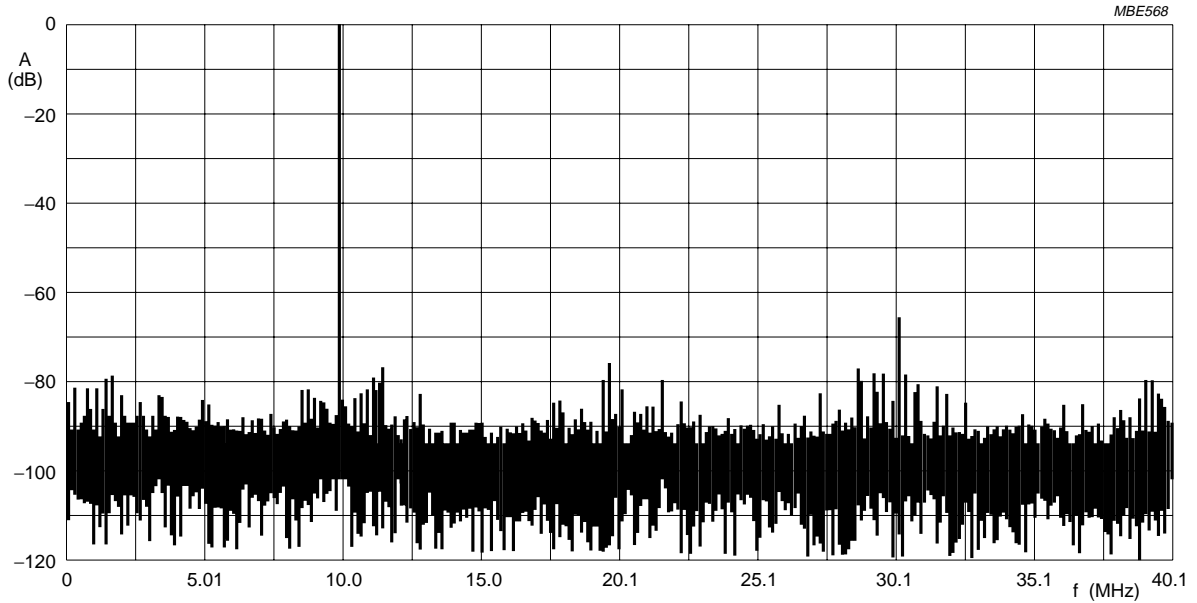


Effective bits: 9.35; THD = -71.18 dB;  
Harmonic levels (dB): 2nd = -73.61; 3rd = -76.14; 4th = -83.82; 5th = -87.36; 6th = -86.33.

Fig.7 Fast Fourier Transform ( $f_{clk} = 80$  MHz;  $f_i = 4.43$  MHz).

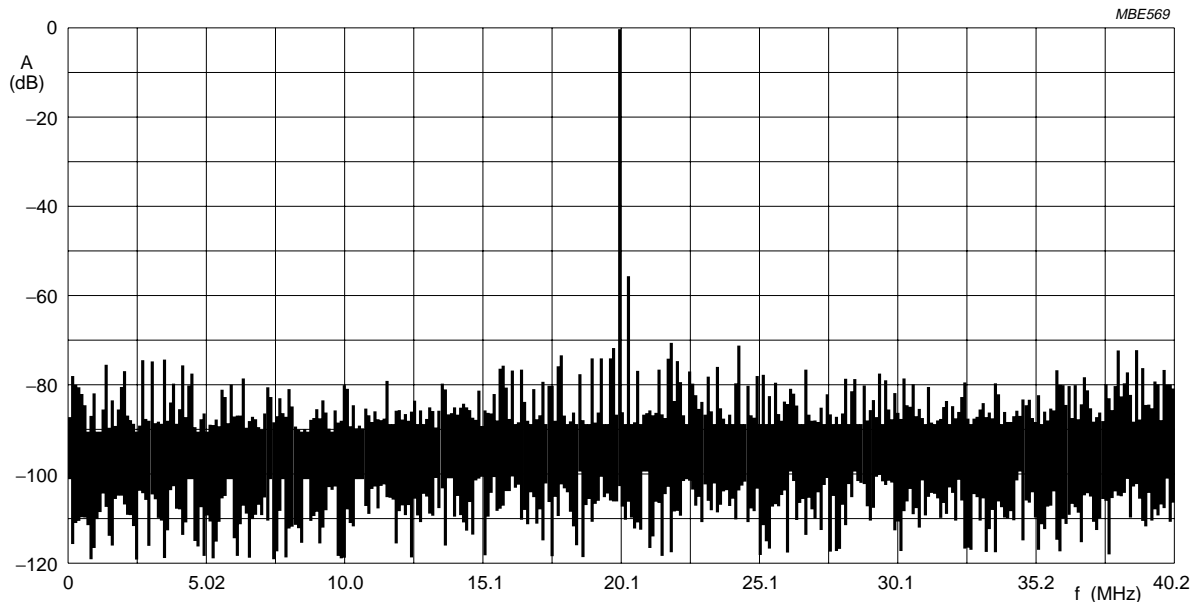
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Effective bits: 9.12; THD = -65.45 dB;  
Harmonic levels (dB): 2nd = -79.52; 3rd = -66.03; 4th = -81.60; 5th = -77.47; 6th = -104.43.

Fig.8 Fast Fourier Transform ( $f_{clk} = 80 \text{ MHz}$ ;  $f_i = 10 \text{ MHz}$ ).



Effective bits: 8.08; THD = -52.60 dB;  
Harmonic levels (dB): 2nd = -58.35; 3rd = -54.22; 4th = -76.61; 5th = -66.90; 6th = -76.80.

Fig.9 Fast Fourier Transform ( $f_{clk} = 80 \text{ MHz}$ ;  $f_i = 20 \text{ MHz}$ ).

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## INTERNAL PIN CONFIGURATIONS

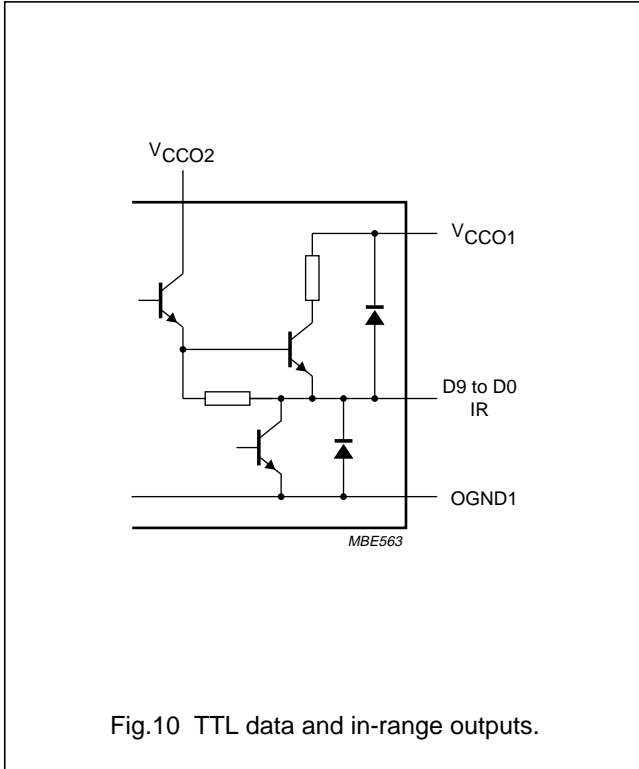


Fig.10 TTL data and in-range outputs.

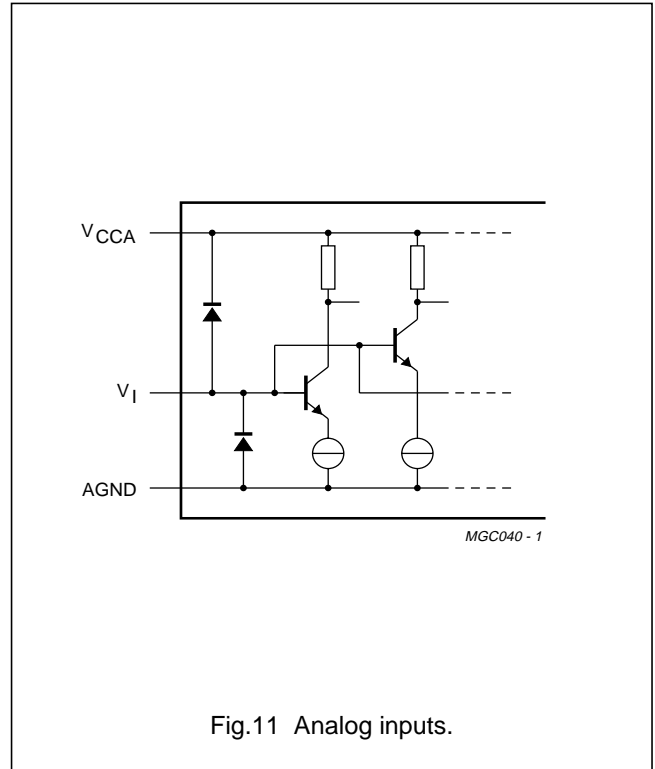


Fig.11 Analog inputs.

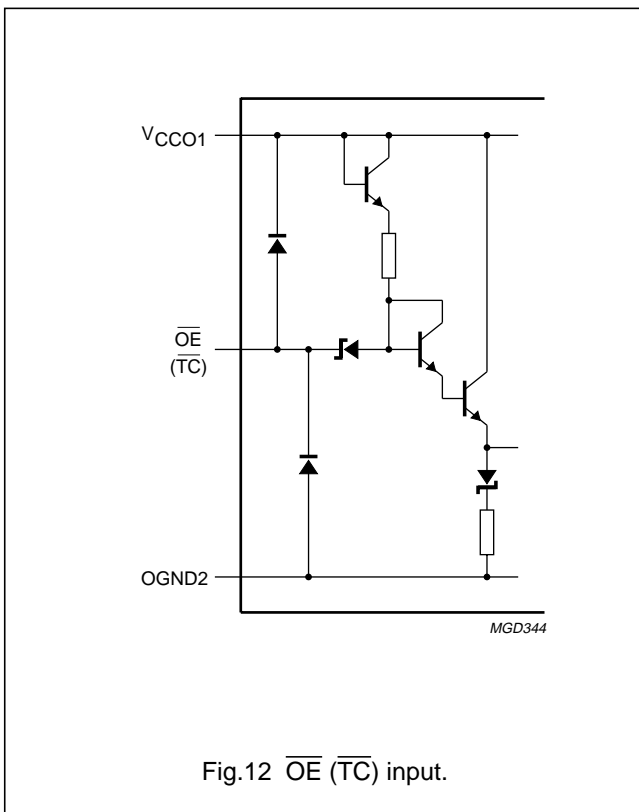


Fig.12  $\overline{OE}$  ( $\overline{TC}$ ) input.

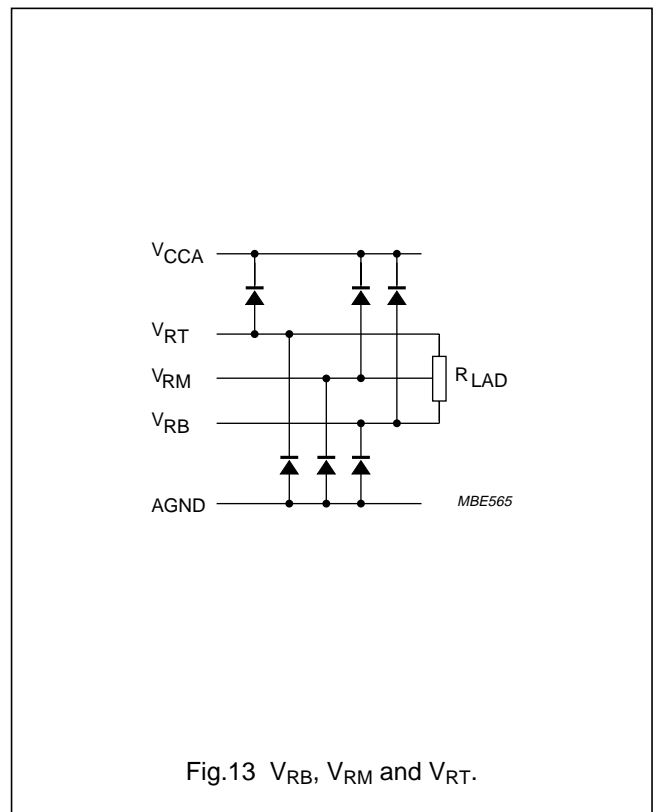


Fig.13  $V_{RB}$ ,  $V_{RM}$  and  $V_{RT}$ .

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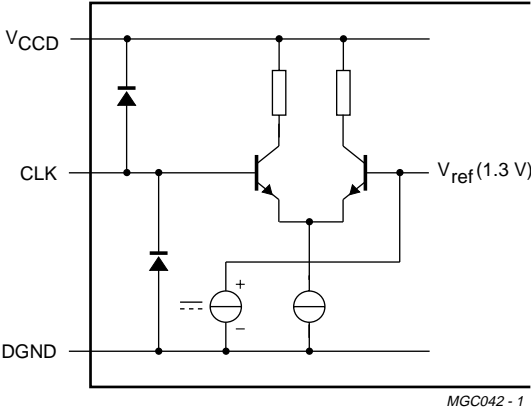


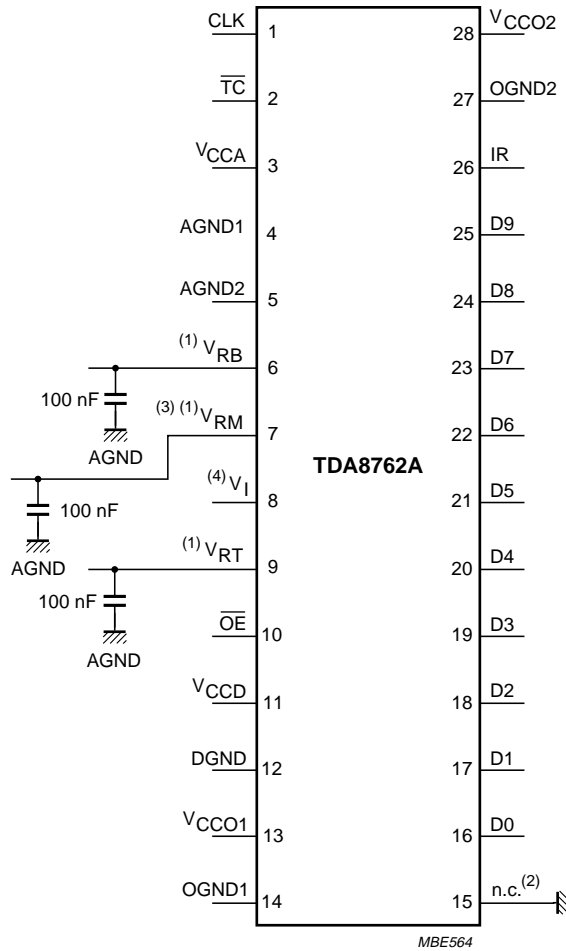
Fig.14 CLK input.



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APPLICATION INFORMATION



The analog and digital supplies should be separated and decoupled.

The external voltage reference generator must be built such that a good supply voltage ripple rejection is achieved with respect to the LSB value. Eventually, the reference ladder voltages can be derived from a well regulated  $V_{CCA}$  supply through a resistor bridge and a decoupled capacitor.

- (1)  $V_{RB}$ ,  $V_{RM}$  and  $V_{RT}$  are decoupled to AGND.
- (2) Pin 15 should be connected to DGND in order to prevent noise influence.
- (3) When  $V_{RM}$  is not used, pin 7 can be left open, avoiding the decoupling capacitor. In any case, this pin must not be grounded.
- (4) When analog input signal is AC coupled, an input bias or a clamping level must be applied to  $V_I$  input (pin 8).

Fig.15 Application diagram.

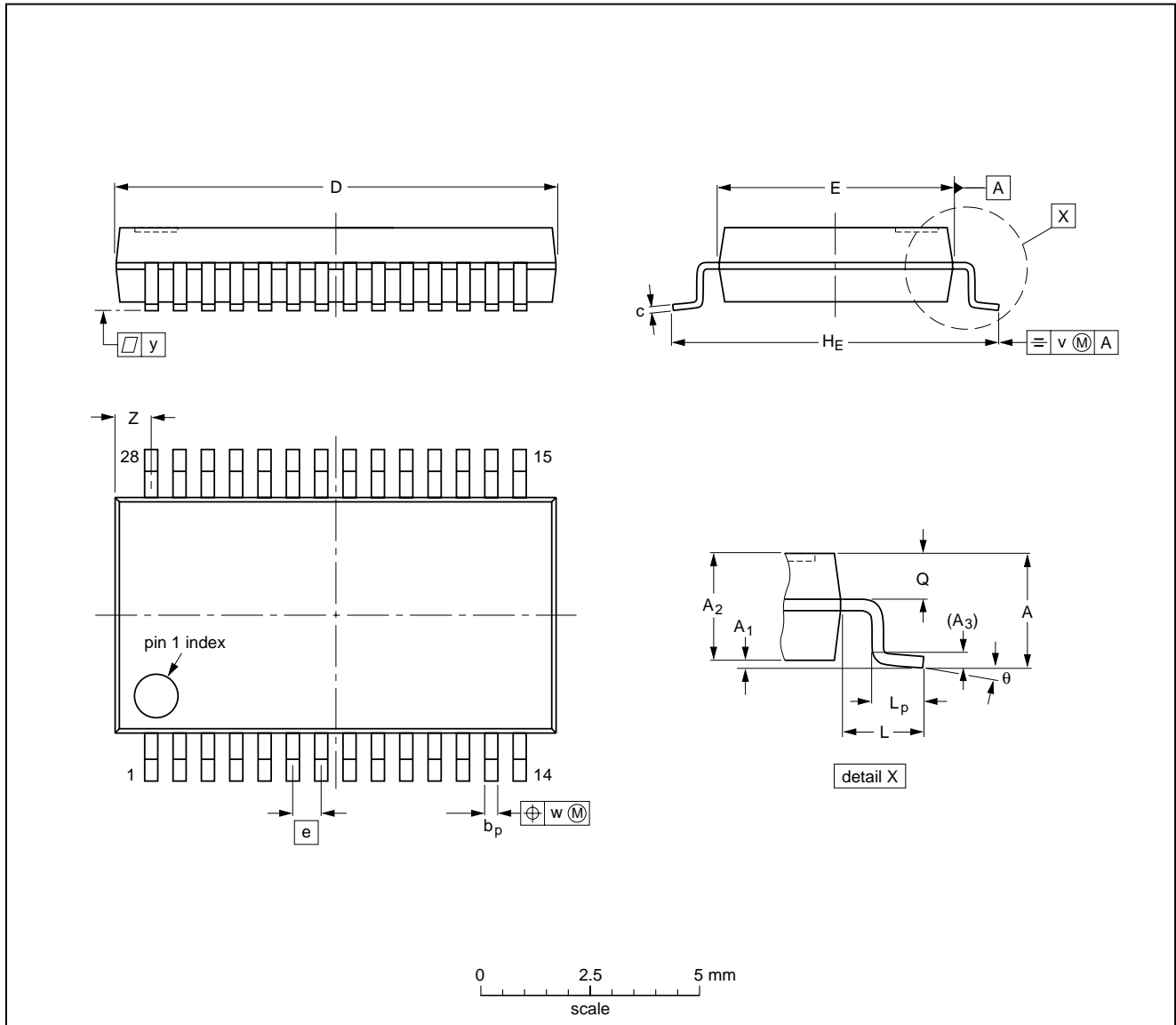
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PACKAGE OUTLINE

SSOP28: plastic shrink small outline package; 28 leads; body width 5.3 mm

SOT341-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	10.4 10.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.1 0.7	8° 0°

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT341-1		MO-150AH				93-09-08 95-02-04

## 10-bit high-speed low-power analog-to-digital converter

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### SOLDERING

#### Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our "IC Package Databook" (order code 9398 652 90011).

#### Reflow soldering

Reflow soldering techniques are suitable for all SSOP packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

#### Wave soldering

Wave soldering is **not** recommended for SSOP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The longitudinal axis of the package footprint must be parallel to the solder flow and must incorporate solder thieves at the downstream end.**

**Even with these conditions, only consider wave soldering SSOP packages that have a body width of 4.4 mm, that is SSOP16 (SOT369-1) or SSOP20 (SOT266-1).**

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

#### Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

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## DEFINITIONS

<b>Data sheet status</b>	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
<b>Limiting values</b>	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
<b>Application information</b>	
Where application information is given, it is advisory and does not form part of the specification.	

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**NOTES**

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Printed in The Netherlands

537021/1100/02/pp24  
Document order number:

Date of release: 1996 Mar 21  
9397 750 00751