

800MHz TDMA FRONT-END GaAs MMIC

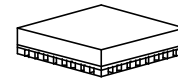
■GENERAL DESCRIPTION

NJG1707PG1 is a front-end IC for a digital cellular phone of 800MHz band. A 2x6 antenna switches and a low noise amplifier are included.

The parallel control signals of three bits logic connect T/R circuits to internal two antennas or external two antennas. The termination ports with external matching circuits make low interference between diversity antennas.

The ultra small & thin FFP32-G1 package is adopted.

■PACKAGE OUTLINE



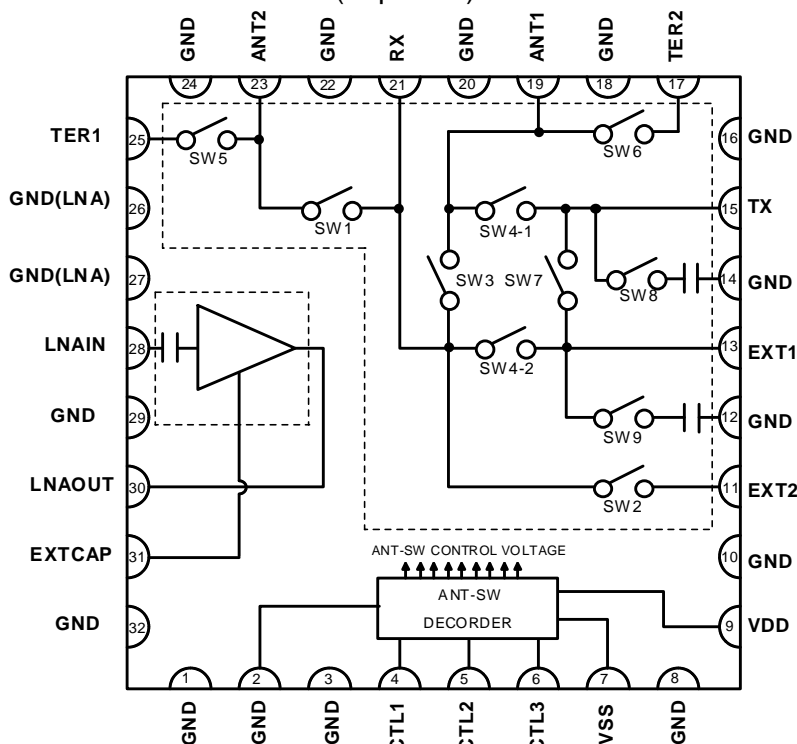
NJG1707PG1

■FEATURES

- Ultra small & thin package FFP32-G1 (Mount Size: 4.5x4.5x0.85mm)
- Antenna Switch
 - Low voltage operation -2.5V (Tx only) and +3.5V
 - Low current consumption 10uA typ. (Tx Mode, $P_{in}=30\text{dBm}$), 2uA typ. (Rx Mode, $P_{in}=10\text{dBm}$)
 - Low insertion loss 0.5dB typ. @ (Tx-ANT1, Tx-EXT1) $f_{in}=960\text{MHz}$, $P_{in}=30\text{dBm}$
 - Low Adjacent Channel Leakage Power -63dBc typ. @ $V_{DD}=+3.5\text{V}$, $V_{SS}=-2.5\text{V}$, $f_{in}=960\text{MHz}$, $P_{in}=30\text{dBm}$
- Low Noise Amplifier
 - Low voltage operation +2.7V typ.
 - Low current consumption +2.7mA typ.
 - Small signal gain 17.5dB typ. @ $f=820\text{MHz}$
 - Low noise figure 1.4dB typ. @ $f=820\text{MHz}$
 - High input IP3 IIP3=-4.5dBm typ. OIP3=+13dBm typ. @ $f=820\text{MHz}+820.1\text{MHz}$

■PIN CONFIGURATION

FFP32 Type
(Top View)



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■ABSOLUTE MAXIMUM RATINGS

| | | | | (T _a =25°C) | |
|-----------------------|------------------|----------------------------|-----------|------------------------|--|
| PARAMETER | SYMBOL | CONDITIONS | RATINGS | UNITS | |
| Supply Voltage 1 | V _{DD1} | V _{DD} Terminal | 6.0 | V | |
| Supply Voltage 2 | V _{DD2} | LNAOUT Terminal | 5.0 | V | |
| Supply Voltage 3 | V _{SS} | V _{SS} Terminal | -4.0~+0.3 | V | |
| Control Voltage | V _{CTL} | CTL1, CTL2, CTL3 Terminals | 6.0 | V | |
| Input Power | P _{in} | TX, ANT1, EXT1 Terminals | 37 | dBm | |
| | | RX, ANT2, EXT2 Terminals | 28 | dBm | |
| | | LNAIN Terminal | 10 | dBm | |
| Power Dissipation | P _D | | 600 | mW | |
| Operating Temperature | T _{opr} | | -40~+85 | °C | |
| Storage Temperature | T _{stg} | | -55~+125 | °C | |

■ELECTRICAL CHARACTERISTICS 1 [ANTENNA SWITCH DC CHARACTERISTICS]

General Conditions: T_a=25°C, V_{DD}=3.5V, V_{SS}=-2.5V

TX, RX, ANT1, ANT2, EXT1, EXT2: terminated (50Ω)

TER1, TER2 : grounded by 10pF capacitor

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|----------------------------------|---------------------|--|------|------|-----------------|-------|
| Positive Supply Voltage | V _{DD} | V _{DD} Terminal | 2.7 | 3.5 | 5.0 | V |
| Negative Supply Voltage | V _{SS} | V _{SS} Terminal | -3.5 | -2.5 | -2.0 | V |
| Current Consumption 1 | I _{DD1} | V _{DD} Terminal Rx Mode, No RF Signal | - | 2.0 | 5.0 | μA |
| Current Consumption 2 | I _{SS1} | V _{SS} Terminal Rx Mode, No RF Signal | -0.1 | - | 0 | uA |
| Current Consumption 3 | I _{DD2} | V _{DD} Terminal, f _{in} =0.1~2GHz Tx Mode, P _{in} =30dBm | - | 10 | 30 | uA |
| Current Consumption 4 | I _{SS2} | V _{SS} Terminal, f _{in} =0.1~2GHz Tx Mode, P _{in} =30dBm | -30 | -10 | - | uA |
| Control Voltage (H) | V _{CTL(H)} | CTL1, CTL2, CTL3 Terminals | 2.0 | 3.0 | V _{DD} | V |
| Control Voltage (L) | V _{CTL(L)} | CTL1, CTL2, CTL3 Terminals | 0 | 0 | 0.6 | V |
| Control Current | I _{CTL} | CTL1, CTL2, CTL3=V _{DD} or CTL1, CTL2, CTL3=0V | -1.3 | - | 1.3 | uA |
| Control terminal Input Impedance | R _{in} | CTL1, CTL2, CTL3 Terminals | 4 | - | - | MΩ |

* The voltage of this terminal should be supplied before or same time with other DC supplying terminals. (CTL1~3, V_{SS}).

■ ELECTRICAL CHARACTERISTICS 2 [Tx Mode]

General Conditions: $T_a=25^{\circ}\text{C}$, $V_{DD}=3.5\text{V}$, $V_{SS}=-2.5\text{V}$, $f_{in}=885\sim 940\text{MHz}$

Tested on PCB circuit as shown below.

Insertion loss of each connectors, striplines, and capacitors are excluded.

TX, RX, ANT1, ANT2, EXT1, EXT2: terminated (50Ω)

TER1, TER2: grounded by 10pF capacitor.

| PARAMETER | SYMBOL | CONDITION | MIN | TYP | MAX | UNITS |
|---------------------------------------|------------------------|--|-----|------|------|-------|
| Tx-ANT1 Insertion Loss | LOSS1 | $P_{in}=30\text{dBm}$ | - | 0.50 | 0.65 | dB |
| Tx-EXT1 Insertion Loss | LOSS2 | $P_{in}=30\text{dBm}$ | - | 0.50 | 0.65 | dB |
| Tx-Rx Isolation | ISL1 | $P_{in}=30\text{dBm}$ Tx-ANT1, Tx-EXT1 passing | 24 | 27 | - | dB |
| Tx-ANT1 Isolation | ISL2 | $P_{in}=30\text{dBm}$ Tx-EXT1 passing | 22 | 25 | - | dB |
| Tx-ANT2 Isolation | ISL3 | $P_{in}=30\text{dBm}$ Tx-ANT1, Tx-EXT1 passing | 33 | 38 | - | dB |
| Tx-EXT1 Isolation | ISL4 | $P_{in}=30\text{dBm}$ Tx-ANT1 passing | 21 | 24 | - | dB |
| Tx-EXT2 Isolation | ISL5 | $P_{in}=30\text{dBm}$ Tx-ANT1, Tx-EXT1 passing | 32 | 37 | - | dB |
| Input Power at 0.5dB Compression 1 | $P_{-0.5\text{dB}}(1)$ | Tx-ANT1, Tx-EXT1 passing | 33 | 35 | - | dBm |
| Adjacent Channel Leakage Power 1 | ACP1 | PDC Standard, $\pm 50\text{kHz}$ offset $P_{in}=30\text{dBm}$ Input Signal ACP=-64dBc @ 30dBm | - | -63 | -60 | dBc |
| Adjacent Channel Leakage Power 2 | ACP2 | PDC Standard, $\pm 100\text{kHz}$ offset $P_{in}=30\text{dBm}$ Input Signal ACP=-76dBc @ 30dBm | - | -74 | -70 | dBc |
| 2nd Harmonics 1 | $2f_0(1)$ | $P_{in}=30\text{dBm}$ Input Signal 2nd Harmonics=-70dBc | - | -65 | -63 | dBc |
| 3rd Harmonics 1 | $3f_0(1)$ | $P_{in}=30\text{dBm}$ Input Signal 3rd Harmonics=-100dBc | - | -64 | -62 | dBc |
| VSWR 1 | VSWR1 | Tx-ANT1, Tx-EXT1 passing | - | 1.2 | 1.5 | |
| Switching Time 1 | T_D1 | CTL1~3 | - | 120 | 500 | nsec |

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■ELECTRICAL CHARACTERISTICS 3 [Rx Mode]

General Conditions: $T_a=25^{\circ}\text{C}$, $V_{DD}=3.5\text{V}$, $V_{SS}=0\text{V}$, $f_{in}=810\sim 885\text{MHz}$

Tested on PCB circuit as shown below.

Insertion loss of each connectors, striplines, and capacitors are excluded.

TX, RX, ANT1, ANT2, EXT1, EXT2: terminated (50Ω)

TER1, TER2: grounded by 10pF capacitor.

| PARAMETER | SYMBOL | CONDITION | MIN | TYP | MAX | UNITS |
|----------------------------------|----------------------|--|-----|------|------|-------|
| Rx-ANT1 Insertion Loss | LOSS3 | $P_{in}=10\text{dBm}$ | - | 0.65 | 0.80 | dB |
| Rx-ANT2 Insertion Loss | LOSS4 | $P_{in}=10\text{dBm}$ | - | 0.60 | 0.75 | dB |
| Rx-EXT1 Insertion Loss | LOSS5 | $P_{in}=10\text{dBm}$ | - | 0.70 | 0.85 | dB |
| Rx-EXT2 Insertion Loss | LOSS6 | $P_{in}=10\text{dBm}$ | - | 0.65 | 0.80 | dB |
| Rx-ANT1 Isolation | ISL6 | $P_{in}=10\text{dBm}$ Rx-ANT2, Rx-EXT1, Rx-EXT2 passing | 22 | 26 | - | dB |
| Rx-ANT2 Isolation | ISL7 | $P_{in}=10\text{dBm}$ Rx-ANT1, Rx-EXT1, Rx-EXT2 passing | 24 | 30 | - | dB |
| Rx-EXT1 Isolation | ISL8 | $P_{in}=10\text{dBm}$ Rx-ANT1, Rx-ANT2, Rx-EXT2 passing | 22 | 26 | - | dB |
| Rx-EXT2 Isolation | ISL9 | $P_{in}=10\text{dBm}$ Rx-ANT1, Rx-ANT2, Rx-EXT1 passing | 22 | 26 | - | dB |
| Input Power at 1dB Compression 1 | $P_{-1\text{dB}}(1)$ | Rx-ANT1, Rx-ANT2, Rx-EXT1, Rx-EXT2 passing | 21 | 26 | - | dBm |
| VSWR 2 | VSWR2 | RX-ANT1, RX-ANT2, RX-EXT1, RX-EXT2 passing | - | 1.2 | 1.6 | |
| Switching Time 2 | T_D2 | CTL1~3 | - | 120 | 500 | nsec |

■ELECTRICAL CHARACTERISTICS 4 [LNA]

General Conditions: $T_a=25^{\circ}\text{C}$, $V_{DD}=3.5\text{V}$, $V_{SS}=0\text{V}$, $f_{in}=820\text{MHz}$

Tested on PCB circuit as shown below.

| PARAMETER | SYMBOL | CONDITION | MIN | TYP | MAX | UNITS |
|---|----------------------|--------------------------------|------|------|------|-------|
| Operation Frequency | f_{RF} | | 810 | - | 885 | MHz |
| Drain Voltage | V_{DD3} | | 2.5 | 2.7 | 4.5 | V |
| Current Consumption | I_{DD3} | No RF input | - | 2.7 | 3.6 | mA |
| Small Signal Gain | Gain | | 16.0 | 17.5 | 18.5 | dB |
| Gain Flatness | G_{flat} | $f_{RF}=810\sim 885\text{MHz}$ | - | 0.5 | 1.0 | dB |
| Noise Figure | NF | | - | 1.4 | 1.6 | dB |
| Pout at 1dB Gain Compression Point | $P_{-1\text{dB}}(2)$ | | -3.0 | +1.0 | - | dBm |
| Input 3 rd order Intercept Point | IIP3 | | -8.0 | -4.5 | - | dBm |
| LNAIN Port VSWR | $VSWR_i$ | | - | 1.5 | 2.5 | |
| LNAOUT Port VSWR | $VSWR_o$ | | - | 1.5 | 2.5 | |

■ TERMINAL INFORMATION

| PIN NO. | SYMBOL | DESCRIPTIONS |
|---|-----------------|---|
| 4 | CTL1 | Control signal input terminal of high impedance C-MOS logic. Logic level: High; more than +2V, Low; 0~+0.6V. Please connect to GND or V _{DD} with 100kΩ if potential is open or uncertain. |
| 5 | CTL2 | |
| 6 | CTL3 | |
| 7 | V _{SS} | Negative supply terminal. Negative voltage of -3.5~-2.0V must be supplied on Tx mode. This terminal is isolated on Rx mode, so open or -2.5~0V condition can be used. Please connect bypass capacitor with GND to keep RF performance. |
| 9 | V _{DD} | Positive supply terminal. The voltage of this terminal should be supplied before or same time with other DC supplying terminals (CTL1~3, V _{SS}). The bias voltage should be +2.7~+5.0V. Please connect bypass capacitor with GND to keep RF performance. |
| 11 | EXT2 | RF port for Rx signal. A DC cut capacitor (56pF~100pF) is required to block V _{DD} voltage. |
| 13 | EXT1 | RF port for Tx/Rx signal. A DC cut capacitor (56pF~100pF) is required to block V _{DD} voltage. |
| 15 | TX | Tx power input terminal. A DC cut capacitor is required to block V _{DD} voltage, and also an external matching circuit is required to improve VSWR(See Application circuit). |
| 17 | TER2 | A termination terminal for ANT1 in case ANT2 is in use. The influence of ANT1 against ANT2 is reduced. A DC cut capacitor (10pF) is required to block V _{DD} voltage. |
| 19 | ANT1 | RF port for Tx/Rx signal. A DC cut capacitor (56pF~100pF) is required to block V _{DD} voltage. |
| 21 | RX | Rx output terminal. A DC cut capacitor is required to block V _{DD} voltage, and also an external matching circuit is required to improve VSWR(See Application circuit). |
| 23 | ANT2 | RF port for Rx signal. A DC cut capacitor (56pF~100pF) is required to block V _{DD} voltage. |
| 25 | TER1 | A termination terminal for ANT2 in case ANT1 is in use. The influence of ANT2 against ANT1 is reduced. A DC cut capacitor (10pF) is required to block V _{DD} voltage. |
| 26,27 | GND(LNA) | Ground terminal of LNA. Please place ground plane close to this pin for good RF performance. |
| 28 | LNAIN | LNA input terminal. An external matching circuit is required. |
| 30 | LNAOUT | LNA output terminal. An external matching circuit with LNA biasing element L3, L4 as in application circuit is required. |
| 31 | EXTCAP | Bypass capacitor terminal of LNA. Please place C9 as in application circuit close to this terminal. |
| 1,2,3,8,10, 12,14,16,1 8,20,22,24, 29,32 | GND | Ground terminal. Please connect to ground plane as close as possible for good RF performance. |

■ TRUTH TABLE

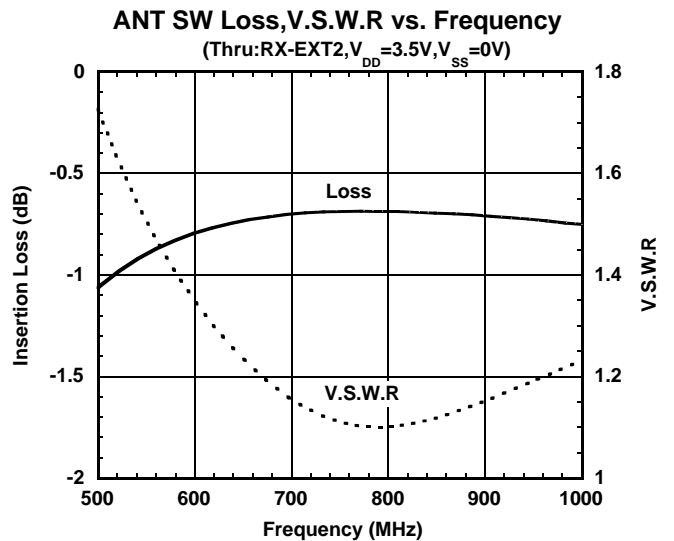
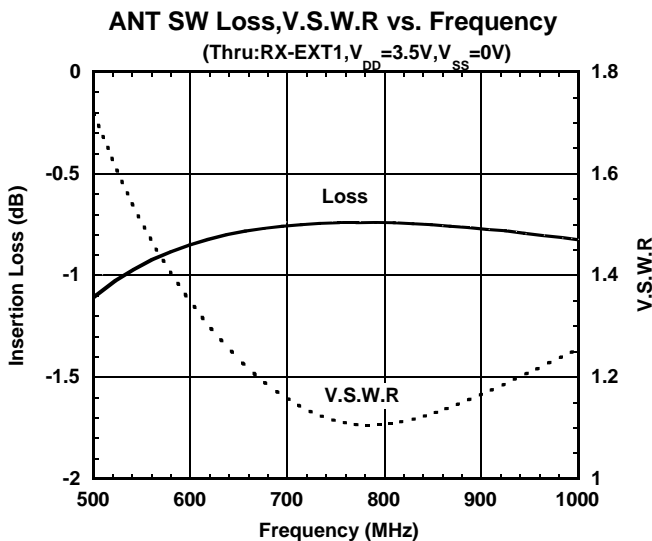
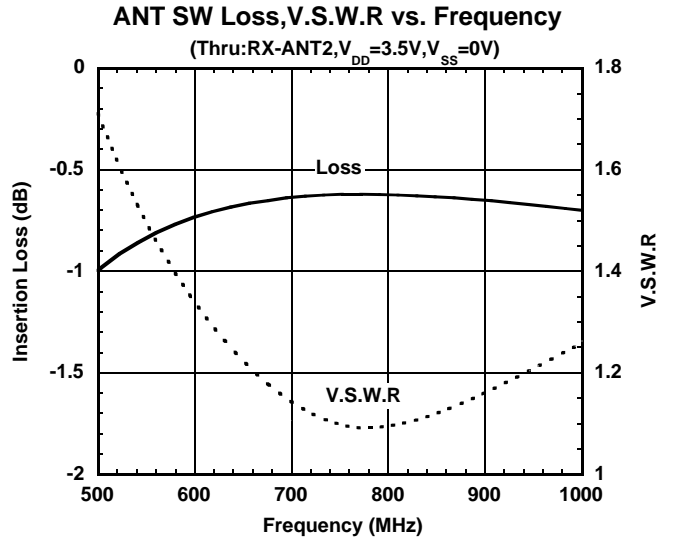
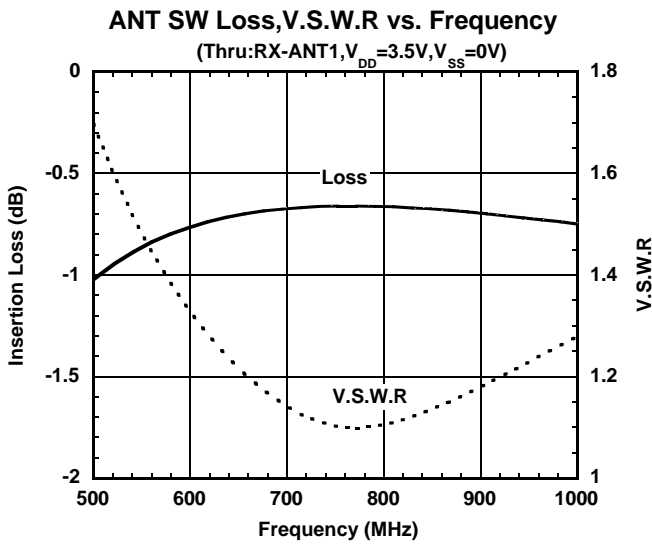
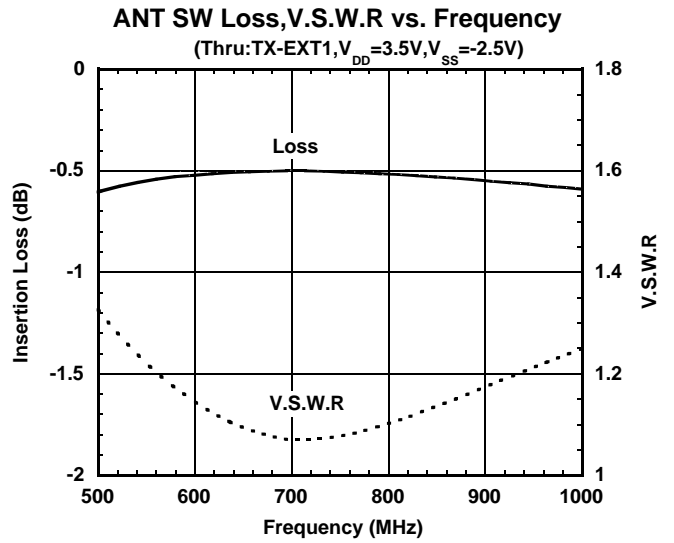
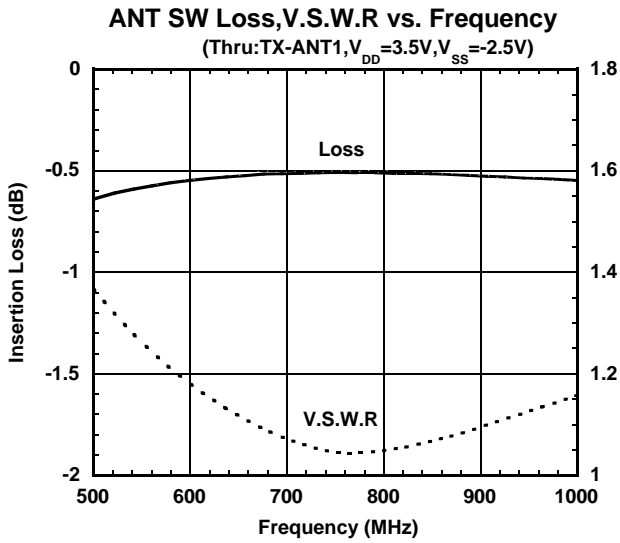
"H"=V_{CTL}(H), "L"=V_{CTL}(L), "X"=H or L

| ROUTE | CONTROL INPUT | | | CONTROL OUTPUT | | | | | | | | |
|---------|---------------|-----------|--------|----------------|-----|-----|-----|-----|-----|-----|-----|-----|
| | Tx/Rx | Diversity | IN/OUT | SW1 | SW2 | SW3 | SW4 | SW5 | SW6 | SW7 | SW8 | SW9 |
| | CTL1 | CTL2 | CTL3 | | | | | | | | | |
| Tx-ANT1 | H | X | H | OFF | OFF | OFF | ON | ON | OFF | OFF | OFF | ON |
| Tx-EXT1 | H | X | L | OFF | OFF | ON | OFF | ON | ON | ON | OFF | OFF |
| Rx-ANT1 | L | L | H | OFF | OFF | ON | OFF | ON | OFF | ON | ON | ON |
| Rx-ANT2 | L | H | H | ON | OFF | OFF | OFF | OFF | ON | ON | ON | ON |
| Rx-EXT1 | L | L | L | OFF | OFF | OFF | ON | ON | ON | OFF | ON | OFF |
| Rx-EXT2 | L | H | L | OFF | ON | OFF | OFF | ON | ON | ON | ON | ON |

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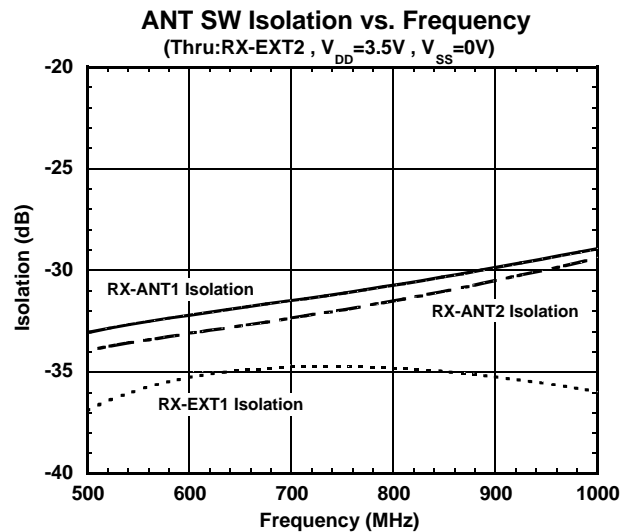
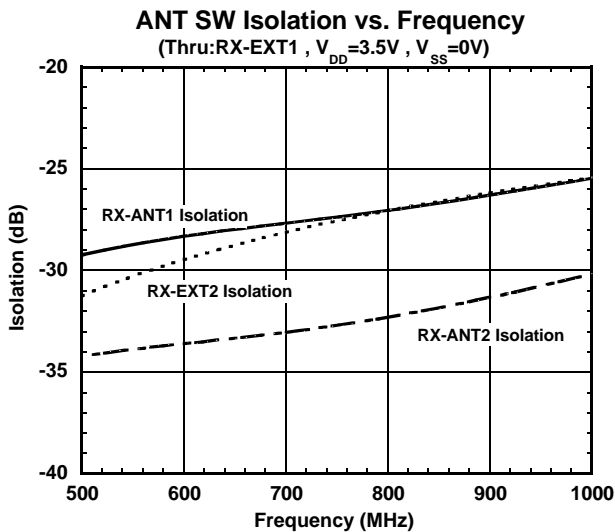
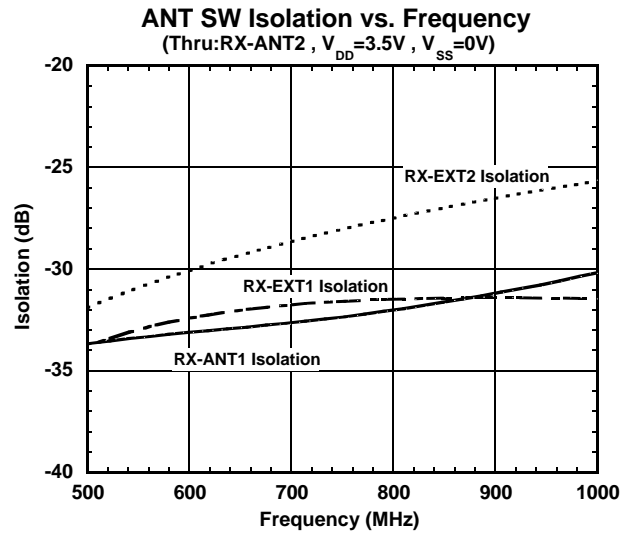
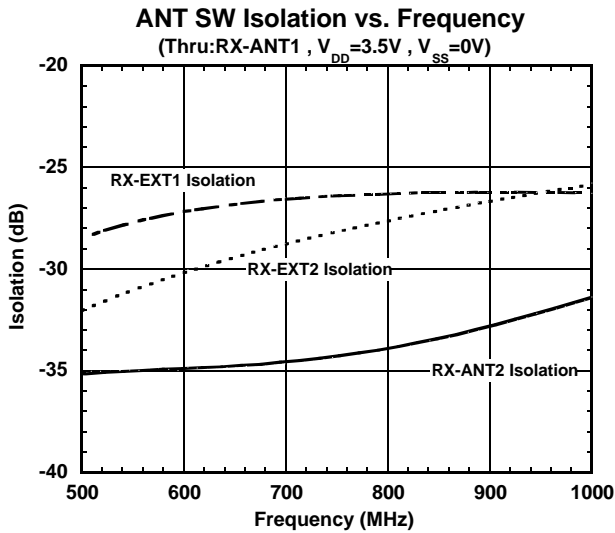
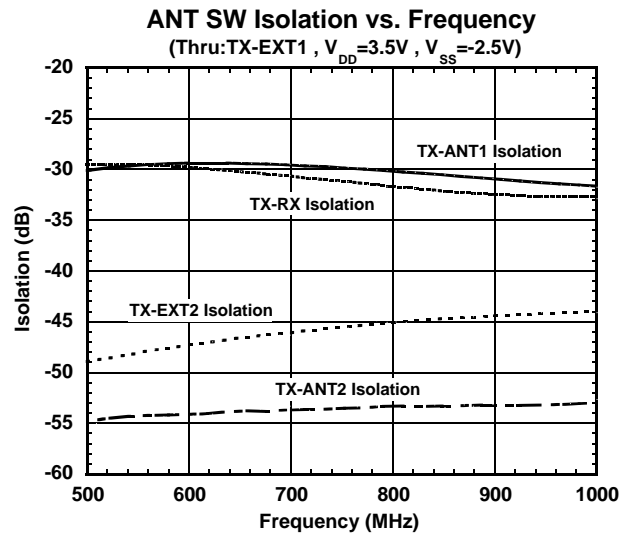
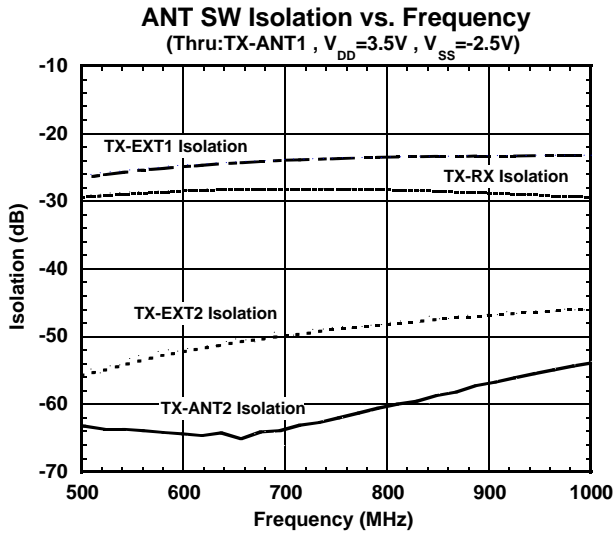
■ TYPICAL CHARACTERISTICS (ANTENNA SWITCH)

Measured on the PCB evaluation circuit, losses of circuits are eliminated.



■ TYPICAL CHARACTERISTICS (ANTENNA SWITCH)

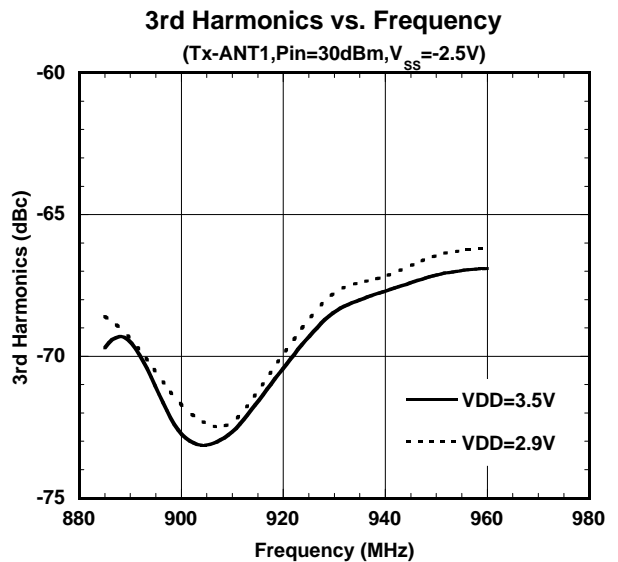
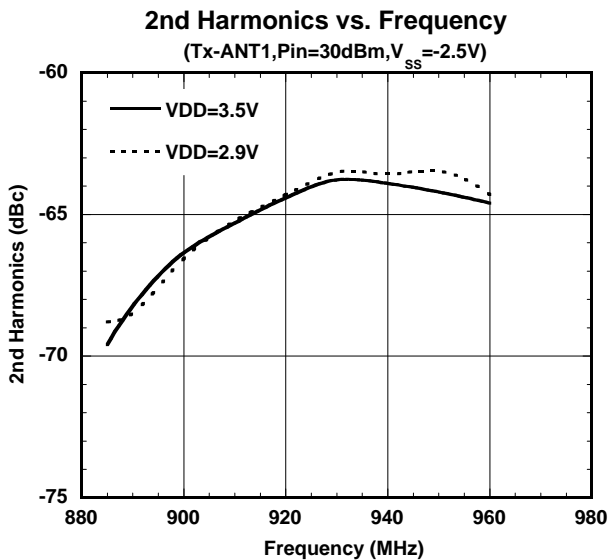
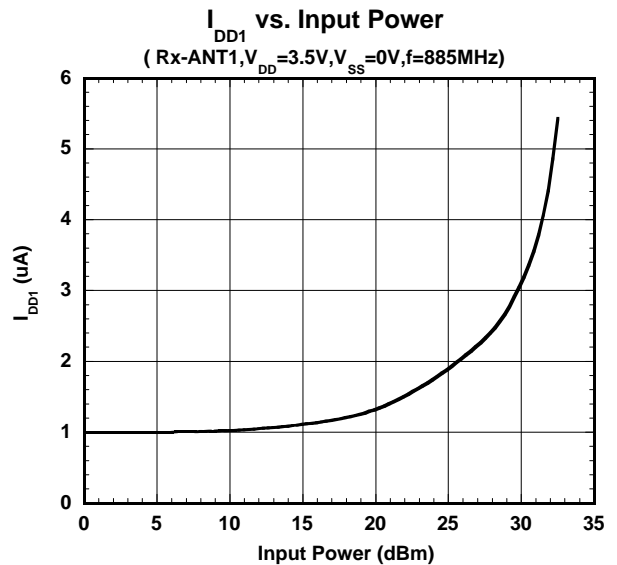
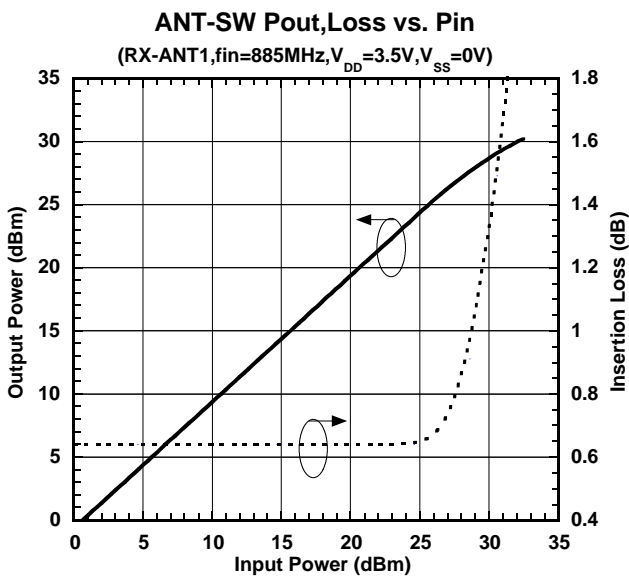
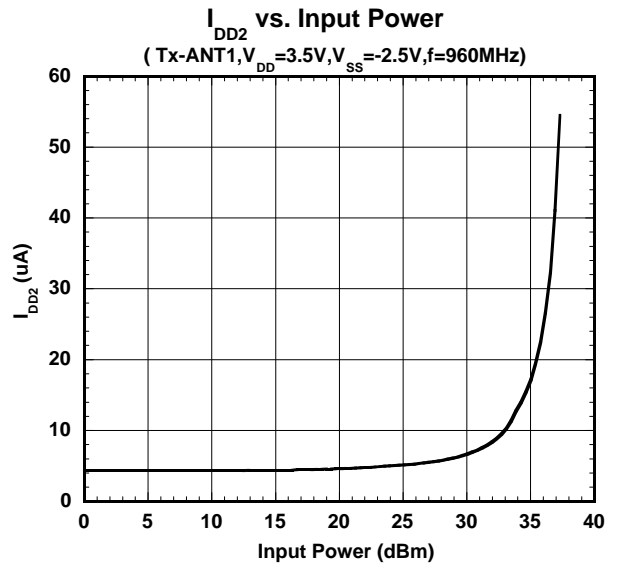
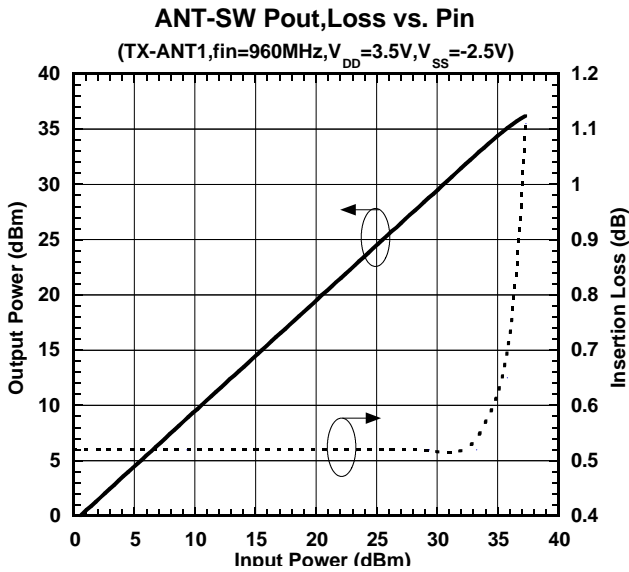
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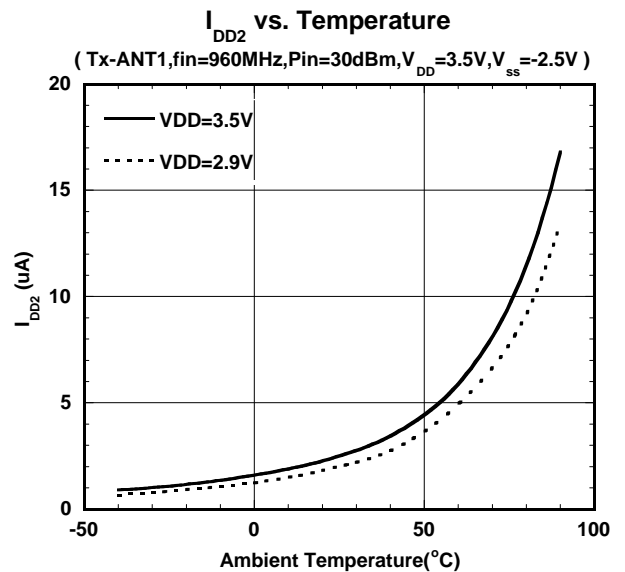
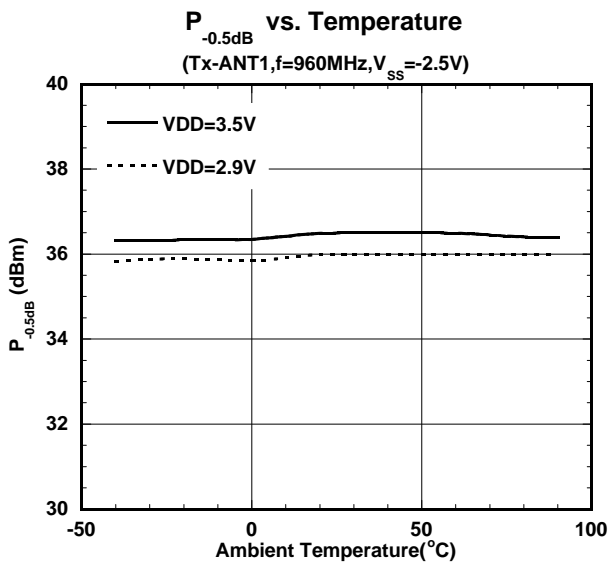
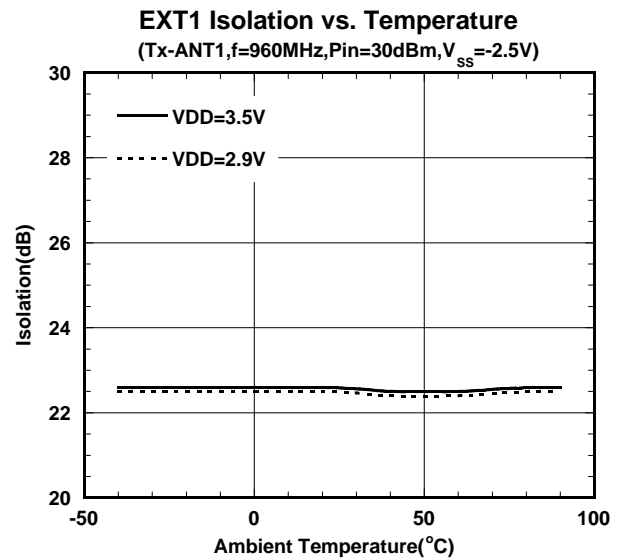
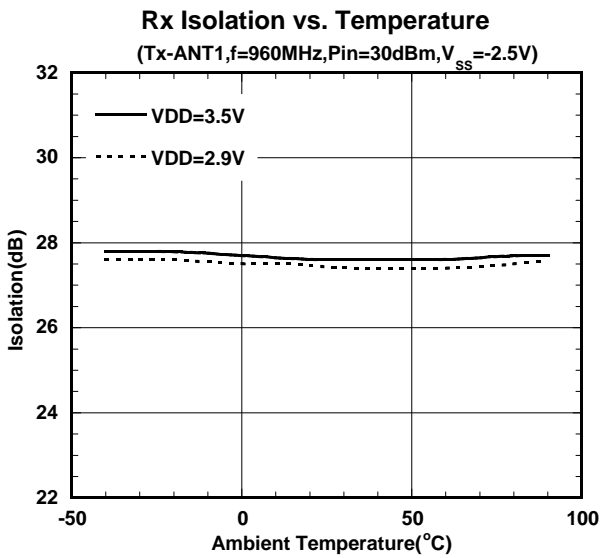
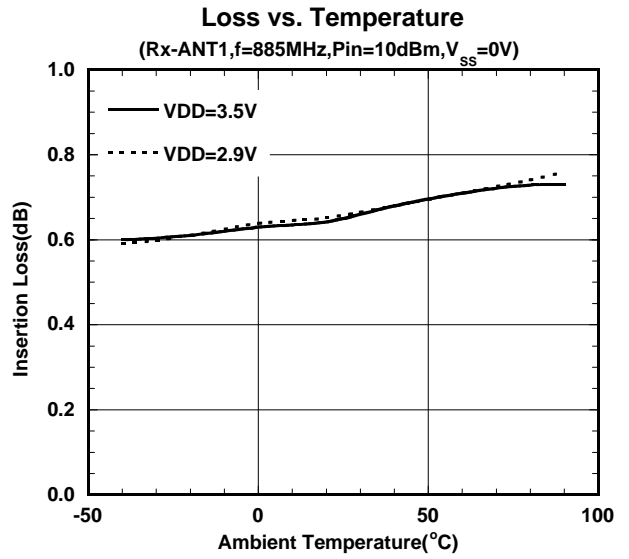
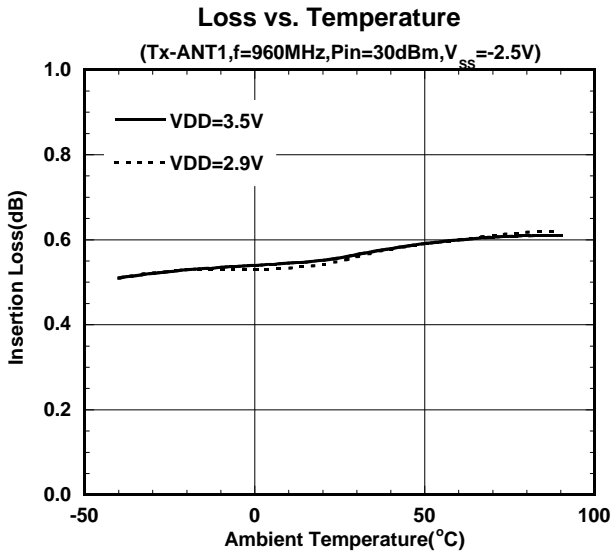
■ TYPICAL CHARACTERISTICS (ANTENNA SWITCH)

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■ TYPICAL CHARACTERISTICS (ANTENNA SWITCH)

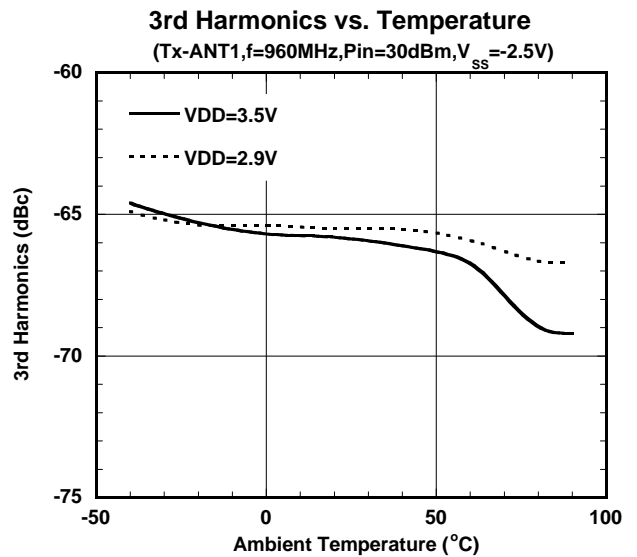
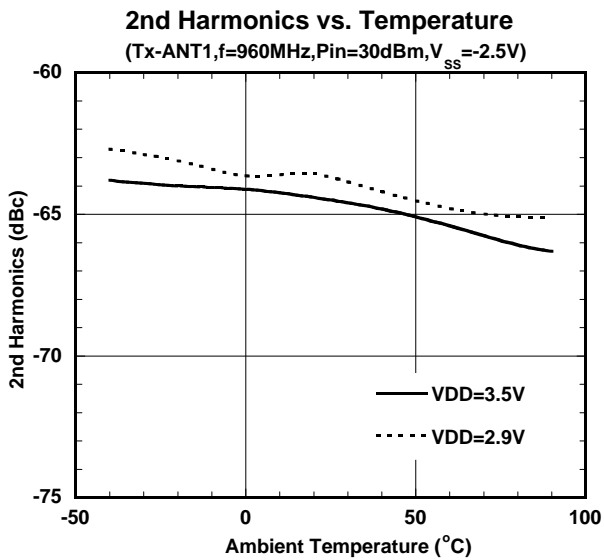
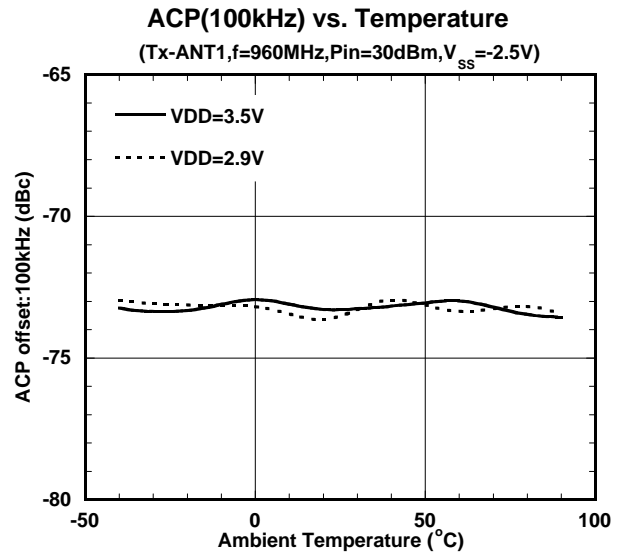
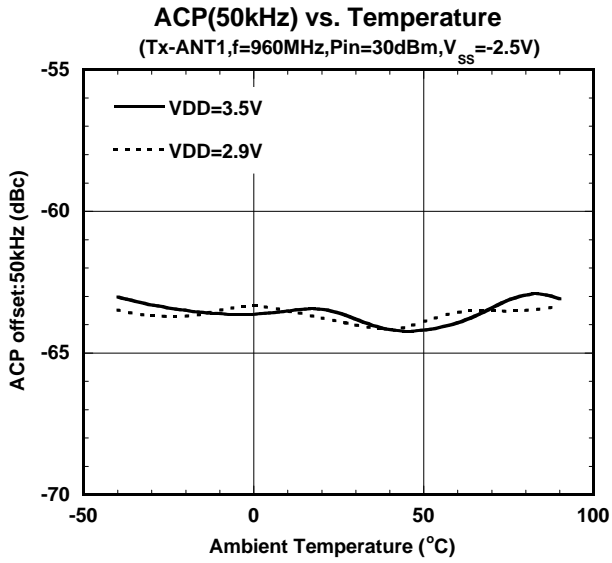
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Measured on the PCB evaluation circuit.

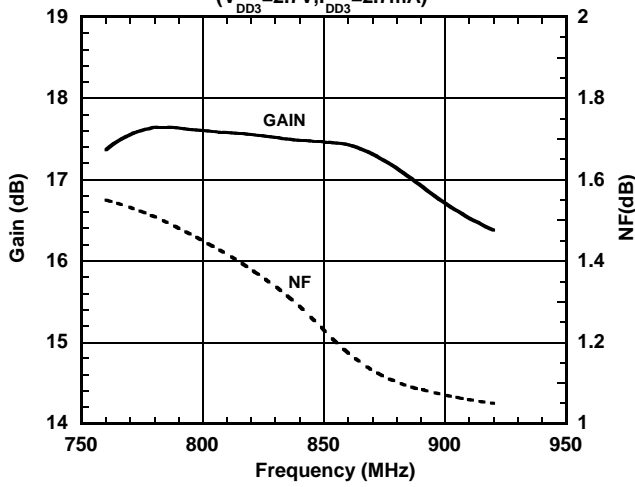


TYPICAL CHARACTERISTICS (LNA)

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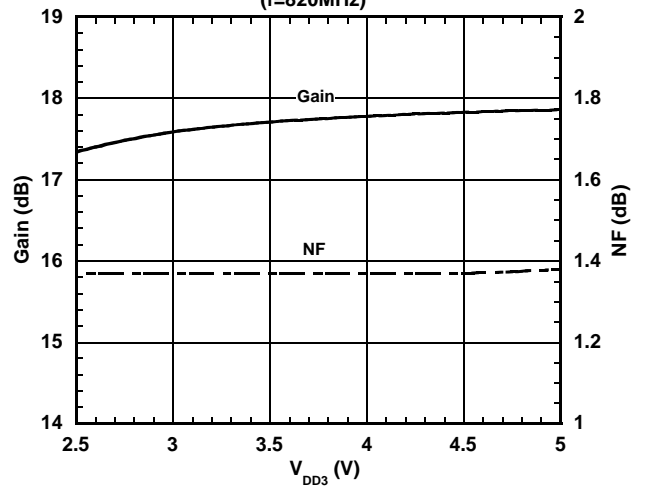
LNA NF, Gain vs. Frequency

($V_{DD3}=2.7V, I_{DD3}=2.7mA$)



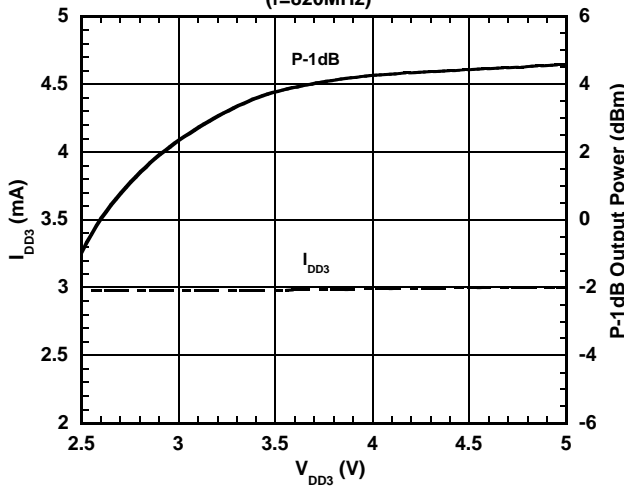
LNA Gain, NF vs. V_{DD3}

($f=820MHz$)



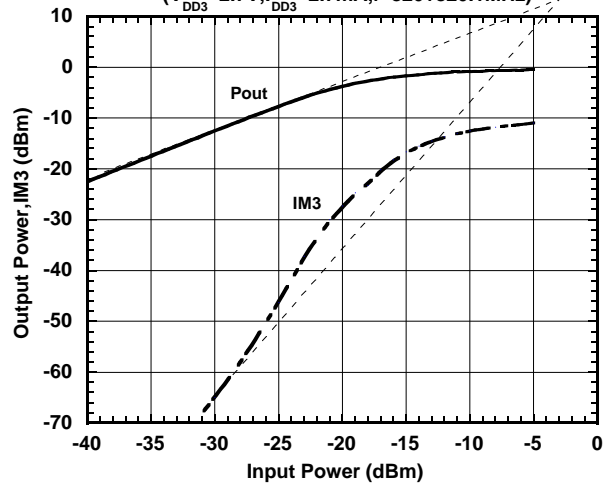
LNA I_{DD3} , P-1dB vs. V_{DD3}

($f=820MHz$)



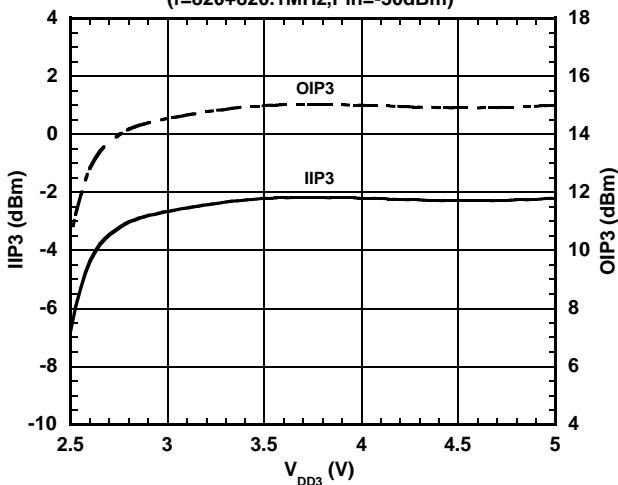
LNA Pout, IM3 vs. Pin

($V_{DD3}=2.7V, I_{DD3}=2.7mA, f=820+820.1MHz$)



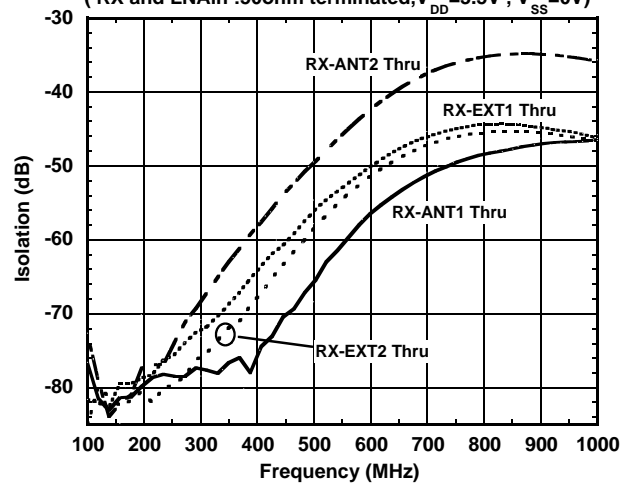
LNA IIP3, OIP3 vs. V_{DD3}

($f=820+820.1MHz, Pin=-30dBm$)



ANT SW - LNA OUT Isolation vs. Frequency

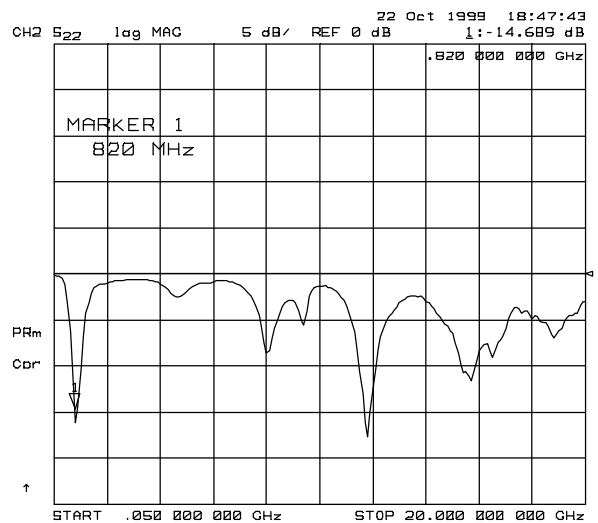
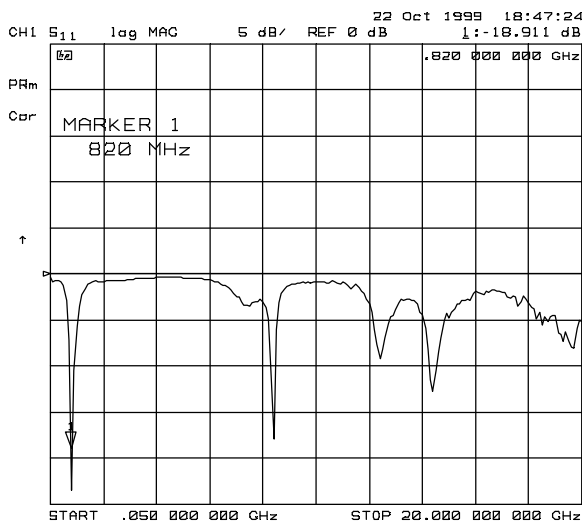
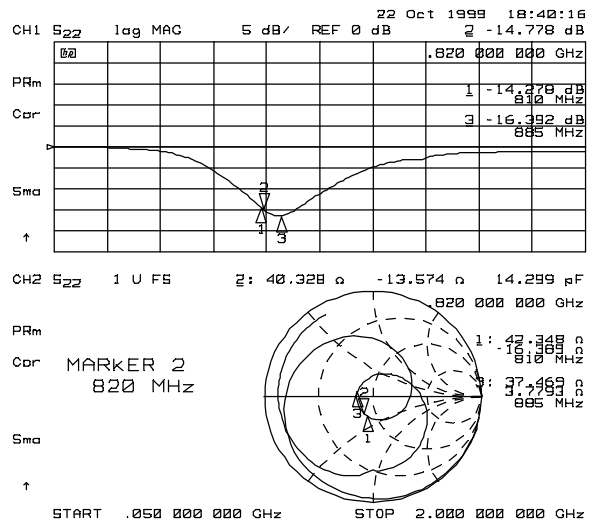
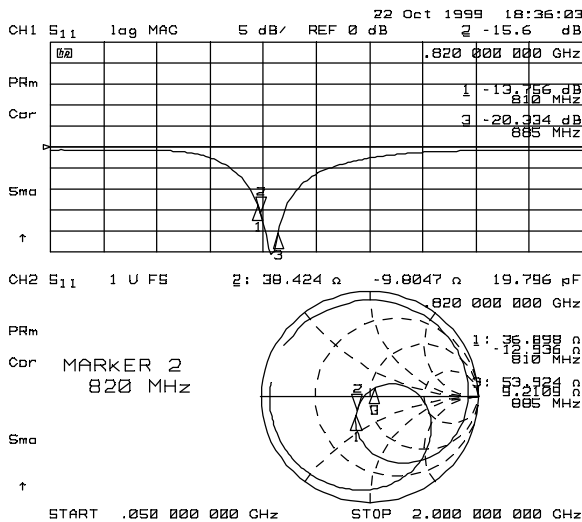
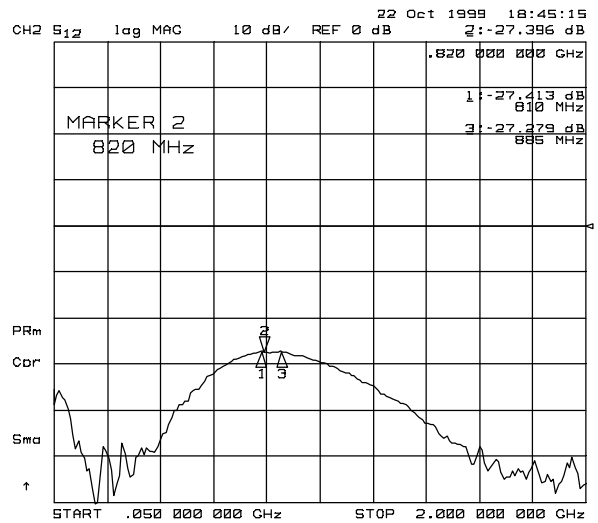
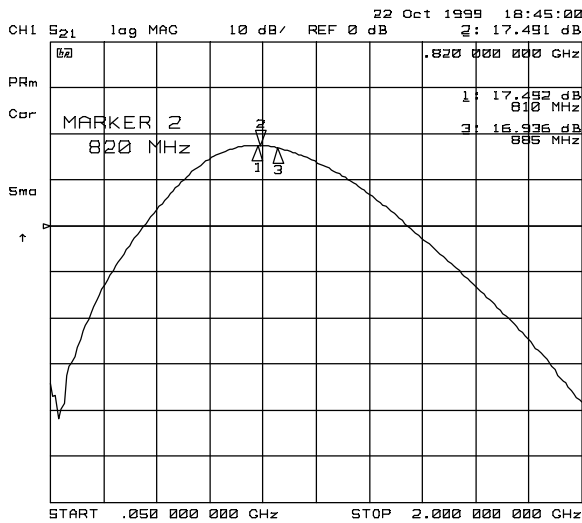
(RX and LNAin :50ohm terminated, $V_{DD}=3.5V, V_{SS}=0V$)



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TYPICAL CHARACTERISTICS (LNA)

Measured on the PCB evaluation circuit. $V_{DD3}=2.7V$

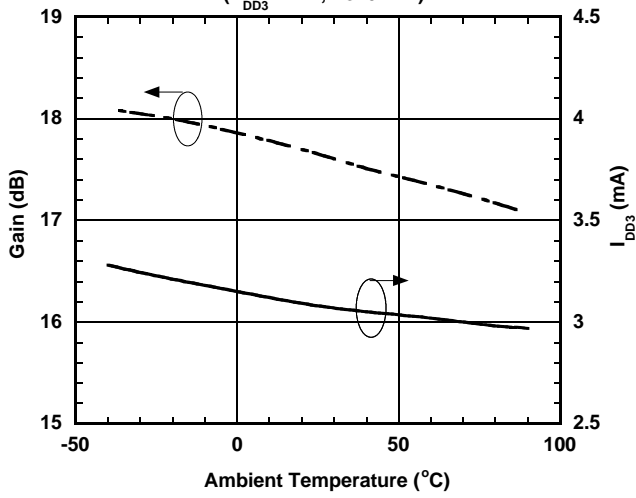


■ TYPICAL CHARACTERISTICS (LNA)

Measured on the PCB evaluation circuit.

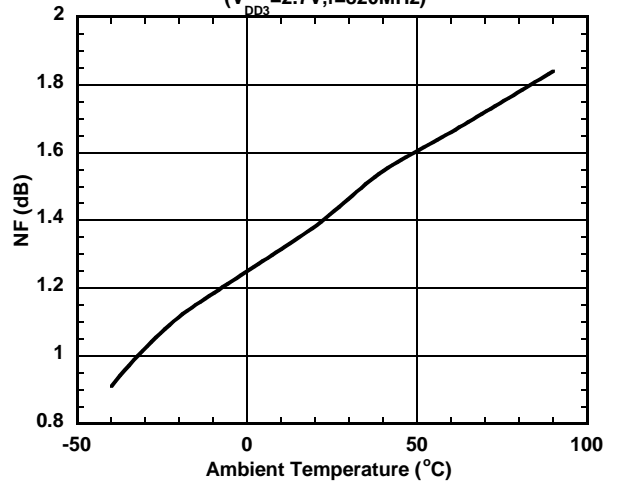
LNA Gain, I_{DD3} vs. Temperature

($V_{DD3}=2.7V, f=820MHz$)



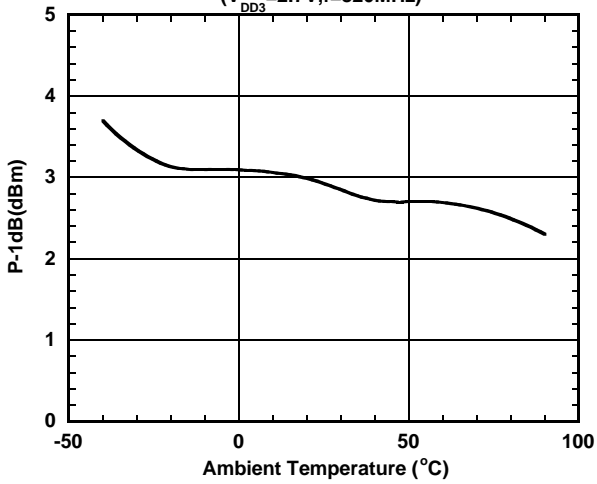
LNA NF vs. Temperature

($V_{DD3}=2.7V, f=820MHz$)



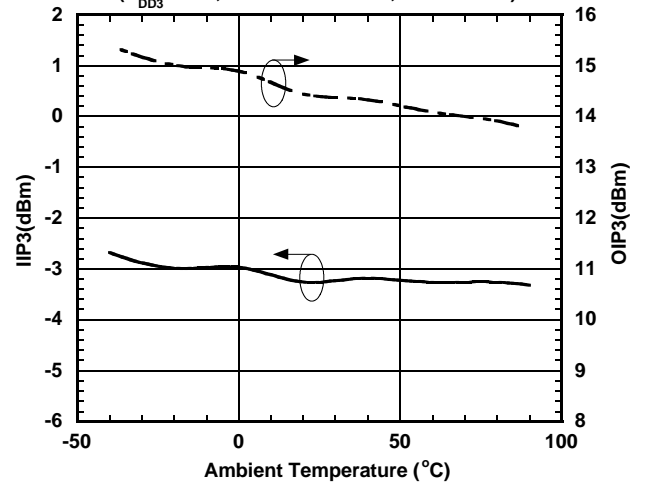
LNA P-1dB vs. Temperature

($V_{DD3}=2.7V, f=820MHz$)



LNA IIP3, OIP3 vs. Temperature

($V_{DD3}=2.7V, f=820.0+820.1MHz, Pin=-30dBm$)



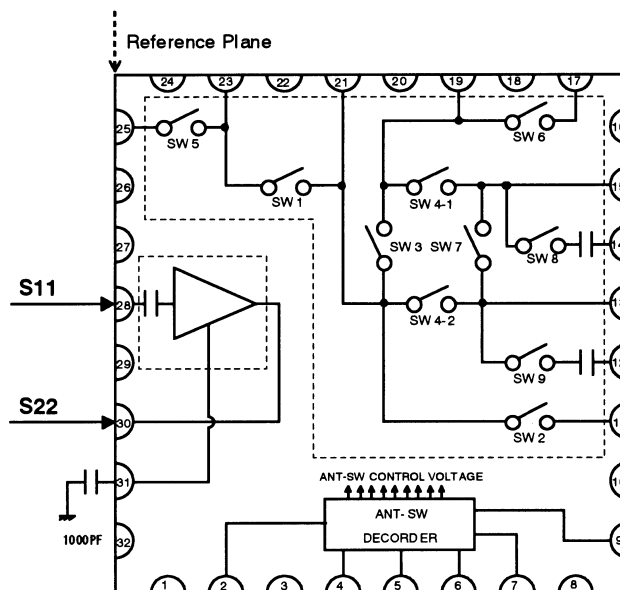
NJG1707PG1

■ TYPICAL CHARACTERISTICS (LNA)

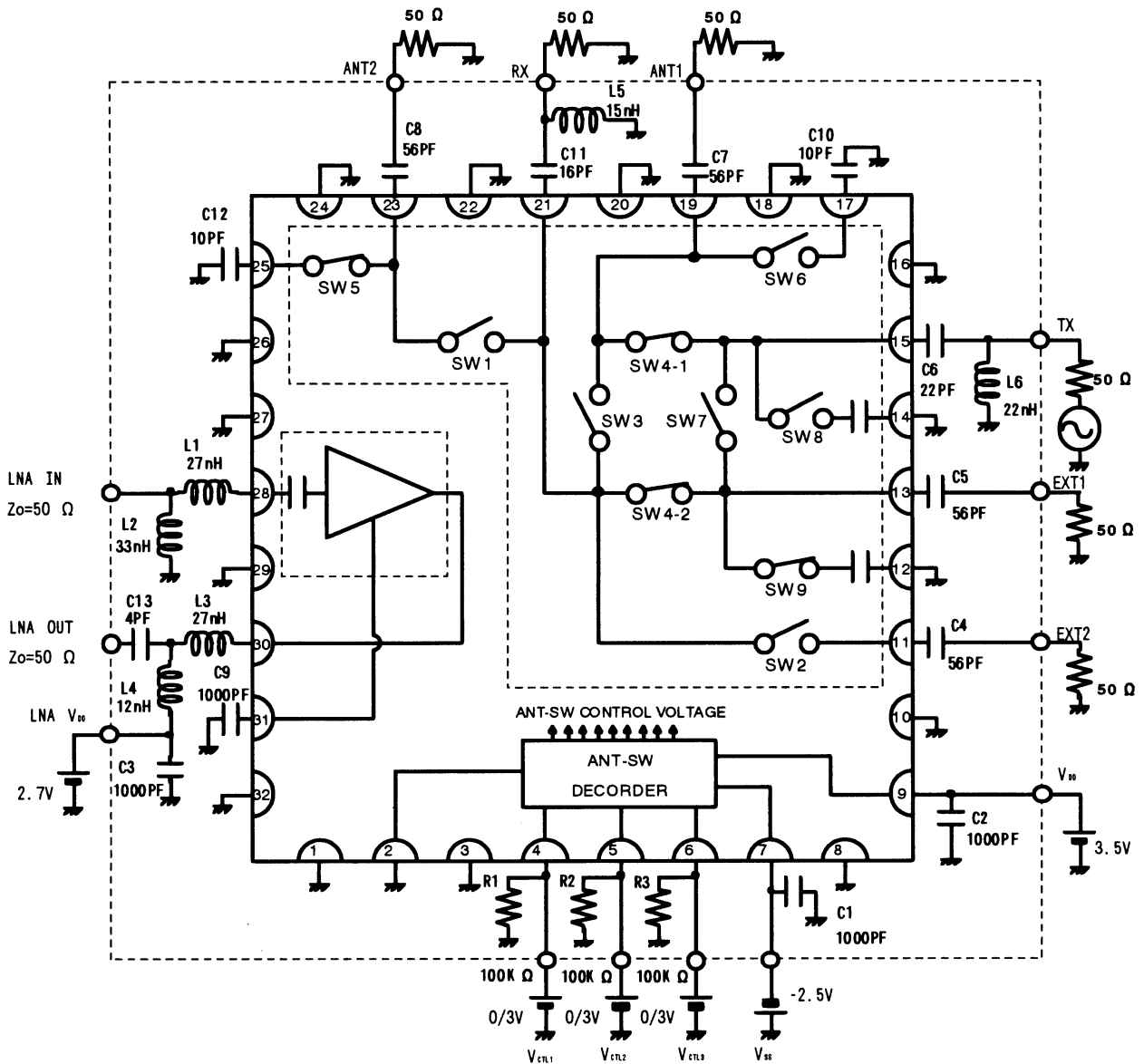
LNA Scattering Parameter Table

| Freq. (GHz) | S11 | | S21 | | S12 | | S22 | |
|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| | mag. (unit) | ang. (deg.) | mag. (unit) | ang. (deg.) | mag. (unit) | ang. (deg.) | mag. (unit) | ang. (deg.) |
| 0.1 | 1.000 | -2.22 | 2.147 | 176.00 | 0.009 | 48.67 | 0.949 | -1.04 |
| 0.2 | 0.987 | -5.10 | 2.087 | 168.16 | 0.008 | 38.98 | 0.940 | -3.71 |
| 0.3 | 0.985 | -7.12 | 2.053 | 161.77 | 0.005 | 68.44 | 0.954 | -4.61 |
| 0.4 | 0.987 | -10.49 | 2.079 | 154.25 | 0.010 | 61.48 | 0.940 | -7.50 |
| 0.5 | 0.967 | -12.19 | 2.020 | 147.74 | 0.008 | 58.51 | 0.939 | -8.86 |
| 0.6 | 0.967 | -15.33 | 1.998 | 141.28 | 0.007 | 57.29 | 0.931 | -11.32 |
| 0.7 | 0.943 | -17.89 | 1.947 | 134.57 | 0.010 | 62.79 | 0.921 | -13.70 |
| 0.8 | 0.928 | -20.65 | 1.899 | 128.63 | 0.010 | 57.35 | 0.918 | -15.28 |
| 0.9 | 0.911 | -23.45 | 1.845 | 122.18 | 0.013 | 61.22 | 0.924 | -18.33 |
| 1 | 0.894 | -26.19 | 1.795 | 116.45 | 0.013 | 64.15 | 0.914 | -20.15 |
| 1.1 | 0.882 | -28.43 | 1.723 | 111.16 | 0.013 | 68.15 | 0.923 | -22.40 |
| 1.2 | 0.867 | -30.91 | 1.675 | 105.79 | 0.014 | 66.63 | 0.910 | -24.64 |
| 1.3 | 0.861 | -33.29 | 1.613 | 100.76 | 0.014 | 69.43 | 0.927 | -26.98 |
| 1.4 | 0.853 | -35.74 | 1.556 | 95.80 | 0.015 | 65.80 | 0.916 | -28.74 |
| 1.5 | 0.848 | -37.65 | 1.498 | 90.90 | 0.015 | 69.41 | 0.921 | -30.73 |
| 1.6 | 0.843 | -39.63 | 1.442 | 86.45 | 0.017 | 75.17 | 0.915 | -32.14 |
| 1.7 | 0.834 | -41.23 | 1.384 | 82.25 | 0.018 | 76.93 | 0.913 | -33.86 |
| 1.8 | 0.832 | -42.72 | 1.344 | 78.49 | 0.018 | 80.33 | 0.913 | -35.13 |
| 1.9 | 0.823 | -43.91 | 1.288 | 74.67 | 0.021 | 84.19 | 0.908 | -36.37 |
| 2 | 0.816 | -44.93 | 1.253 | 71.30 | 0.022 | 82.05 | 0.912 | -37.14 |

$V_{DD3}=2.7V$, $I_{DD3}=3mA$, $Z_0=50\Omega$



RECOMMENDED CIRCUIT (Tx-ANT1 PASSING)

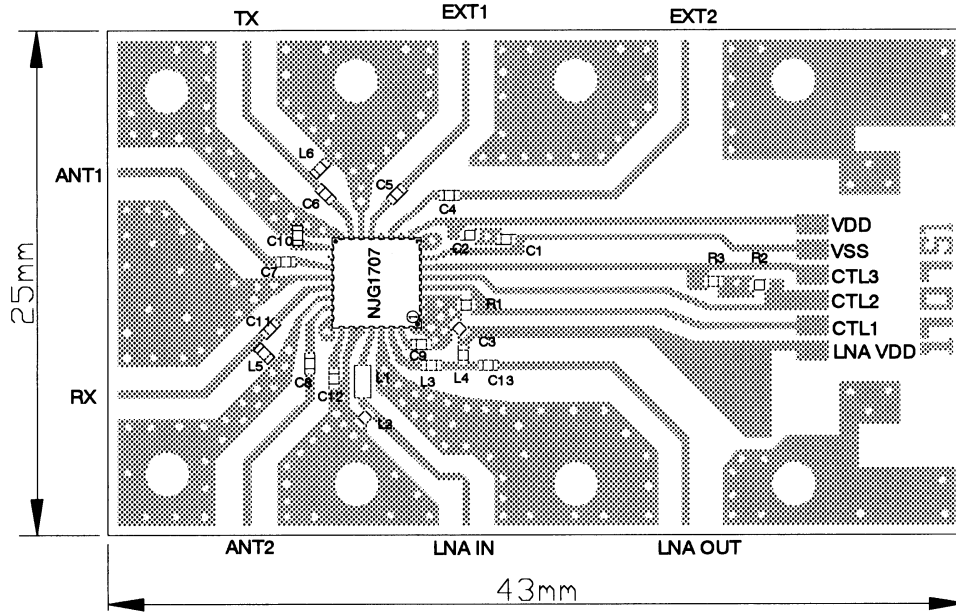


PRECAUTIONS

Please connect resistors R1~R3 between VCTL1~VCTL3 terminals (Pin#4, 5, 6) and GND or V_{DD} only when CTL1~CTL3 voltage is required to clip to H or L level.

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RECOMMENDED PCB DESIGN



PCB: FR-4, t= 0.2mm
Stripline width: 0.4mm

Board total loss (Capacitors, Connectors, and PCB)

| Pass route | 800MHz band (dB) | Frequency (MHz) |
|------------|------------------|-----------------|
| TX-ANT1 | 0.30 | 960 |
| TX-EXT1 | 0.26 | |
| RX-ANT1 | 0.28 | 885 |
| RX-ANT2 | 0.29 | |
| RX-EXT1 | 0.32 | |
| RX-EXT2 | 0.37 | |

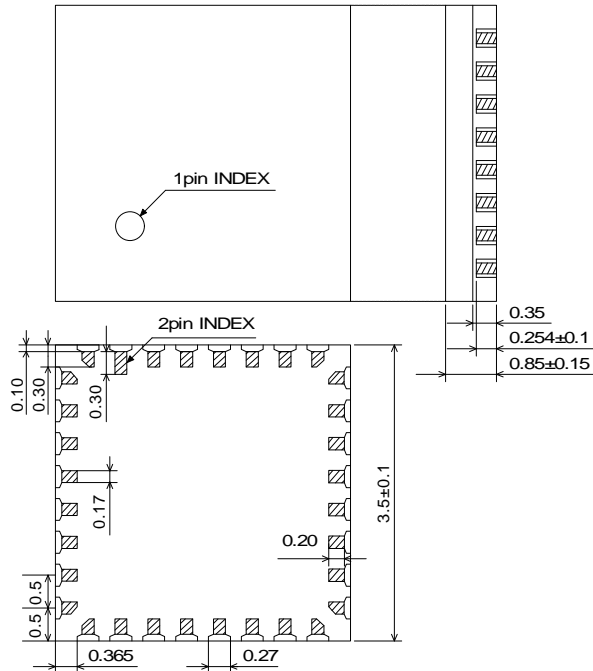
PARTS LIST

| PARTS ID | VALUE | COMMENT |
|----------------|--------|---------------------|
| R1-R3 | 100Ω | 1005 Size |
| C1~3, C9 | 1000pF | MURATA(GRM36) |
| C4, C5, C7, C8 | 22pF | MURATA(GRM36) |
| C10, C12 | 10pF | MURATA(GRM36) |
| C11 | 16pF | MURATA(GRM36) |
| C13 | 4pF | MURATA(GRM36) |
| L1 | 27nH | TAIYO-YUDEN(HK1608) |
| L2 | 33nH | TAIYO-YUDEN(HK1005) |
| L3 | 27nH | TAIYO-YUDEN(HK1005) |
| L4 | 12nH | TAIYO-YUDEN(HK1005) |
| L5 | 15nH | TAIYO-YUDEN(HK1005) |
| L6 | 22nH | TAIYO-YUDEN(HK1005) |

PRECAUTIONS

- [1] The bypass capacitors should be connected to the V_{DD}, V_{SS} terminals as close as possible respectively.
- [2] For good RF performance, the ground terminals should be directly connected to the ground patterns and through-holes as close as possible by using relatively wide pattern.

PACKAGE OUTLINE (FFP32-G1)



| | |
|--------------|---------------|
| UNITS | : mm |
| PCB | : Ceramic |
| OVER COAT | : Epoxy resin |
| LEAD SURFACE | : Au |
| WEIGHT | : 30mg |

Cautions on using this product

This product contains Gallium-Arsenide (GaAs) which is a harmful material.

- Do NOT eat or put into mouth.
- Do NOT dispose in fire or break up this product.
- Do NOT chemically make gas or powder with this product.
- To waste this product, please obey the relating law of your country.

[CAUTION]

The specifications on this databook are only given for information, without any guarantee as regards either mistakes or omissions. The application circuits in this databook are described only to show representative usages of the product and not intended for the guarantee or permission of any right including the industrial rights.

This product may be damaged with electric static discharge (ESD) or spike voltage. Please handle