

3A Bus Termination Regulator

GENERAL DESCRIPTION

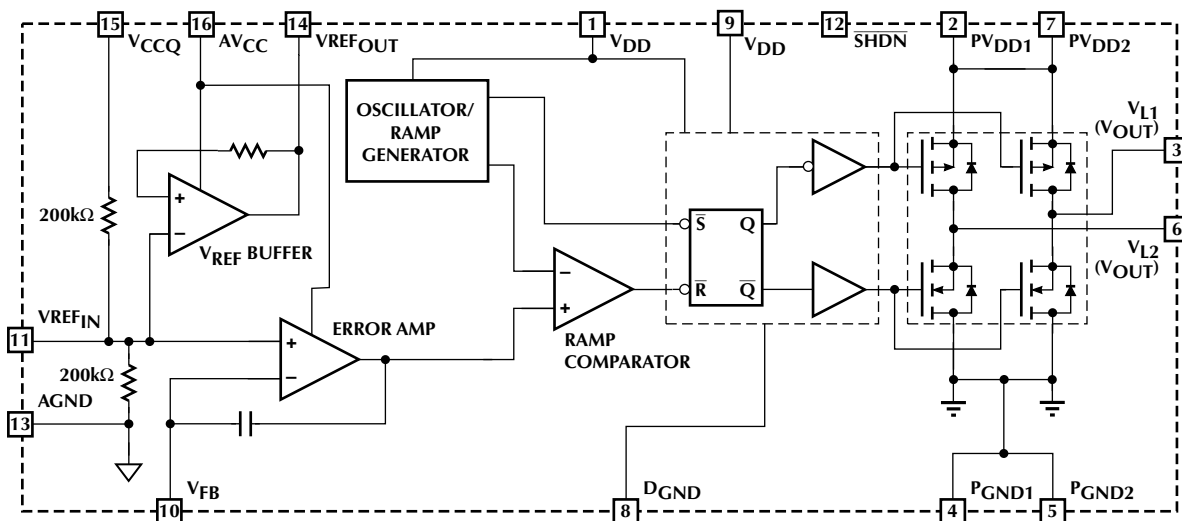
The ML6554 switching regulator is designed to convert voltage supplies ranging from 2.3V to 4V into a desired output voltage or termination voltage for various applications. The ML6554 can be implemented to produce regulated output voltages in two different modes. In the default mode, when the V_{REF} pin is open, the ML6554 output voltage is 50% of the voltage applied to V_{CCQ} . The ML6554 can also be used to produce various user-defined voltages by forcing a voltage on the $V_{REF_{IN}}$ pin. In this case, the output voltage follows the input $V_{REF_{IN}}$ voltage. The switching regulator is capable of sourcing or sinking up to 3A of current while regulating an output V_{TT} voltage to within 3% or less.

The ML6554, used in conjunction with series termination resistors, provides an excellent voltage source for active termination schemes of high speed transmission lines as those seen in high speed memory buses and distributed backplane designs. The voltage output of the regulator can be used as a termination voltage for other bus interface standards such as SSTL, CMOS, Rambus™, GTL+, VME, LV-CMOS, LV-TTL, and PECL.

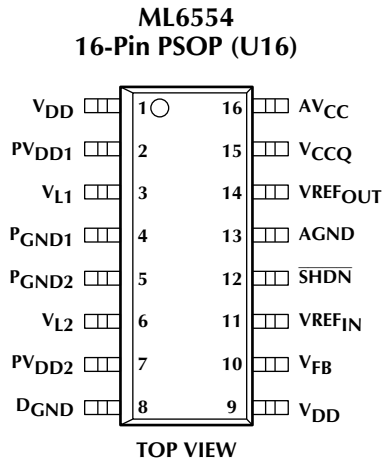
FEATURES

- Power SOP package
- Can source and sink up to 3A, no heat sink required
- Integrated Power MOSFETs
- Generates termination voltages for SSTL-2 SDRAM, SGRAM, or equivalent memories
- Generates termination voltages for active termination schemes for GTL+, Rambus, VME, LV-TTL, PECL and other high speed logic
- V_{REF} input available for external voltage divider
- Separate voltages for V_{CCQ} and PV_{DD}
- Buffered V_{REF} output
- V_{OUT} of $\pm 3\%$ or less at 3A
- Minimum external components
- Shutdown for standby or suspend mode operation
- Thermal Shutdown $\approx 130^\circ\text{C}$

BLOCK DIAGRAM



PIN CONFIGURATION



PIN DESCRIPTION

PIN	NAME	FUNCTION	PIN	NAME	FUNCTION
1	V _{DD}	Digital supply voltage	9	V _{DD}	Digital supply voltage
2	PV _{DD1}	Voltage supply for internal power transistors	10	V _{FB}	Input for external compensation feedback
3	V _{L1}	Output voltage/ inductor connection	11	V _{REFIN}	Input for external reference voltage
4	P _{GND1}	Ground for output power transistors	12	$\overline{\text{SHDN}}$	Shutdown active low. CMOS input level
5	P _{GND2}	Ground for output power transistors	13	AGND	Ground for internal reference voltage divider
6	V _{L2}	Output voltage/inductor connection	14	V _{REFOUT}	Reference voltage output
7	PV _{DD2}	Voltage supply for internal power transistors	15	V _{CCQ}	Voltage reference for internal voltage divider
8	D _{GND}	Digital ground	16	AV _{CC}	Analog voltage supply

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

PV_{DD}	5.0V
Voltage on Any Other Pin	GND – 0.3V to $V_{IN} + 0.3V$
Average Switch Current (I_{AVG})	3.0A
Junction Temperature	
Storage Temperature Range	

Lead Temperature (Soldering, 10 sec)	
Thermal Resistance (θ_{JC})(Note 3)	2°C/W
Output Current, Source or Sink	3.0A

OPERATING CONDITIONS

Temperature Range	0°C to 70°C
PV_{DD} Operating Range	2.0V to 4.0V

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, $PV_{DD} = 3.3V \pm 10\%$, T_A = Operating Temperature Range (Note 1)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	
SWITCHING REGULATOR							
V_{TT}	Output Voltage, SSTL_2 (See Figure 1)	$I_{OUT} = 0$, $V_{REF} = \text{open}$ Note 2	$V_{CCQ} = 2.3V$	1.12	1.15	1.18	V
			$V_{CCQ} = 2.5V$	1.22	1.25	1.28	V
			$V_{CCQ} = 2.7V$	1.32	1.35	1.38	V
		$I_{OUT} = \pm 3A$, $V_{REF} = \text{open}$ Note 2	$V_{CCQ} = 2.3V$	1.09	1.15	1.21	V
			$V_{CCQ} = 2.5V$	1.19	1.25	1.31	V
			$V_{CCQ} = 2.7V$	1.28	1.35	1.42	V
$V_{REF_{OUT}}$	Internal Resistor Divider	$I_{OUT} = 0$ Note 2	$V_{CCQ} = 2.3V$	1.139	1.15	1.162	V
			$V_{CCQ} = 2.5V$	1.238	1.25	1.263	V
			$V_{CCQ} = 2.7V$	1.337	1.35	1.364	V
Z_{IN}	V_{REF} Reference Pin Input Impedance	Note 2	$V_{CCQ} = 0$		100	k Ω	
	Switching Frequency				650	kHz	
ΔV_{OFFSET}	Offset Voltage $V_{TT} - V_{REF_{OUT}}$	$V_{CCA} = 2.5V$ No Load	$V_{CCQ} = 2.5$	-12.5		12.5	mV

SUPPLY

I_Q	Quiescent Current	$I_{OUT} = 0$, no load	I_{VCCQ}		10		μA
			I_{AVCC}		500		μA
			I_{DVCC}		7		mA

BUFFER

I_{REF}	Output Load Current		3			mA
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Note 1: Limits are guaranteed by 100% testing, sampling, or correlation with worst-case test conditions.

Note 2: AV_{CC} , $PV_{DD} = 3.3V \pm 10\%$

Note 3: Infinite heat sink

FUNCTIONAL DESCRIPTION

This switching regulator is capable of sinking and sourcing 3A of current without an external heatsink. The ML6554 uses a power surface mount package (PSOP) that includes an integrated heat slug. The heat can be piped through the bottom of the device and onto the PCB (Figure 2).

The ML6554 integrates two power MOSFETs that can be used to source and sink 3A of current while maintaining a tight voltage regulation. Using the external feedback, the output can be regulated well within 3% or less, depending on the external components chosen. Separate voltage supply inputs have been added to accommodate applications with various power supplies for the databus and power buses.

OUTPUTS

The output voltage pins (V_{L1} , V_{L2}) are tied to the databus, address, or clock lines via an external inductor. See the Applications section for recommendations. Output voltage is determined by the V_{CCQ} or V_{REFIN} inputs.

INPUTS

The input voltage pins (V_{CCQ} or V_{REFIN}) determine the output voltages (V_{L1} or V_{L2}). In the default mode, where the V_{REFIN} pin is floating, the output voltage is 50% of the V_{CCQ} input. V_{CCQ} can be the reference voltage for the databus.

Output voltage can also be selected by forcing a voltage at the V_{REFIN} pin. In this case, the output voltage follows the voltage at the V_{REFIN} input. Simple voltage dividers can be used in this case to produce a wide variety of output voltages between 2.3V to 4V.

VREF INPUT AND OUTPUT

The V_{REFIN} input can be used to force a voltage at the outputs (Inputs section, above). The V_{REFOUT} pin is an output pin that is driven by a small output buffer to provide the V_{REF} signal to other devices in the system. The output buffer is capable of driving several output loads. The output buffer can handle 3mA.

OTHER SUPPLY VOLTAGES

Several inputs are provided for the supply voltages: PV_{DD1} , PV_{DD2} , AV_{CC} , and V_{DD} .

The PV_{DD1} and PV_{DD2} provide the power supply to the power MOSFETs. V_{DD} provides the voltage supply to the digital sections, while AV_{CC} supplies the voltage for the analog sections. Again, see the Applications section for recommendations.

FEEDBACK INPUT

The V_{FB} pin is an input that can be used for closed loop compensation. This input is derived from the voltage output. See application section for recommendation.

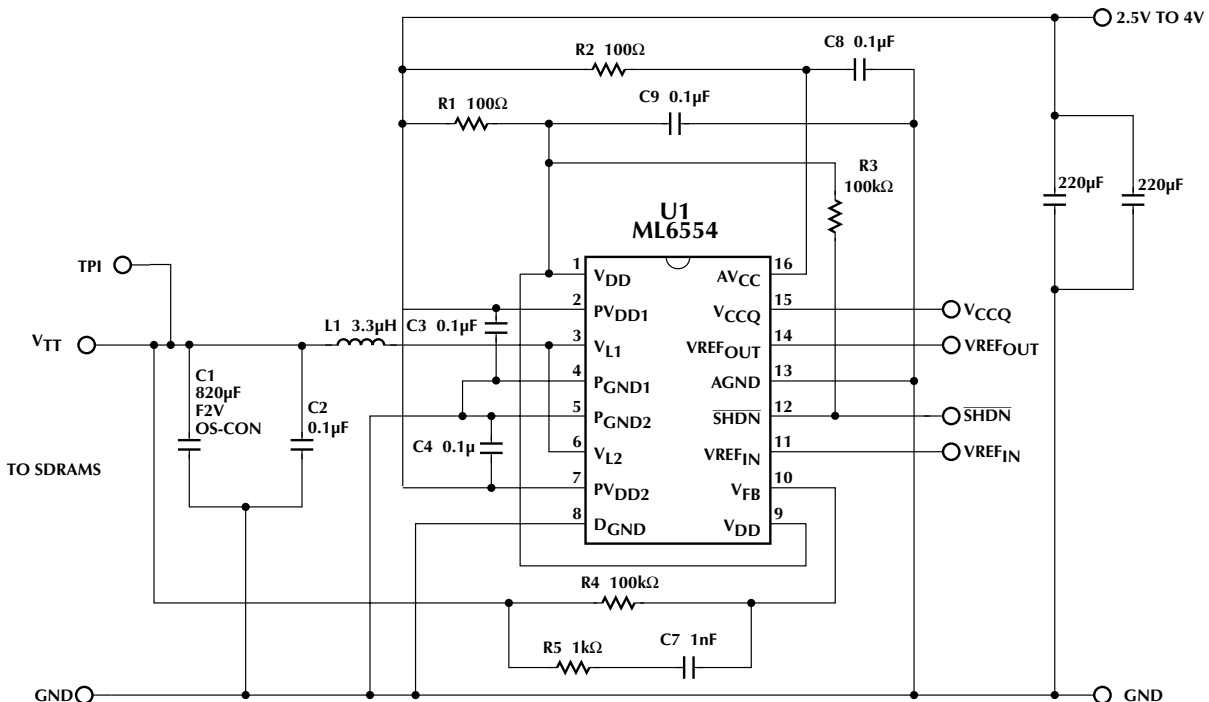


Figure 1.

APPLICATIONS

USING THE ML6554 FOR SSTL BUS TERMINATION

The circuit schematic in Figure 1 shows a recommended approach for constructing a bus terminating solution for an SSTL-2 bus. This circuit can be used in PC memory and Graphics memory applications as shown in Figures 3 and 4. Note that the ML6554 can provide the voltage reference (V_{REF}) and terminating voltages (V_{TT}). Using the layout as shown in Figures 5, 6, and 7, and measuring the V_{TT} performance using the test setup as described in Figure 8, the ML6554 delivered a $V_{TT} \pm 20\text{mV}$ for 1A to 3A loads (see Figure 9). Table 1 provides a recommended parts list. For more recent Applications Notes or Evaluation Boards contact Micro Linear.

POWER HANDLING CAPABILITY OF THE PSOP PACKAGE

Using the board layout shown in Figures 5, 6, and 7; soldering the ML6554 to the board at zero LFPM the temperature around the package measured 55°C for 3A loads. Note that a 1ounce copper plane was used in the board construction.

Airflow is not likely to be needed in the operation of this device (assuming a board layout similar to that described above). The power handling performance of the PSOP package is shown by a study of the package manufacturer for various airflow vs. θ_{JA} conditions in Figure 10.

BUS TERMINATION SOLUTIONS FOR OTHER BUSES

Table 2 provides a summary of various bus termination V_{REF} & V_{TT} requirements. The ML6554 can be used for those applications.

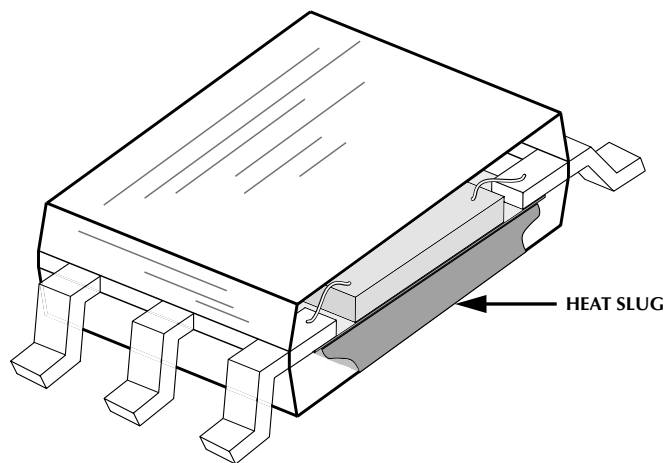


Figure 2. Cutaway view of PSOP Package

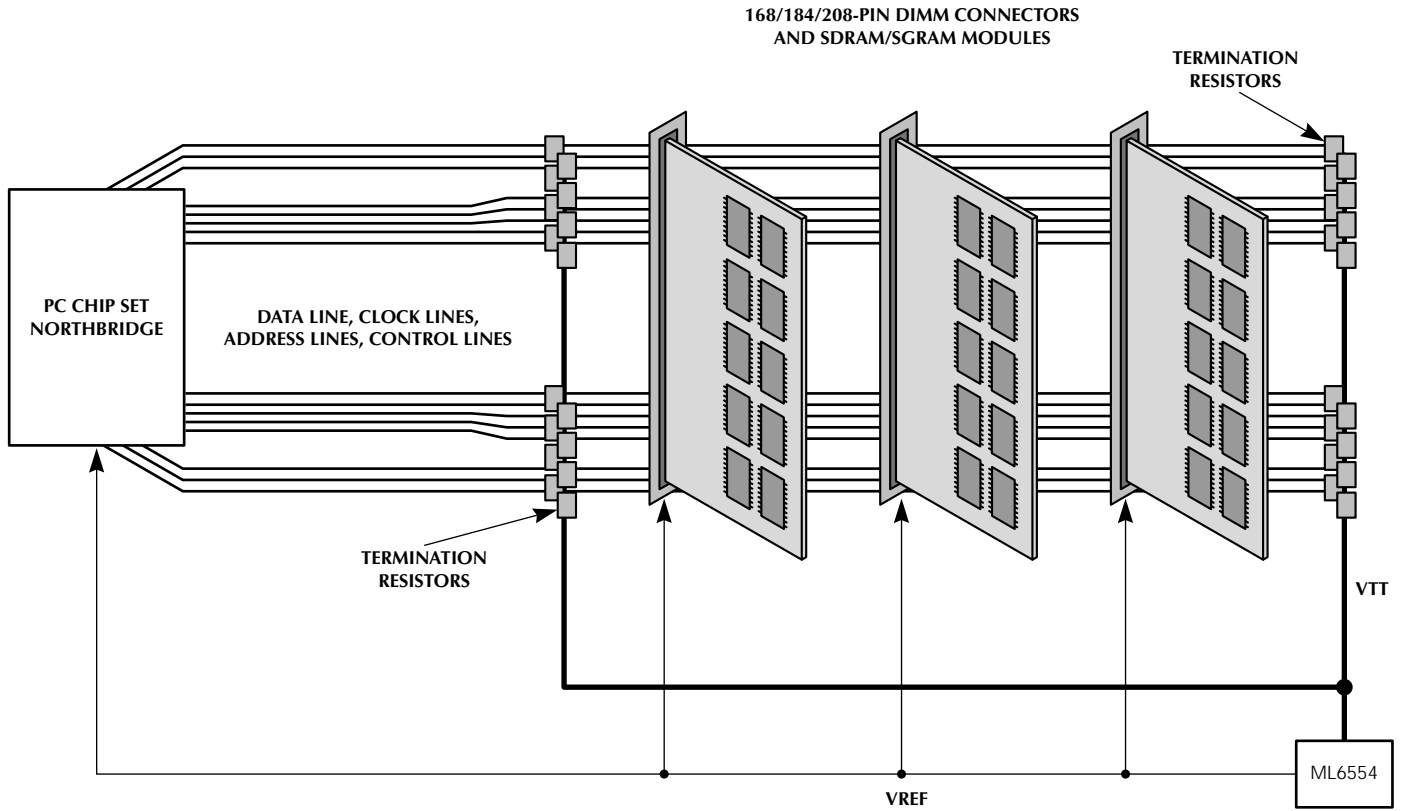


Figure 3. Complete Termination Solution PC Main Memory (PC Motherboard)

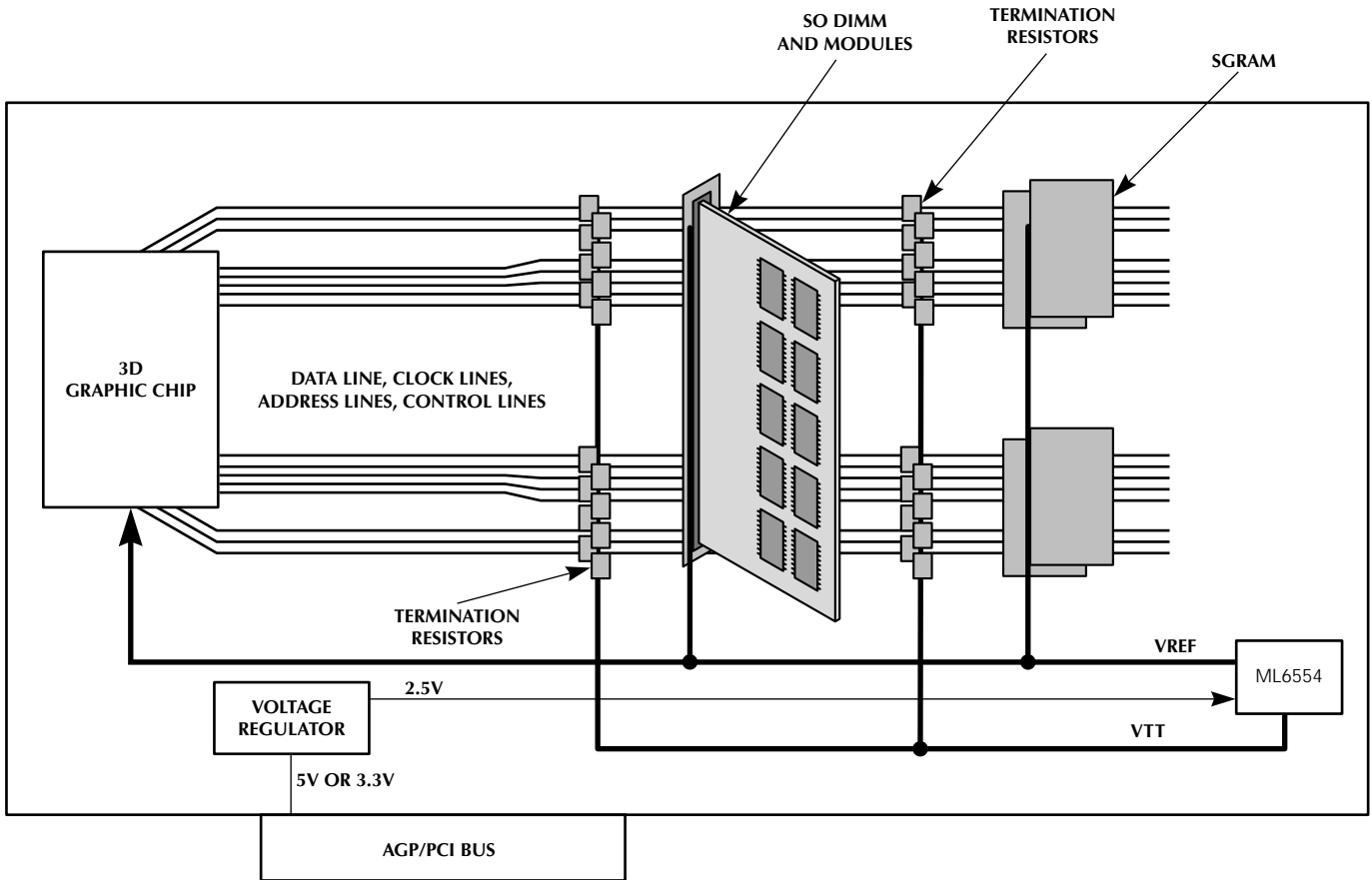


Figure 4. Complete Termination Solution Graphics Memory Bus – AGP Graphics Cards

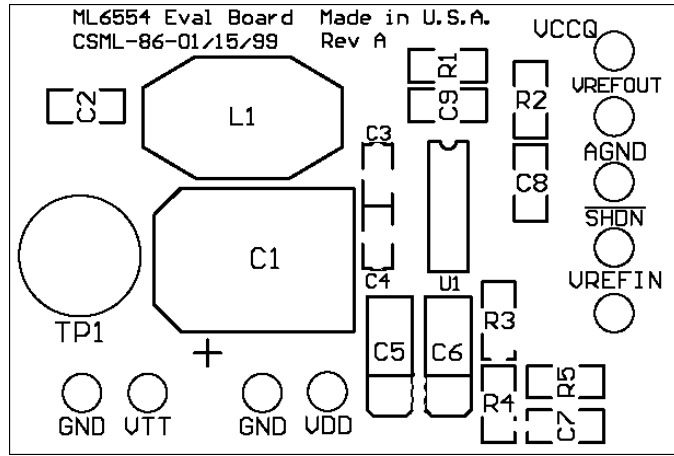


Figure 5. Top Silk

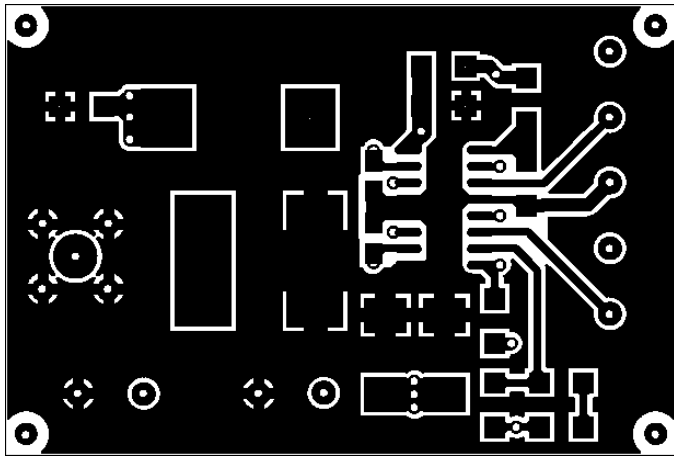


Figure 6. Top Layer

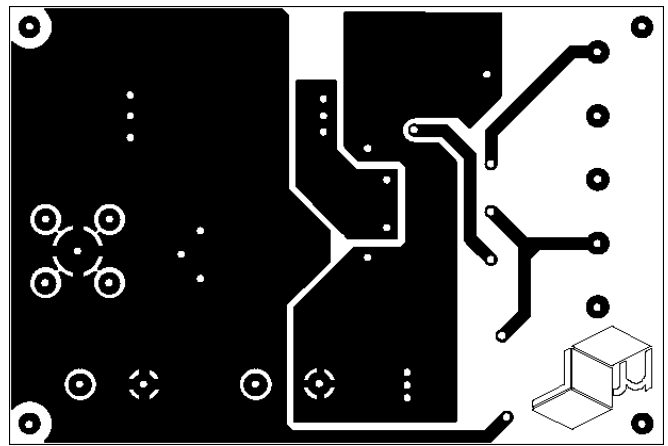


Figure 7. Bottom Layer

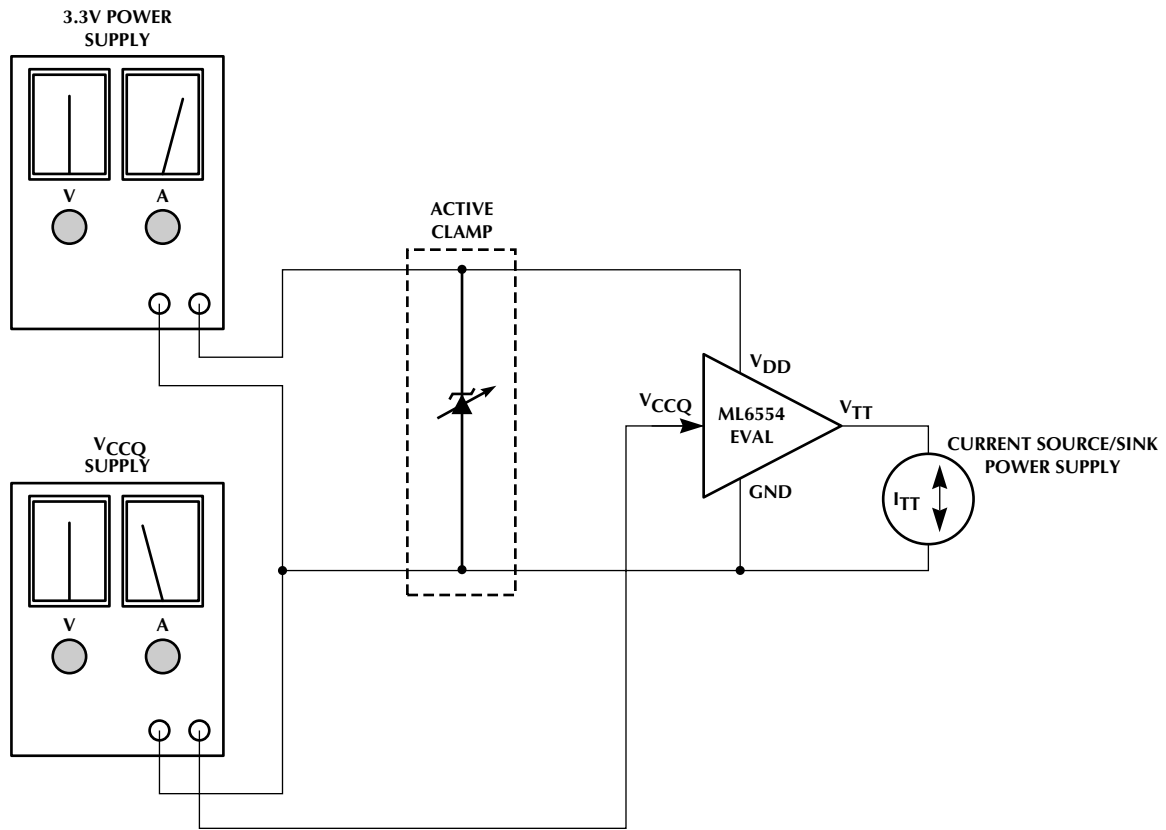


Figure 8. Test Circuit Setup

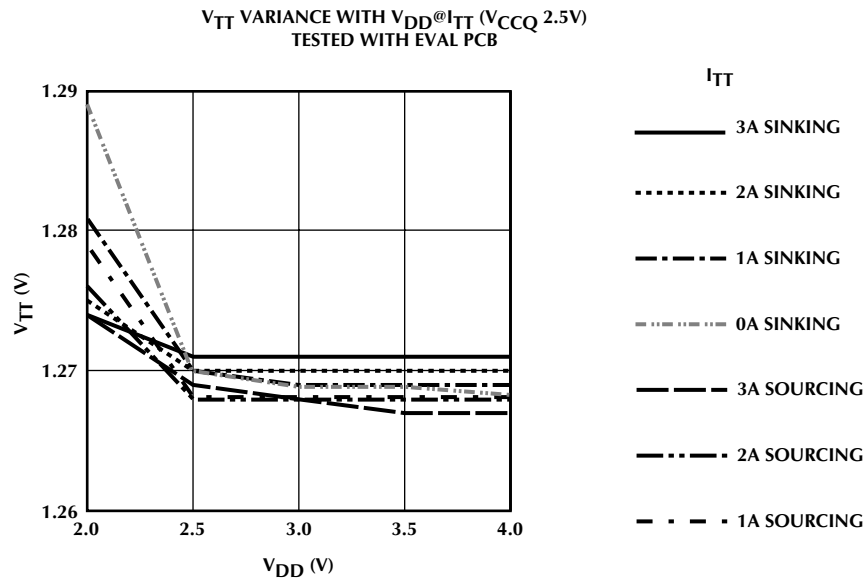


Figure 9. VTT Performance for SSTL-2 Bus

ITEM	QTY	DESCRIPTION	MANUFACTURER / PART NUMBER	DESIGNATOR
RESISTORS				
1	2	100Ω1210 SMD	Panasonic/ERJ-8ENF1000V	R1, R2
2	1	1kΩ 1210 SMD	Panasonic/ERJ-8ENF1001V	R5
3	2	100kΩ1210 SMD	Panasonic/ERJ-8ENF1003V	R3, R4
CAPACITORS				
4	3	0.1μF 1210 Film SMD	Panasonic/ECV3VB1E104K Panasonic/ECU-V1H104KBW	C2, C8, C9
5	1	820μF 2V Solid Elect. SMD	Sanyo/ 2SV820M Os Con	C1
6	2	330μF Tant 6.3V 100mΩ	AVX/ TPSE337M006R0100	C5, C6
7	1	1nF 1210 Film SMD	Panasonic/ECU-V1H102KBM	C7
8	2	0.1μF 0805 Film	Panasonic/ECJ-2VF1C104Z	C3, C4
ICS				
9	1	ML6554 Bus Terminator Power SOP Package	ML6554CU	U1
MAGNETICS				
10	1	3.3μH 5A inductor SMD	Coilcraft/D03316P-332HC Pulse Eng./ P0751.332T Gowanda/SMP3316-331M XFMRS inc./XF0046-S4	L1
OTHER				
11	1	Scope probe socket	Tektronics/131-4353-00	TP1
12	1	12 Pin breakaway strip	Sullins/PTC36SAAN (36 PINS)	I/O, standoffs

Table 1. Recommend Parts List for SSTL-2 Termination Circuit

VENDOR LIST

1. AVX (207) 282-5111
2. Sanyo (619) 661-6835
3. Tektronix (408) 496-0800
4. Coilcraft (847) 639-6400
5. Pulse (800) 797-8573
6. Gowanda (716) 532-2234
7. Xfmrs Inc. (317) 834-1066
8. Panasonic (714) 373-7366
9. Digikey (800) 344-4539

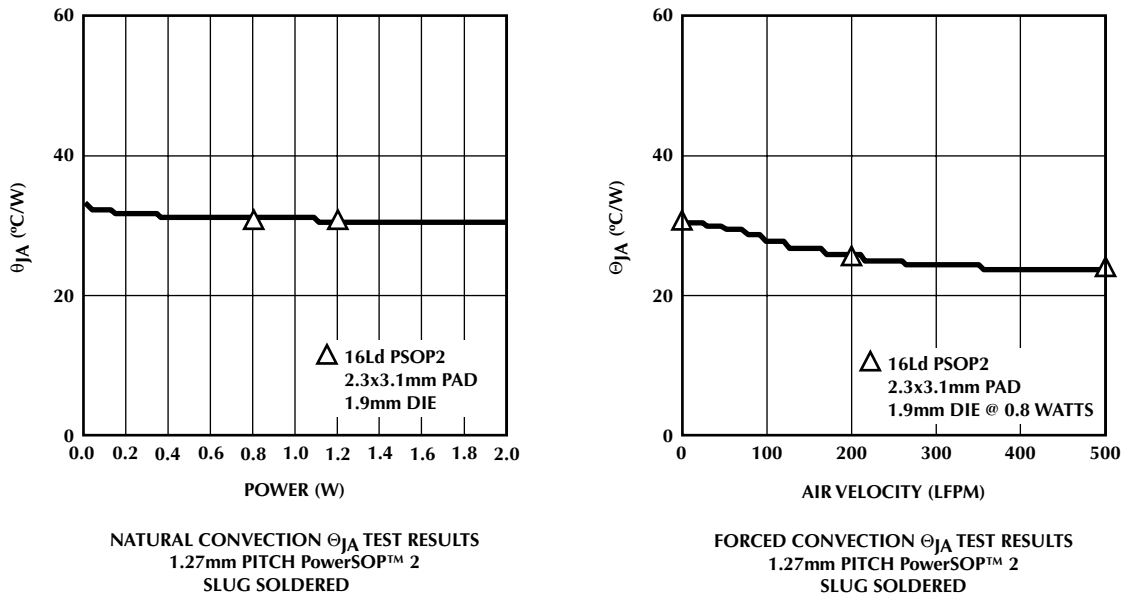
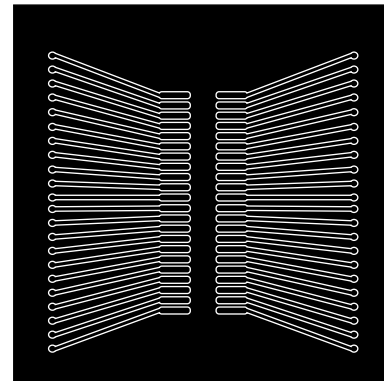


Figure 10. Graphical Results Summary – 1S2P Test Board

DRAWING NUMBER	ENG-CB-1007 REV A
Applicable Jedec Spec	JC 51-X (Note 1) (Sroposed Spec)
Substrate Material	FR-4
Dimensions (LxW) (Overall)	114.3 x 76.2mm
Dimensions (LxW) (Metallization)	55 x 65mm
Dimensions (LxW) (Inner Planes)	73 x 73mm
Thickness	1.6 mm
Pitch	1.27mm
Stackup (# Signal Layers, # Cu Planes)	1S2P
Cu Trace Coverage (Signal Layer)	12%
Cu Coverage (Internal Layer)	100%
Trace Width (Spec/Measured)	235.5±25.5/288µm
Trace Cu Thickness (Spec/Measured)	70±14/67µm
Inner Cu Thickness (Spec/Measured)	35±3.5/31µm
Build #	C1797



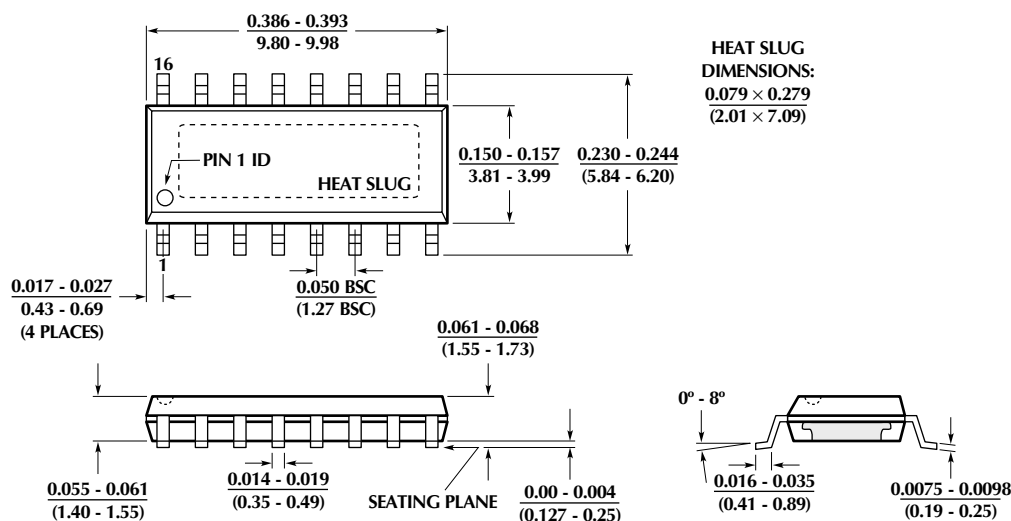
Note 1: Proposed Spec "Thermal Test Board with Two Internal Solid Copper Planes for leaded Surface Mount Packages".

Figure 11. Test Board Layout for θ_{JA} vs. Airflow

BUS	DESCRIPTION	DRIVING METHOD	VDDQ	VTT	VREF	MICRO LINEAR SOLUTIONS	INDUSTRY SYSTEM COMPONENTS
GTL+	Gunning Transceiver Bus Plus	Open Drain	5v or 3.3V Note 10	1.5V±10% Note12	1.0V±2% Note 11	ML6554CU; Mode: V _{REF} Input = 1.5V, V _{CC} = 5V	300 to 500MHz Processor; PC Chipsets; GTL _P 16xxx Buffers; Fairchild, Texas Instr.
SSTL_2	Series Stub Terminated Logic for 2V	Symmetric Drive, Series Resistance	2.5V±10%	0.5x(V _{DDQ}) ±3%	2.5V	ML6554CU or ML6553CS; Mode: V _{REF} Input = Floating or Forced, V _{CC} = 3.3V	SSTL SDRAM; Hitachi, Fujitsu, NEC, Micro, Mitsubishi
RAMBUS	RAMBUS Signaling Logic	Open Drain	None Specified	2.5V	2.0V	ML6553CS; Mode: V _{REF} Input = Open, V _{CC} = V _{DDQ}	nDRAM, RAMBUS, Intel, Toshiba
LV-TTL	Low Voltage TTL Logic or PECL or 3.3V VME	Symmetric Drive	3.3±10%	V _{DDQ} /2	3.3V	ML6553CS; Mode: V _{REF} Input = Open, V _{CC} = V _{DDQ}	Processors or backplanes; LV-TTL SDRAM, EDO RAM

Table 2. Termination Solutions Summary By Buss Type


PHYSICAL DIMENSIONS inches (millimeters)

**Package: U16
16-Pin PSOP**

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML6554CU	0°C to 70°C	16-Pin PSOP (U16)

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