SONY

CXA2153S

Preamplifier for High Resolution Computer Display

Description

The CXA2153S is a bipolar IC developed for high resolution computer displays.

Features

- Built-in wide-band amplifier: 180MHz@–3dB (Typ.)
- Input dynamic range: 1.0Vp-p (Typ.)
- High gain preamplifier (15dB)
- R, G and B incorporated in a single package (SDIP 30 pins)
- I^2C bus control
  - Contrast control
  - R/G/B drive control
  - Brightness control
  - OSD contrast control
  - 4-channel DAC control output
- Built-in gamma function
- Built-in high-speed ABL blanking
- Built-in sync separator for Sync on Green
- Built-in blanking mixing function (with blanking level fixed at 0.4V)
- Built-in OSD mixing function
- Video period detection function
- Built-in VBLK synchronous DAC refresh system

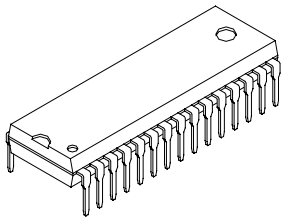
Applications

High resolution computer displays

Structure

Bipolar silicon monolithic IC

30 pin SDIP (Plastic)



Absolute Maximum Ratings (Ta = 25°C, GND = 0V)

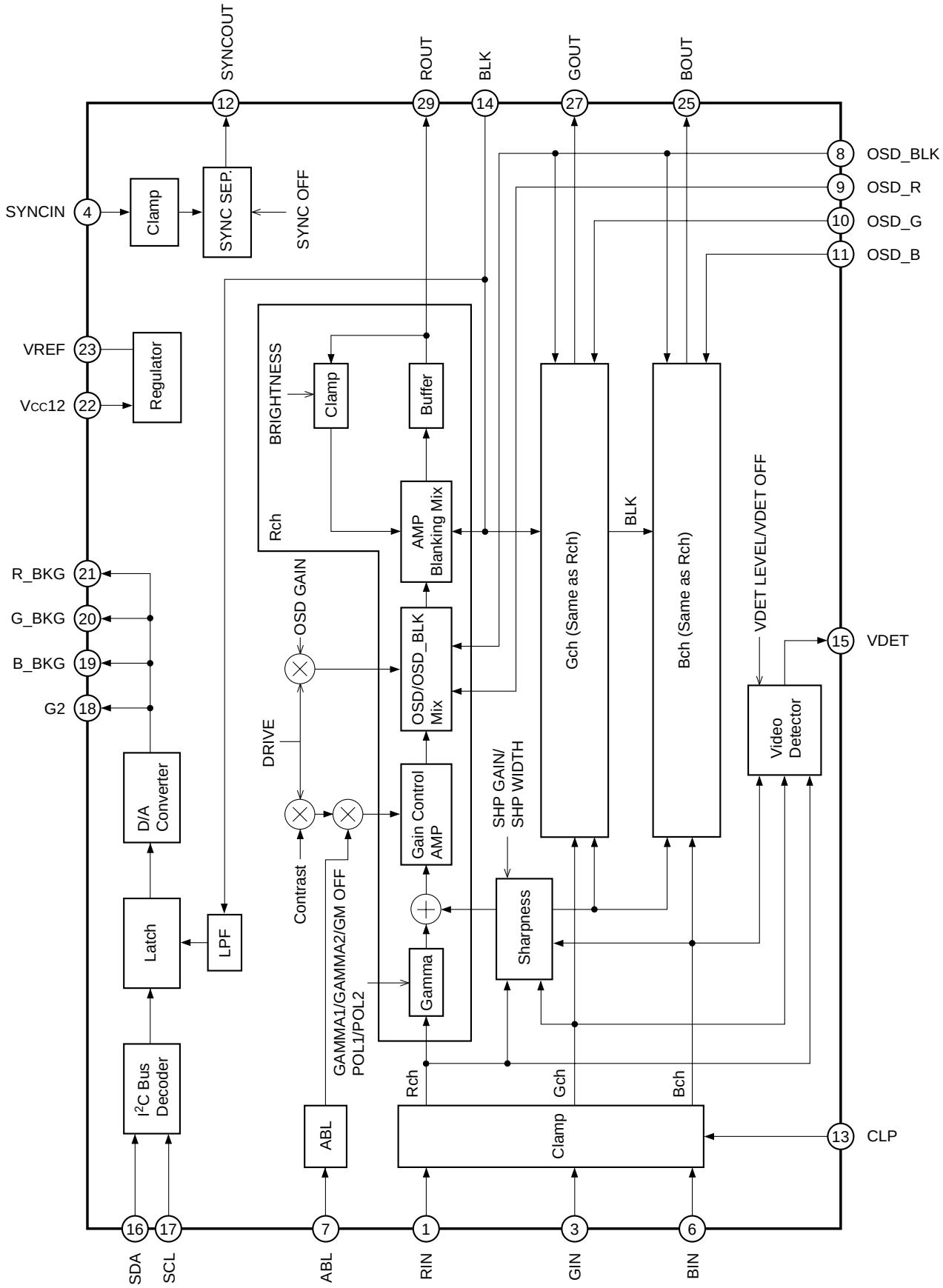
• Supply voltage	Vcc12	13	V
	Vcc5	5.5	V
• Operating temperature	Topr	–20 to +75	°C
• Storage temperature	Tstg	–65 to +150	°C
• Allowable power dissipation	P_D	2.05	W
• Pin voltage	Vcc5 + 0.3V	1, 3, 4, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17 (Pin)	
	VREF (Pin 23) + 0.3V	18, 19, 20, 21, 25, 27, 29 (Pin)	

Recommended Operating Conditions

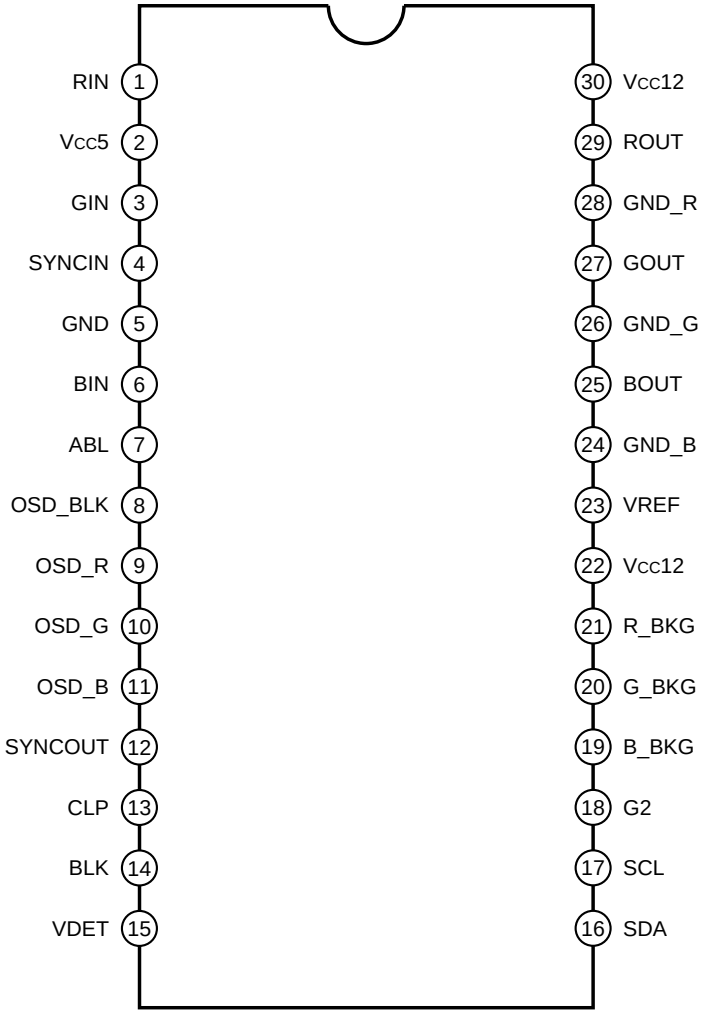
Supply voltage	Vcc12	12 ± 0.5	V
	Vcc5	5 ± 0.25	V

E99X02A1Y-PS

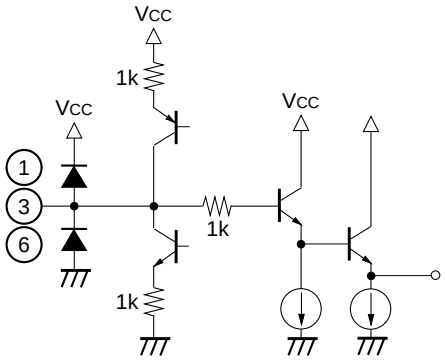
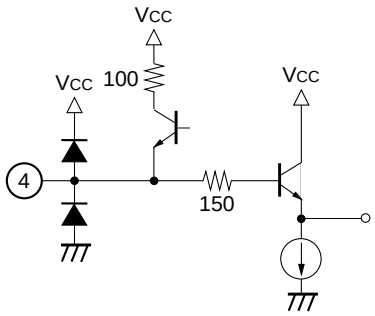
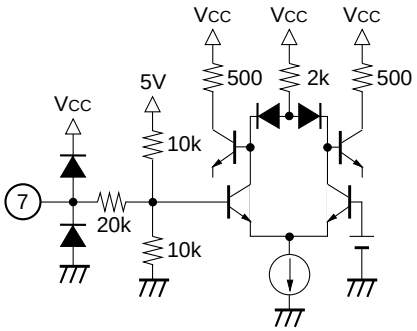
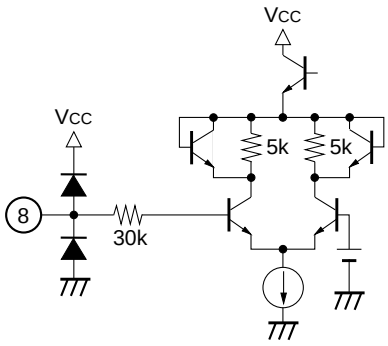
Block Diagram

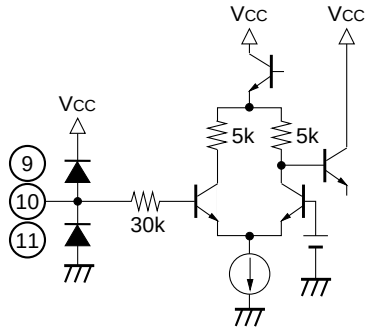
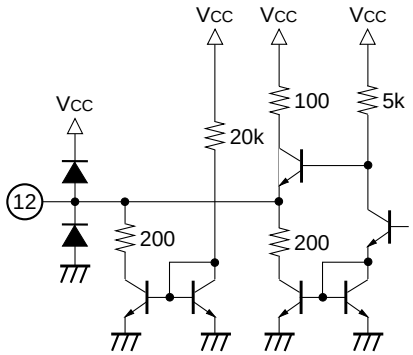
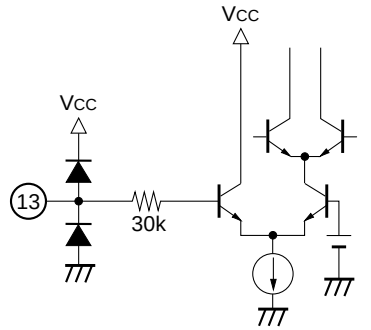
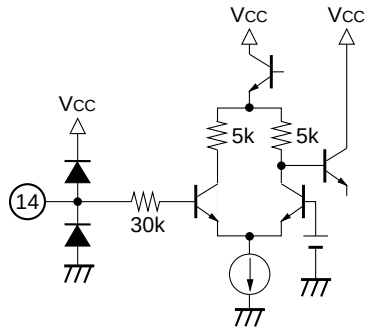


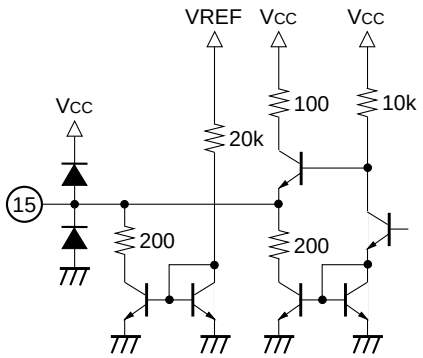
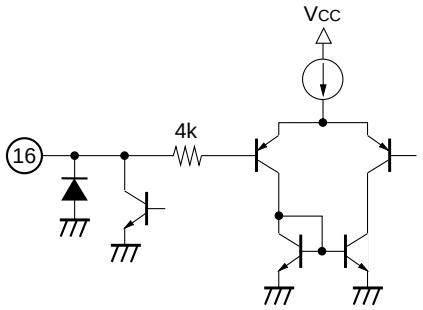
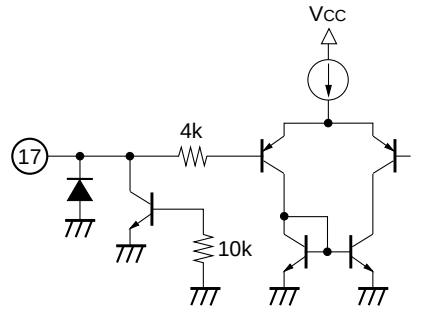
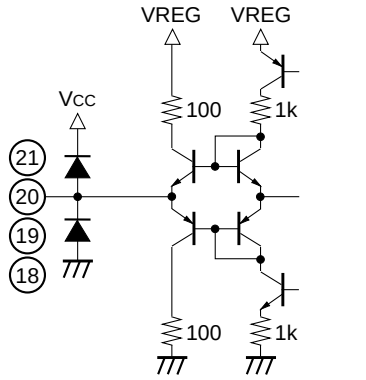
Pin Configuration

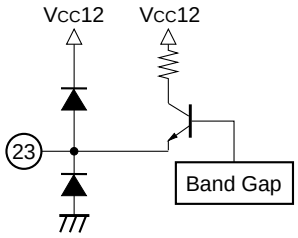
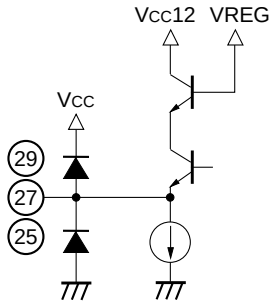


Pin Description

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
1 3 6	RIN GIN BIN	3.1V (CLAMP)		RGB signal inputs. Input via the capacitor.
2	Vcc5	5V		5V power supply.
4	SYNCIN	2.9V		Sync-on-green signal input. Input via the capacitor.
5	GND			GND
7	ABL	2.5V (when open)		ABL input.
8	OSD_BLK			OSD_BLK control input. VILMAX = 0.8V VIHMIN = 2.8V

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
9 10 11	OSD_R OSD_G OSD_B			OSD control input. VILMAX = 0.8V VIHMIN = 2.8V
12	SYNCOUT			Sync separator output of Sync-on-green signal. I²C bus SOG off: Output at 0. Typ.: High = 4.2V Low = 0.2V (positive polarity)
13	CLP			Clamp pulse (positive polarity) input. VILMAX = 0.8V VIHMIN = 2.8V
14	BLK			Blanking pulse input. Set the V blanking pulse width to 300µs or more. VILMAX = 1.2V VIHMIN = 4.7V

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
15	VDET			Video detector output. I²C bus VDET off: Output at 0.
16	SDA			I²C bus standard SDA (serial data) input/output. VILMAX = 1.5V VIHMIN = 3.5V VOLMAX = 0.4V
17	SCL			I²C bus standard SCL (serial clock) input. VILMAX = 1.5V VIHMIN = 3.5V
21 20 19 18	R_BKG G_BKG B_BKG G2			BKG/G2 adjustment DAC outputs. The output DC is 1.5 to 5.5V.
22 30	Vcc12	12V		12V power supply

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
23	VREF	9V		9V regulator. Connect with Vcc12 via a resistor of around 220Ω. It cannot be used as an external power supply.
28 26 24	GND_R GND_G GND_B	0V		GNDs
29 27 25	ROUT GOUT BOUT			R, G and B signal outputs.

I²C BUS Register Definitions

Slave Address

SLAVE RECEIVER: 40 (HEX)

Register Table

Sub Address	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
00h	CONTRAST							
01h	BRIGHTNESS							
02h	R_BKG							
03h	G_BKG							
04h	B_BKG							
05h	OSD GAIN							
06h	G2							
07h	R_DRV							
08h	G_DRV							
09h	B_DRV							
0Ah	*	*	SHP WIDTH		SHP GAIN			
0Bh	POL1	GAMMA1		POL2	GAMMA2			
0Ch	*	*	VDET LVL	VDET OFF	SOG OFF	GAM OFF	0	D R OFF

*: Don't Care

Sub Address 0000 CONTRAST (8) Controls the gain common to the R, G and B channels. Since control is performed by multiplying with R/G/B DRIVE, the white balance can be adjusted by R/G/B DRIVE and the luminance can be adjusted by CONTRAST.

0: Output level minimum (0Vp-p)
255: Output level maximum (4.4Vp-p; with 0.7Vp-p input)

Sub Address 0001 BRIGHTNESS (8) Controls the black level common to the R, G and B channels.

0: Black level minimum (0.8V)
255: Black level maximum (2.9V)

Sub Address 0010 R_BKG (8) Controls Pin 21 (R BACKGROUND) output voltage.

0: Output voltage minimum (1.5V)
255: Output voltage maximum (5.5V)

Sub Address 0011 G_BKG (8) Controls Pin 20 (G BACKGROUND) output voltage.

0: Output voltage minimum (1.5V)
255: Output voltage maximum (5.5V)

Sub Address 0100 B_BKG (8) Controls Pin 19 (B BACKGROUND) output voltage.

0: Output voltage minimum (1.5V)
255: Output voltage maximum (5.5V)

Sub Address 0101 OSD GAIN (8)
Controls the OSD gain common to the R, G and B channels. Since control is performed by multiplying with R/G/B DRIVE, the video white balance and tracking are obtained.
0: Gain minimum (0Vp-p)
255: Gain maximum (4.5Vp-p)

Sub Address 0110 G2 (8)
Controls Pin 18 (G2) output voltage.
0: Output voltage minimum (1.5V)
255: Output voltage maximum (5.5V)

Sub Address 0111 R_DRV (8)
Controls the gain for the R channel. Control is performed by multiplying with CONTRAST. Use this for adjusting the white balance.
0: Output level minimum (0Vp-p)
255: Output level maximum (4.4Vp-p; with 0.7Vp-p input)

Sub Address 1000 G_DRV (8)
Controls the gain for the G channel. Control is performed by multiplying with CONTRAST. Use this for adjusting the white balance.
0: Output level minimum (0Vp-p)
255: Output level maximum (4.4Vp-p; with 0.7Vp-p input)

Sub Address 1001 B_DRV (8)
Controls the gain for the B channel. Control is performed by multiplying with CONTRAST. Use this for adjusting the white balance.
0: Output level minimum (0Vp-p)
255: Output level maximum (4.4Vp-p; with 0.7Vp-p input)

Sub Address 1010 SHP WIDTH (2)
Controls the sharpness time constant switching.
0: OFF
1: 25ns
2: 50ns
3: 100ns

Sub Address 1010 SHP GAIN (4)
Controls the sharpness gain.
0: Gain minimum (0dB)
F: Gain maximum (6dB) * Amplitude at SHP OFF is assumed to be 0dB.

Sub Address 1011 POL1 (1)
Controls the polarity of the correction at GAMMA1.
0: – correction
1: + correction

Sub Address 1011 GAMMA1 (2)
Controls the gain of the inflection point 1 (15 IRE) at GAMMA.
0: 0 IRE correction
3: 9 IRE correction

Sub Address 1011 POL2 (1)
Controls the polarity of the correction at GAMMA2.
0: – correction
1: + correction

Sub Address 1011 GAMMA2 (4)

Controls the gain of the inflection point 2 (60 IRE) at GAMMA.
- 0: 0 IRE correction
- 7: 20 IRE correction

Sub Address 1100 VDET LVL (1)

Controls the signal detection (VDET) slice level.
- 0: Slice level (160mV when RIN or GIN or BIN)
- 1: Slice level (200mV when RIN or GIN or BIN)

Sub Address 1100 VDET OFF (1)

Controls the video detection output.
- 0: Output on
- 1: Output off

Sub Address 1100 SOG OFF (1)

Controls the sync separator output.
- 0: Output on
- 1: Output off

Sub Address 1100 GM OFF (1)

Controls the gamma function operation.
- 0: Gamma on
- 1: Gamma off

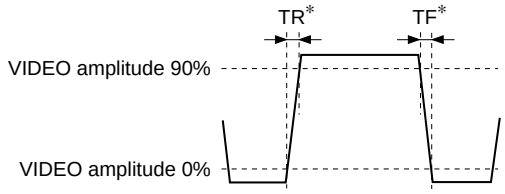
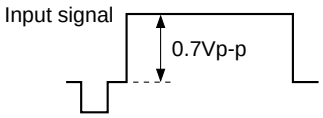
Sub Address 1100 D R OFF (1)

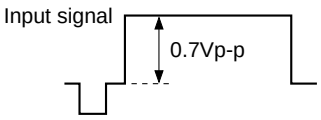
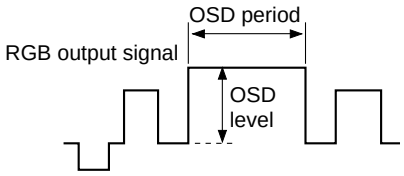
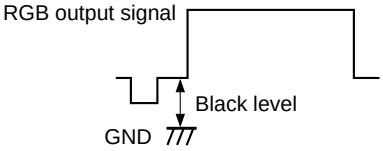
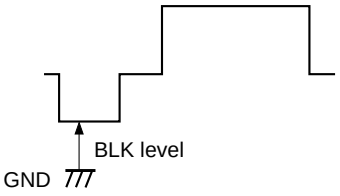
Controls the VBLK synchronous DAC refresh function. The operation of this function is set to OFF when the power is turned on.
- 0: Function operation on
- 1: Function operation off

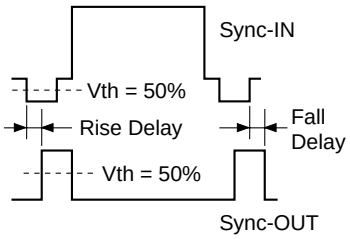
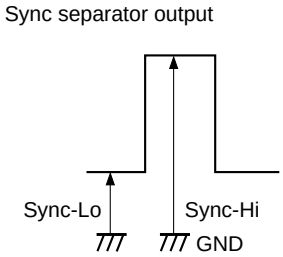
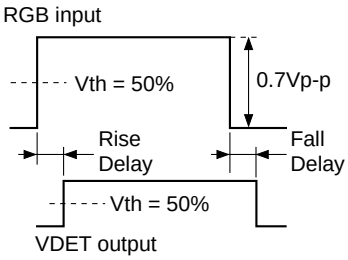
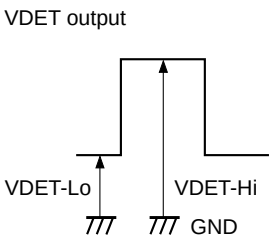
I²C BUS Logic System

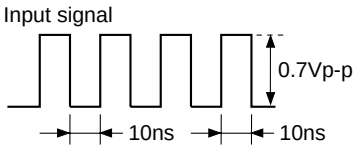
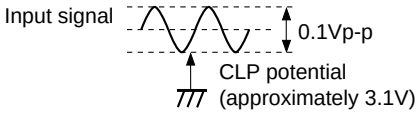
No.	Item	Symbol	Min.	Typ.	Max.	Unit
1	High level input voltage	V_{IH}	3.0	—	5.0	V
2	Low level input voltage	V_{IL}	0	—	1.5	V
3	Low level output voltage SDA during current inflow of 3mA	V_{OL}	0	—	0.4	V
4	Maximum clock frequency	f_{SCL}	0	—	400	kHz
5	Minimum waiting time for data change	t_{BUF}	1.3	—	—	µs
6	Minimum waiting time for data transfer start	t_{HD}; STA	0.6	—	—	µs
7	Low level clock pulse width	t_{LOW}	1.3	—	—	µs
8	High level clock pulse width	t_{HIGH}	0.6	—	—	µs
9	Minimum waiting time for start preparation	t_{SU}; STA	0.6	—	—	µs
10	Minimum data hold time	t_{HD}; DAT	0	—	900	ns
11	Maximum data preparation time	t_{SU}; DAT	100	—	—	ns
12	Rise time	t_R	—	—	1	µs
13	Fall time	t_F	—	—	300	ns
14	Minimum waiting time for stop preparation	t_{SU}; STO	0.6	—	—	µs

Electrical Characteristics

No.	Measurement item	Symbol	Measurement contents	Min.	Typ.	Max.	Unit
1	Current consumption (5V)	Icc1	Vcc5 (5V) pin inflow current RGB signal input: None	38	55	73	mA
2	Current consumption (12V)	Icc2	Vcc12 (12V) pin inflow current RGB signal input: None	28	42	57	mA
3	Current consumption (12V OFF)	Icc3	Pin inflow current when 12V OFF RGB signal input: None	3.4	4.9	6.6	mA
4	Pulse characteristics	TR	Measure input rise time (TR1), input fall time (TF1), input rise time (TR2) and input fall time (TF2), then substitute these values into the following equations. $TR = \sqrt{(TR2^2 - TR1^2)}$, $TF = \sqrt{(TF2^2 - TF1^2)}$ (Contrast = 7F, DRIVE = FF, BRIGHTNESS = 7F)	0.9	1.96	3	ns
		TF		1.6	3.1	4.6	
5	Contrast control 1	GCONT1	Measure the level of the output signal amplitude Vout when a 0.7Vp-p video signal is input. GCONT1: Contrast = DRIVE = FF GCONT2: Contrast = 00/DRIVE = FF	4	4.4	4.8	Vp-p
6	Contrast control 2	GCONT2		–100	0	120	mVp-p
7	Relative contrast	GCONGAP	Calculate the difference in the data obtained in No.5 and No.6 between the channels.	–180	0	180	mV

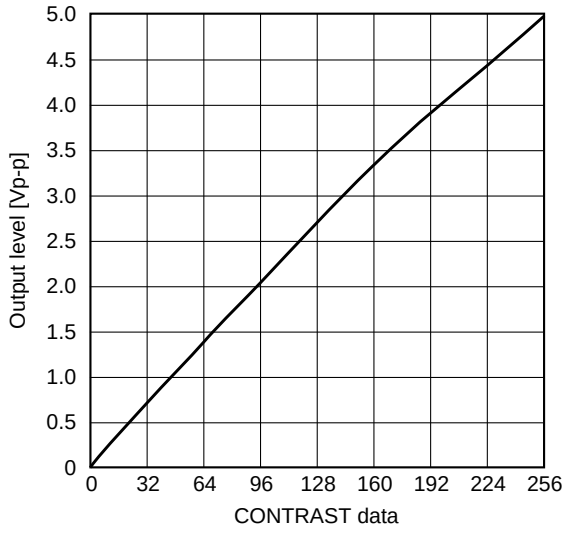
No.	Measurement item	Symbol	Measurement contents	Min.	Typ.	Max.	Unit
8	Drive control	GDRV	Measure the level of the output signal amplitude Vout when a 0.7Vp-p video signal is input. Contrast = FF/DRIVE = 00 	–100	0	120	mVp-p
9	OSD gain control	GOSD1	Measure the OSD level of the output signal when the OSD pulse is input. GOSD1: OSD = FF/DRIVE = FF GOSD2: OSD = 00/DRIVE = FF 	4	4.57	5.15	Vp-p
		GOSD2		–330	0	360	mVp-p
10	Relative OSD	OSDGAP	Calculate the difference in the data obtained in No.9 between the channels.	–200	0	200	mV
11	Brightness control	VBRT1	Measure the black level of the RGB output signal. VBRT1: Brightness = 00 VBRT2: Brightness = FF 	0.6	0.8	0.95	V
		VBRT2		2.5	2.93	3.28	
12	Relative brightness	VBRTGAP	Calculate the difference in the data obtained in No.11 between the channels.	–200	0	200	mV
13	BLK level	VBLK	Measure the BLK level of the output signal when a BLK pulse is input. 	0.13	0.43	0.74	V

No.	Measurement item	Symbol	Measurement contents	Min.	Typ.	Max.	Unit
14	Sync separator output rise delay	SDLYR		6.5	8.5	11	ns
	Sync separator output fall delay	SDLYF		6.5	8.8	11	
15	Sync separator output	Sync-Hi		3.9	4	—	V
		Sync-Lo		—	0.2	0.45	
16	Sync separator capacity	SyncChk	Gradually reduce the sync level when the duty is cycle 4.8% and 22.7% from 0.3Vp-p and measure the sync level at which the sync signals can be separated.	0.24	—	—	Vp-p
17	VDET output rise delay	DDLYR		5.5	7.2	10	ns
	VDET output fall delay	DDLYF		8.5	11.9	15.5	
18	VDET output	VDET-Hi		4	4.1	—	V
		VDET-Lo		—	0.25	0.4	

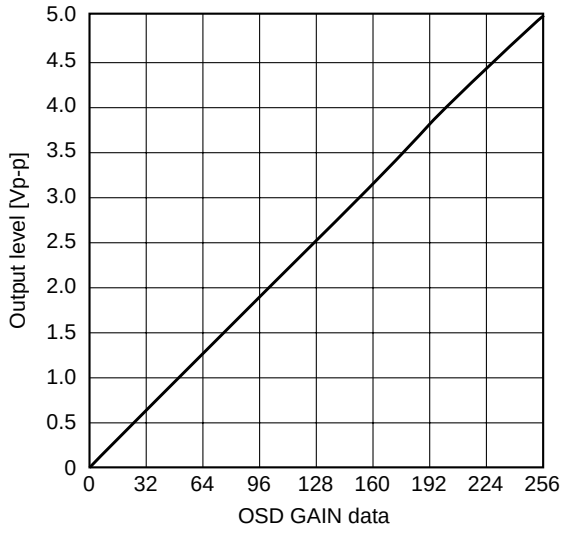
No.	Measurement item	Symbol	Measurement contents	Min.	Typ.	Max.	Unit
19	DAC output voltage (BKG = 00)	VBKG1	Measure the DAC output voltage (Pin 20) when BKG = 00/FF.	1.25	1.45	1.67	V
	DAC output voltage (BKG = FF)	VBKG2		5.45	5.7	5.95	
20	VDET output amplitude	VDET	Input the crosshatch signal of Dot Clock 100MHz/ 0.7p-p to the RGB inputs, and measure the VDET output amplitude. VDET LEVEL = 0 	3.35	3.8	4.4	Vp-p
21	Sharpness gain 1	SHP1	Input a 10MHz sin wave to RGB at an amplitude of 0.1Vp-p, and measure the output level. (CONTRAST: 7F/DRIVE: FF/ABL: 5V) SHP1: SHP GAIN = F/SHP SW = 0 SHP2: SHP GAIN = 0/SHP SW = 3 SHP3: SHP GAIN = F/SHP SW = 3 	0.3	0.4	0.5	Vp-p
	Sharpness gain 2	SHP2		0.3	0.4	0.5	
	Sharpness gain 3	SHP3		0.6	0.8	1.0	
22	Gamma correction	GAM1	Input 15 [IRE] and 60 [IRE] amplitude signals (100 [IRE] = 0.7Vp-p) to the RGB inputs, and measure the output amplitude. GAM1: GAMMA1 = 3/POL1 = 1, Vin = 0.105Vp-p GAM2: GAMMA1 = 3/POL1 = 0, Vin = 0.105Vp-p GAM3: GAMMA2 = F/POL2 = 1, Vin = 0.42Vp-p GAM4: GAMMA2 = F/POL2 = 0, Vin = 0.42Vp-p (CONTRAST: 7F/DRIVE: FF/ABL: 5V)	0.5	0.65	0.8	Vp-p
		GAM2		0.05	0.15	0.25	
		GAM3		1.8	2.1	2.4	
		GAM4		0.8	1.0	1.25	

Control Characteristics

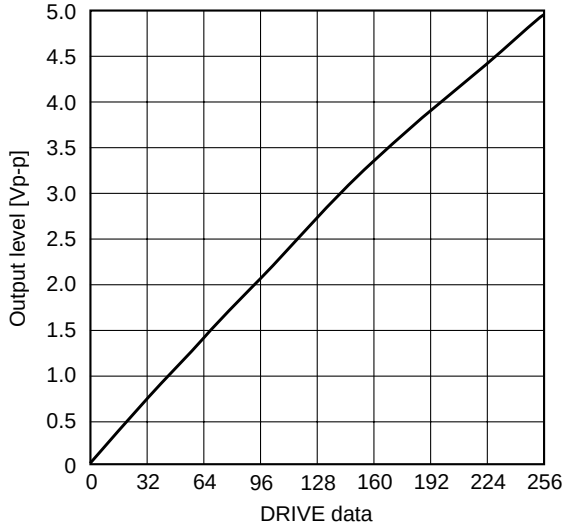
CONTRAST Control Characteristics



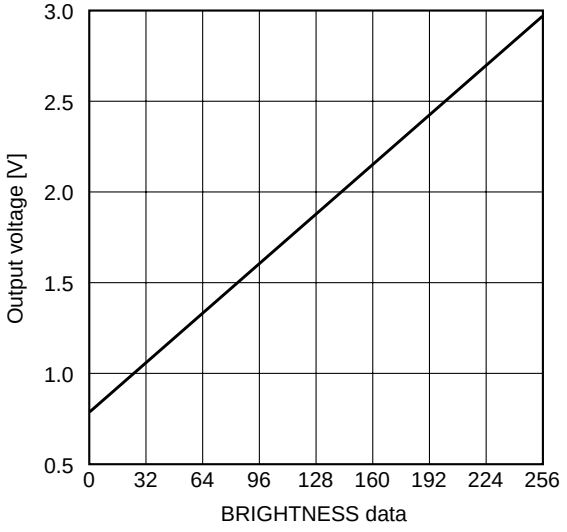
OSD GAIN Control Characteristics



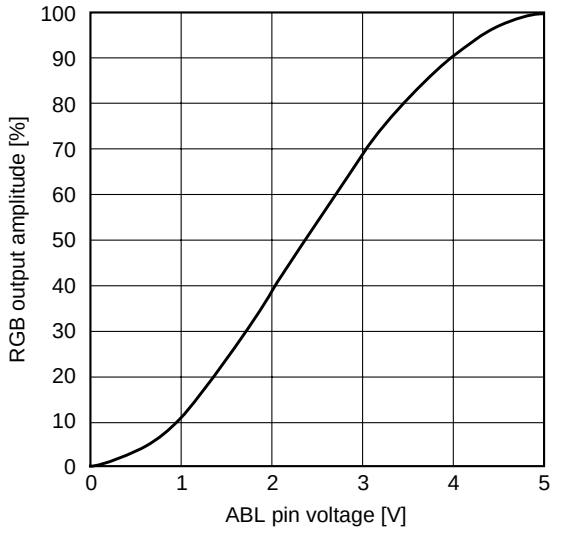
DRIVE Control Characteristics



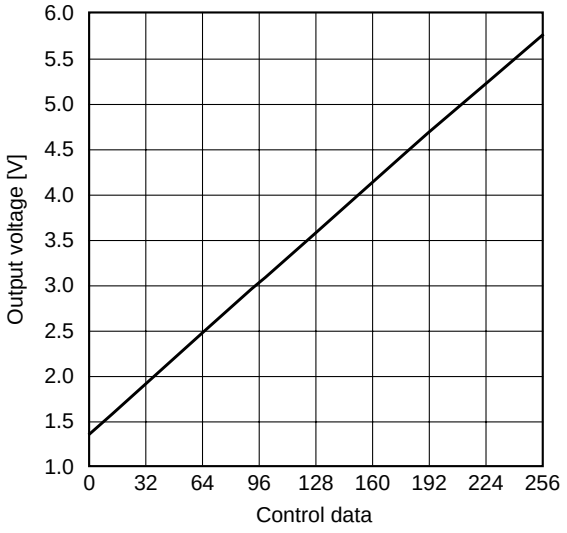
BRIGHTNESS Control Characteristics



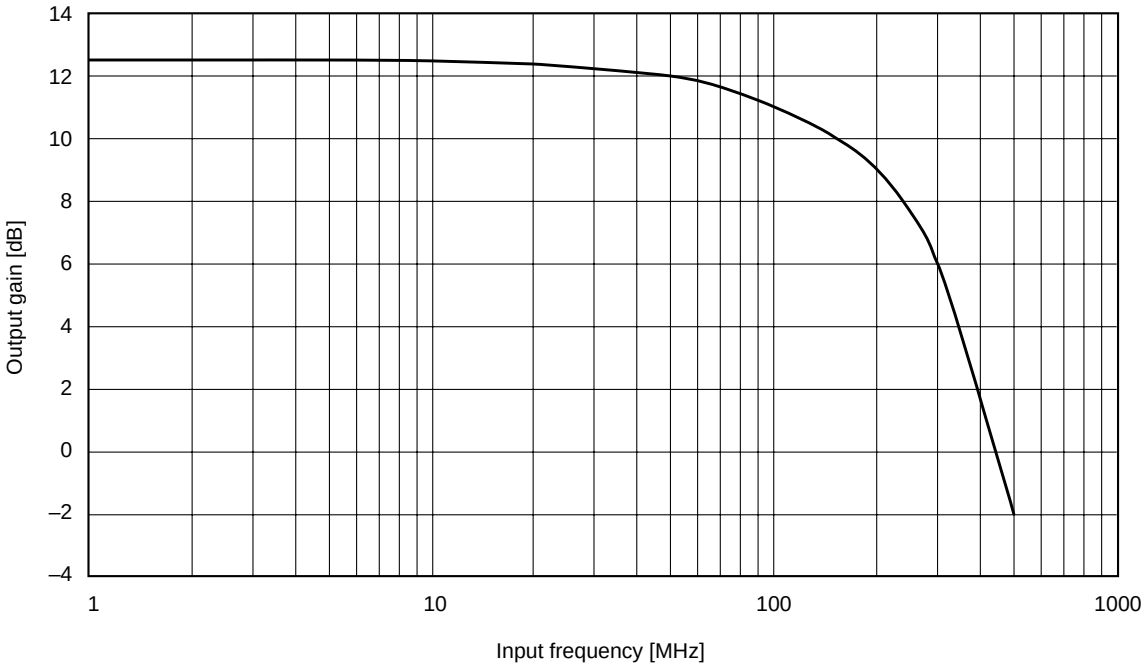
ABL Control Characteristics



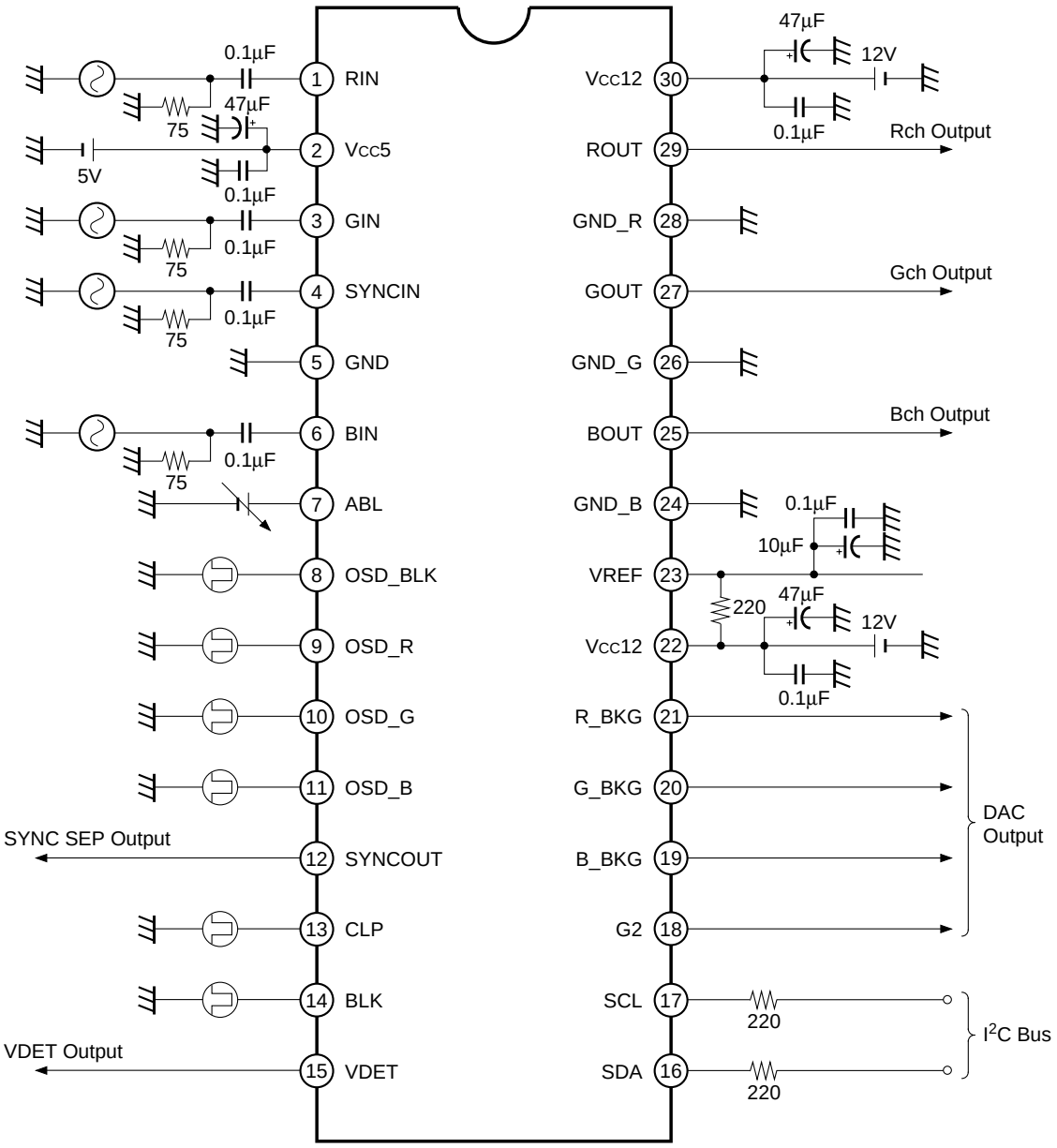
RGB BKG/G2 Control Characteristics



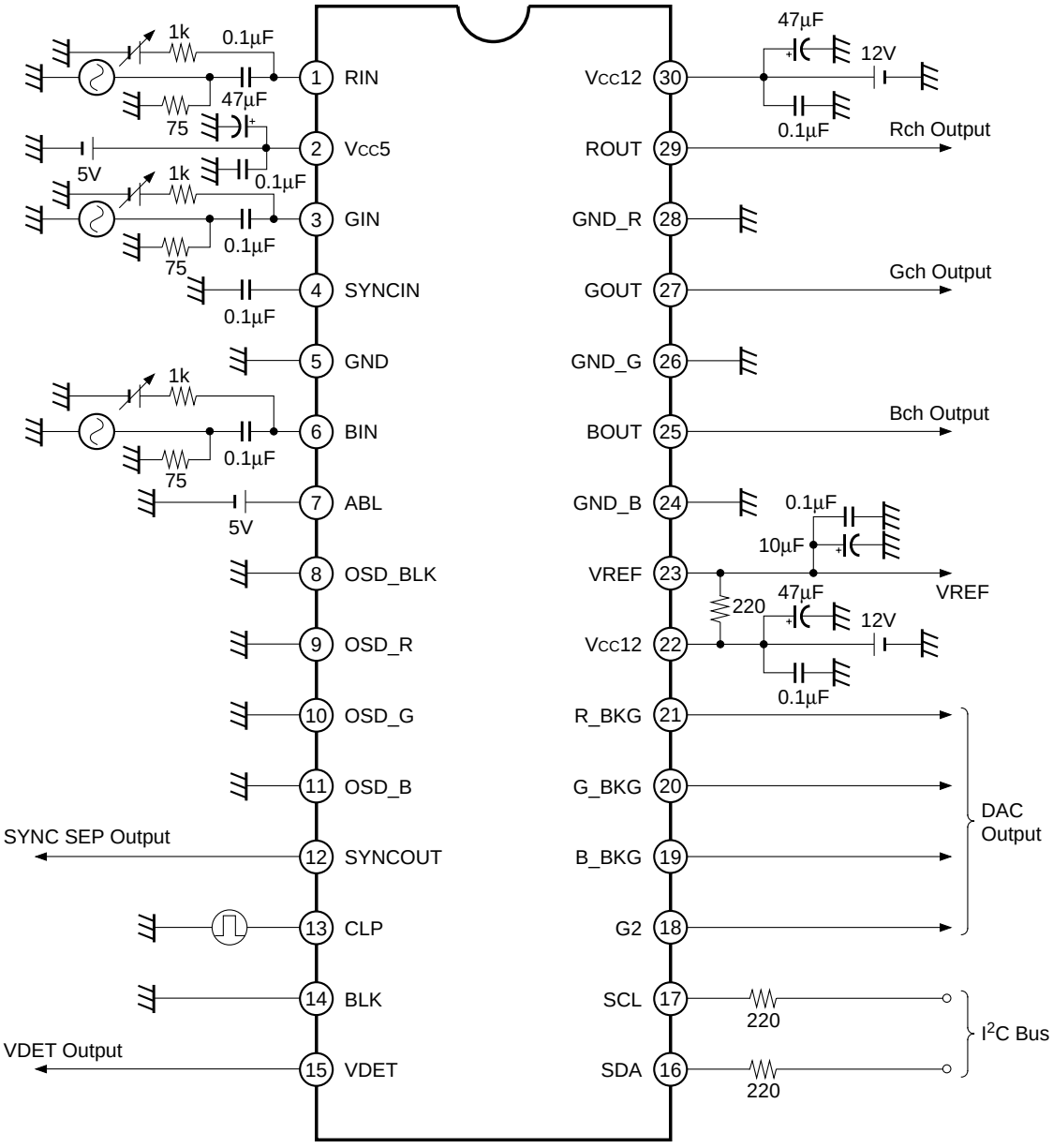
Frequency Characteristic



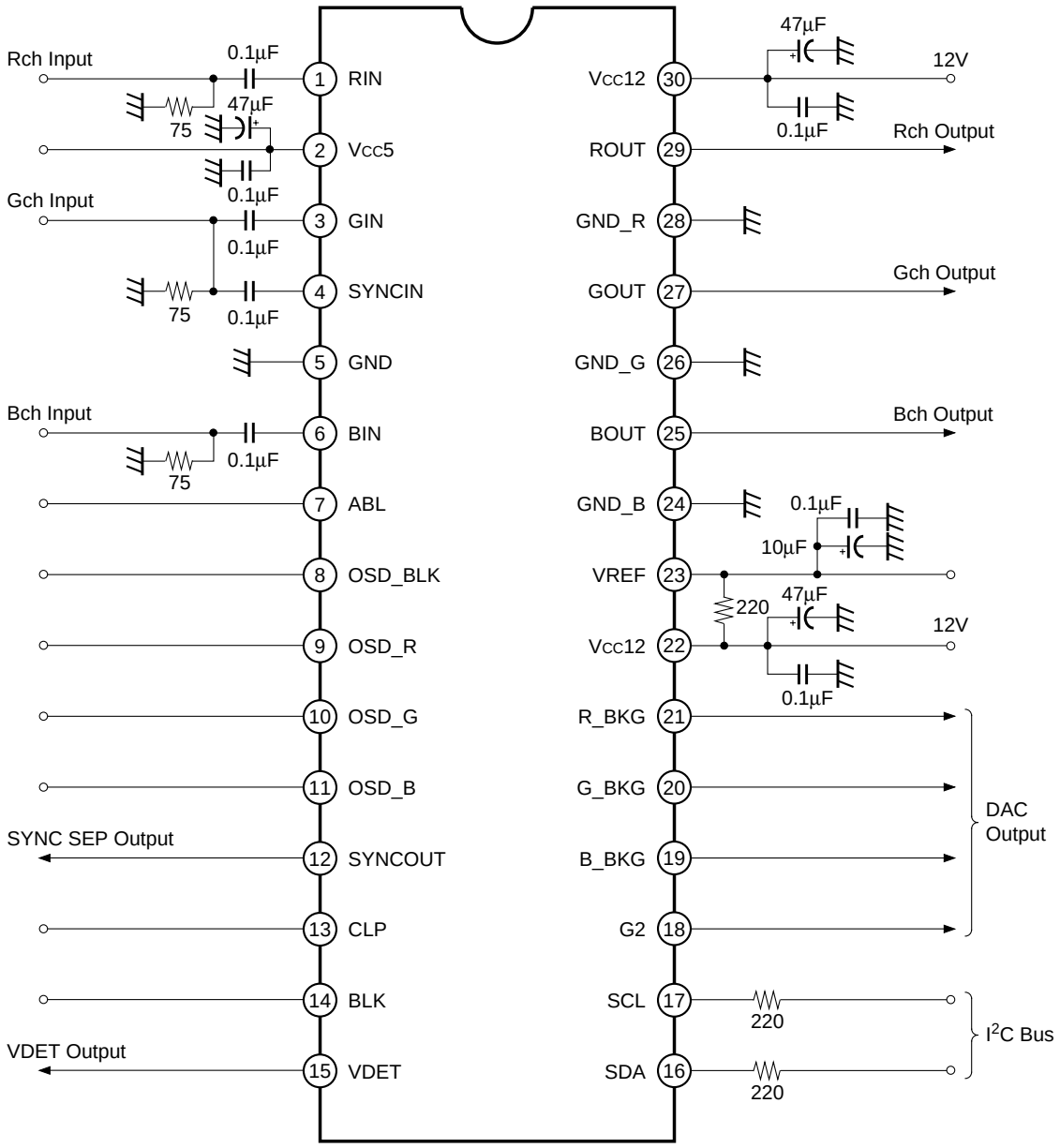
Electrical Characteristics Measurement Circuit



Electrical Characteristics Measurement Circuit (Frequency Response)



Application Circuit

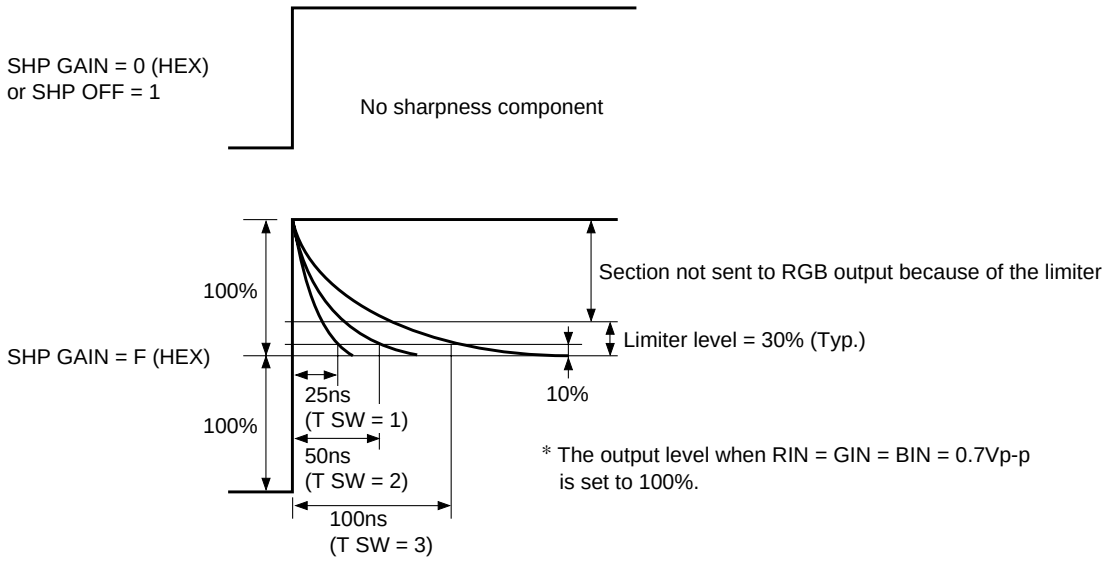


Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Description of Operation

1. Sharpness function

The RGB signals input to Pins 5, 7 and 10 are mixed at a ratio of 0.6G + 0.3R + 0.1B to form the Y signal. The high-frequency component is removed from this Y signal by a differentiation circuit, and the amplitude is controlled by a gain control circuit. The signal which undergoes gain control (sharpness component) has its amplitude clipped by a limiter circuit and is then added to the R, G and B signals.



2. VBLK synchronous DAC refresh system

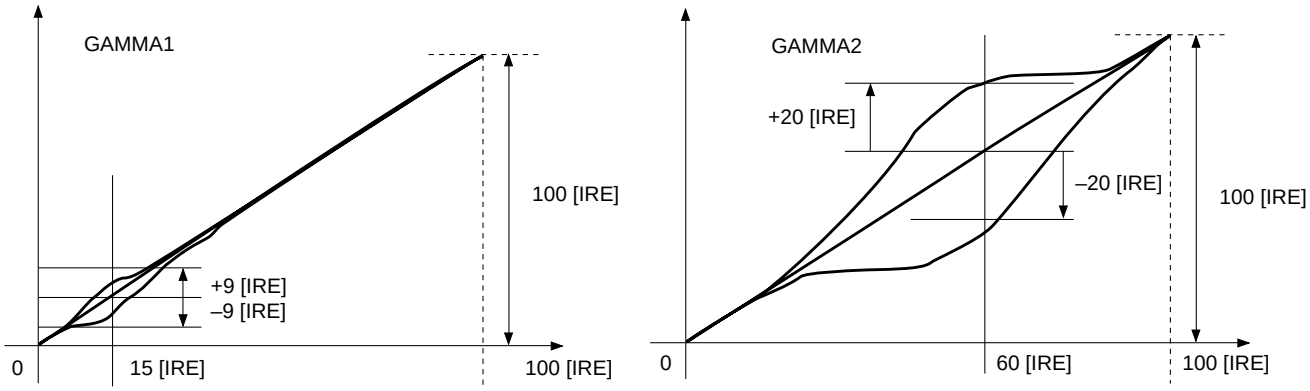
The VBLK signal is removed from the composite BLK signal which has been input to Pin 14, and the data for each control DAC is overwritten all at once in synchronization with this VBLK signal. The received I^2C bus data is held by a latch until the next VBLK signal arrives. As a result, I^2C bus data transmission from the microcomputer is timing-free. Set the width of the V blanking pulse which is input to Pin 14 to 300µs or more.

(See the next page)

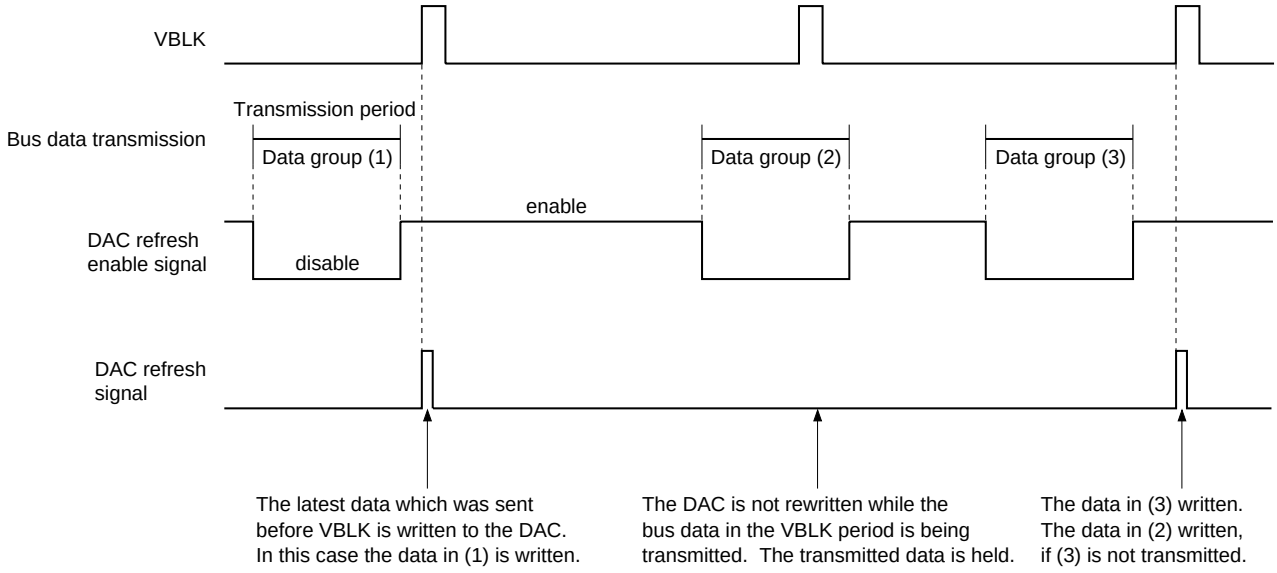
3. Gamma correction function

Using the output obtained when 700mVp-p RGB signals are input as a reference (100 [IRE]), the ±9 [IRE] (GAMMA1) and ±20 [IRE] (GAMMA2) waveforms can be corrected at the 15 [IRE] and 60 [IRE] inflection points, respectively.

The polarity switching gain can be controlled separately for each point, enabling correction broken at two points. The I^2C bus controls the polarity switching and gain correction.



VBLK Synchronous DAC Refresh System



The VBLK signal is extracted from the composite BLK signal which has been input to Pin 14, and the DAC data for each control is rewritten all at once in synchronization with this VBLK signal. The received I^2C bus data is held by a latch until the next VBLK signal arrives. Therefore, I^2C bus data transmission from the microcomputer is timing-free. Set the width of the V blanking pulse which is input to Pin 14 to 300µs or more.

Operation during power saving (Pin 22, V_{CC}12 OFF)

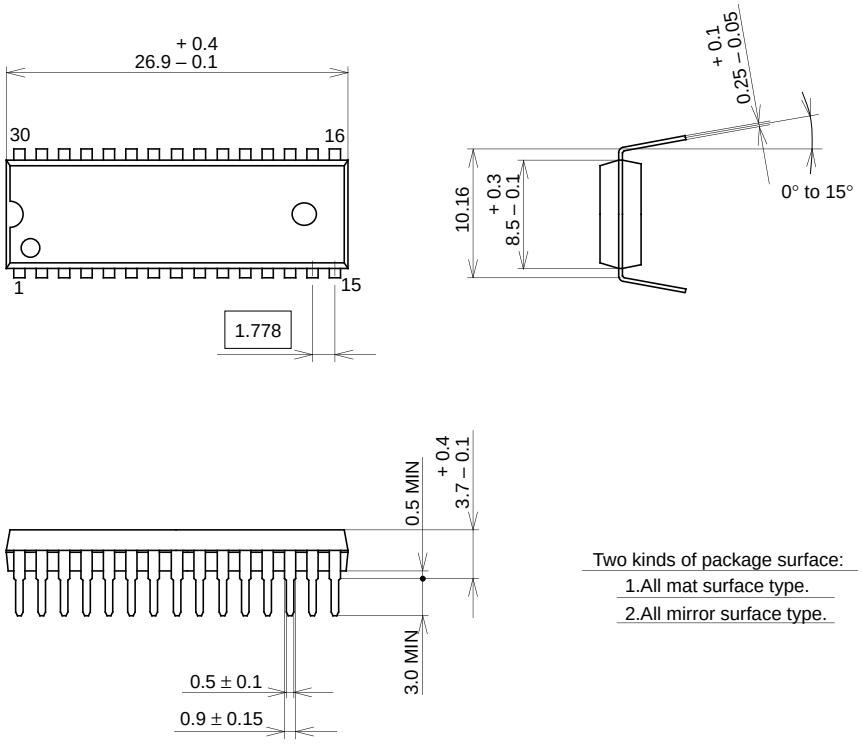
Only the sync separator function operates. All the other functions are shut down.

Notes on Operation

1. Set the output for ROUT, GOUT and BOUT for reception at high impedance.
2. Make the wiring from ROUT, GOUT and BOUT to the power amplifier as short as possible.
3. Connect the Vcc5, Vcc12 and VREF decoupling capacitors so that the ceramic capacitor and electrolytic capacitor are connected in parallel and the distance from the IC is less than 3mm.
4. Connect the clamp capacitors for RIN, GIN and BIN so that the distance from the IC is as short as possible.
5. Input the signals to RIN, GIN and BIN at low impedance via a clamp capacitor.
6. Set the output to OFF when the VDET/CSYNC output is not used. (Otherwise, this may cause the crosstalk to deteriorate.)
7. The VREF output cannot be used as an external power supply.
8. Turn the power on in the order of 5V $\rightarrow$ 12V, and off in the order of 12V $\rightarrow$ 5V. (Be sure to observe this order particularly during power-off, otherwise spots may remain on the screen.)
9. When applying blanking to the video period, the blanking pulse input to the BLK pin should have a high level of 4.7V or more.
10. When not using the sync separation function, connect the Sync In pin to GND through a capacitor, and set SOG_OFF = 1 (bus setting).
11. When there is no clamp pulse input to Pin 13 (CLP), the output potential rises. Always input a clamp pulse.

Package Outline Unit: mm

30PIN SDIP (PLASTIC)



Two kinds of package surface:
1.All mat surface type.
2.All mirror surface type.

SONY CODE	SDIP-30P-01
EIAJ CODE	P-SDIP30-8.5x26.9-1.778
JEDEC CODE	

PACKAGE STRUCTURE

MOLDING COMPOUND	EPOXY RESIN
LEAD TREATMENT	PALLADIUM PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	1.8g