SONY

CXA1854AR

Decoder/Driver/Timing Generator for Color LCD Panels

Description

The CXA1854AR is an IC designed exclusively to drive color LCD panels LCX009AK/AKB/LCX005BK/BKB. This IC greatly reduces the number of circuits and parts required to drive LCD panels by incorporating RGB decoder functions for video signals, driver functions, and a timing generator for driving panels onto a single chip.

Features

- Color LCD panels
  LCX009AK/AKB/LCX005BK/BKB driver
- Both NTSC/PAL compatible
- Supports composite inputs, Y/C inputs and Y/color difference inputs
- Band-pass filter, trap and delay line
- Sharpness function
- 2-point γ compensation circuits
- R, B output delay time adjustment circuit
  (supports both right and left inversion)
- Polarity reversed circuit / line inverted mode
- Supports external RGB input
- Supports line inversion
- Supports AC drive for LCD panel during no signal

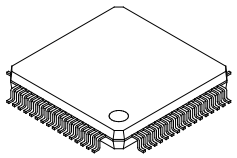
Applications

- Color LCD viewfinders
- Liquid crystal projectors
- Industrial monitors

Structure

Bipolar CMOS IC

64 pin LQFP (Plastic)



Absolute Maximum Ratings (Ta = 25°C)

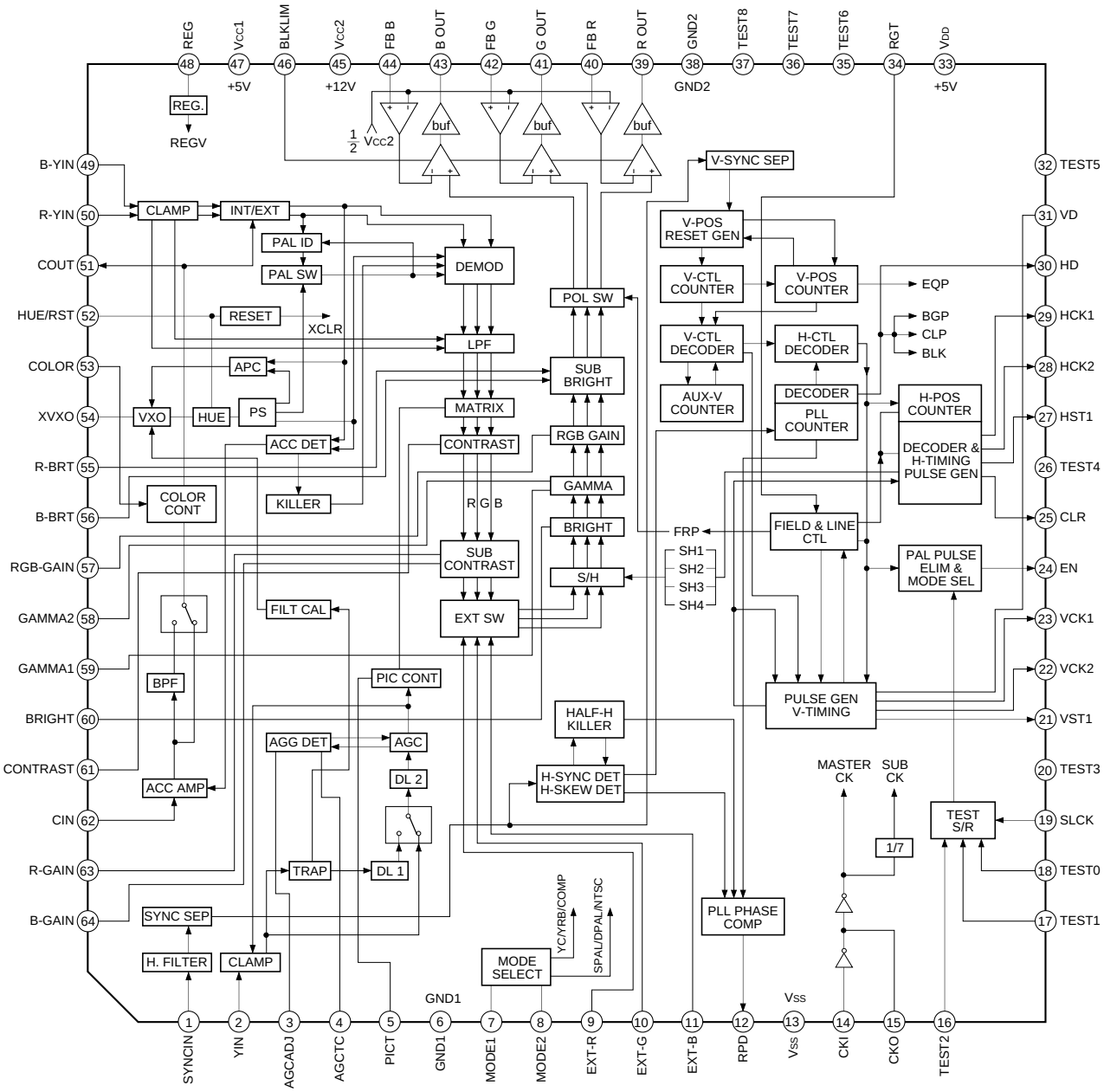
• Supply voltage	$V_{CC}1$ – GND	6	V
• Supply voltage	$V_{CC}2$ – GND	14	V
• Supply voltage	V_{DD} – V_{SS}	6	V
• Analog input pin voltage	VINA	–0.3 to $V_{CC}1$	V
• Digital input pin voltage	VIND	–0.3 to V_{DD} + 0.3	V
• Operating temperature range	Topr	–15 to +70	°C
• Storage temperature range	Tstg	–40 to +150	°C
• Allowable power dissipation	PD (Ta ≤ 70°C)	400	mW

Operating conditions

• Supply voltage	$V_{CC}1$ – GND	4.6 to 5.3	V
• Supply voltage	$V_{CC}2$ – GND	11.0 to 13.0	V
• Supply voltage			
LCX009 mode	V_{DD} – V_{SS}	4.5 to 5.5	V
LCX005 mode	V_{DD} – V_{SS}	2.7 to 5.5	V

E95X01A73

Block Diagram



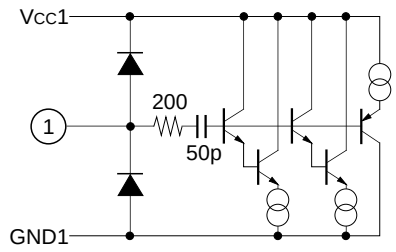
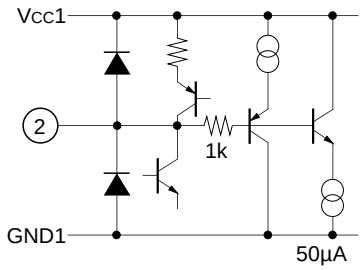
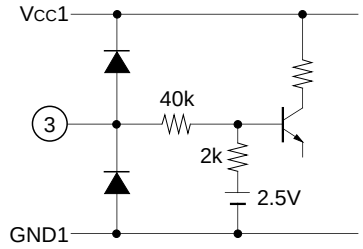
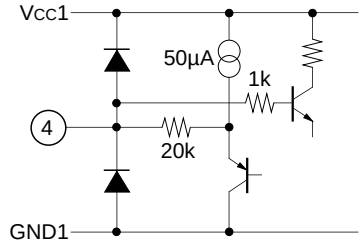
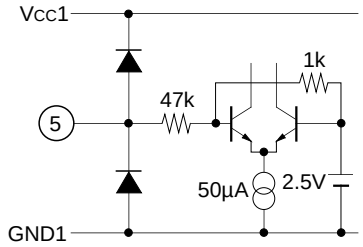
Pin Description (H: Pull up, M: Intermediate setting, L: Pull down)

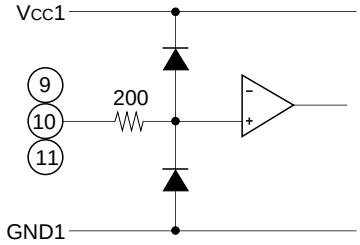
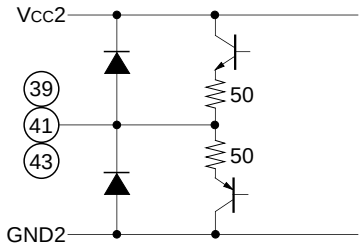
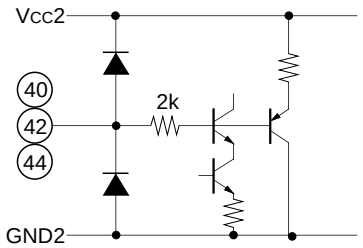
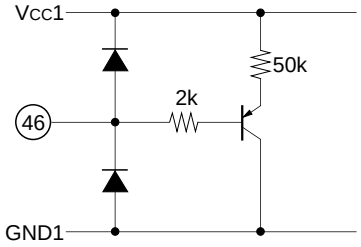
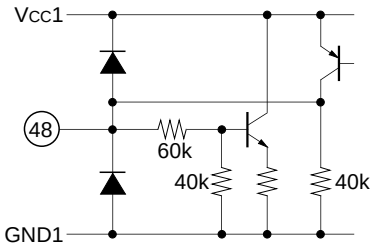
Pin No.	Symbol	I/O	Description	Input pin for open status
1	SYNC IN	I	Sync input	
2	Y IN	I	Y signal input	
3	AGCADJ	I	AGC level adjustment	
4	AGCTC	O	AGC time constant	
5	PICT	I	Y signal frequency characteristics adjustment	
6	GND1		Analog 5V GND	
7	MODE1	I	Switches between NTSC (H), DPAL* (M) and SPAL* (L)	M
8	MODE2	I	Switches between composite (H), Y/color difference (M) and YC input (L)	M
9	EXT-R	I	External digital input R (input conditions noted separately)	
10	EXT-G	I	External digital input G (input conditions noted separately)	
11	EXT-B	I	External digital input B (input conditions noted separately)	
12	RPD	O	Phase comparator output	
13	V_{SS}		Digital GND	
14	CKI	I	Oscillation cell input	
15	CKO	O	Oscillation cell output	
16	TEST2	I	Test	L
17	TEST1	I	Test	L
18	TEST0	I	Test	L
19	SLCK	I	Switches between LCX005BK (H) and LCX009AK (L)	L
20	TEST3	O	Leave this pin open.	
21	VST1	O	V start pulse 1 output	
22	VCK2	O	V clock pulse 2 output	
23	VCK1	O	V clock pulse 1 output	
24	EN	O	EN pulse output	
25	CLR	O	CLR pulse output	
26	TEST4	O	Leave this pin open.	
27	HST1	O	H start pulse 1 output	
28	HCK2	O	H clock pulse 2 output	
29	HCK1	O	H clock pulse 1 output	
30	HD	O	HD pulse output	
31	VD	O	VD pulse output	
32	TEST5	I	Leave this pin open.	L

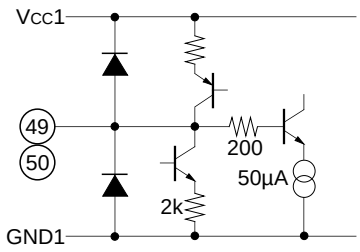
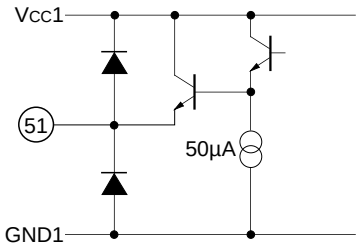
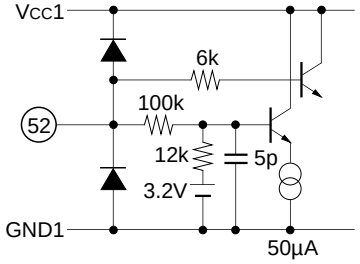
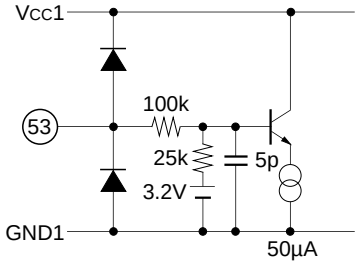
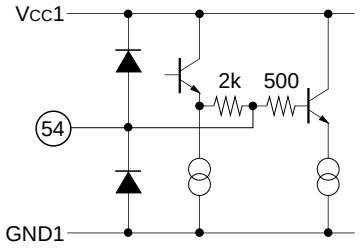
* DPAL supports demodulation methods which use an external delay line during demodulation; SPAL supports methods which internally process chroma demodulation.

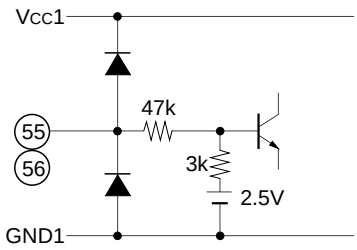
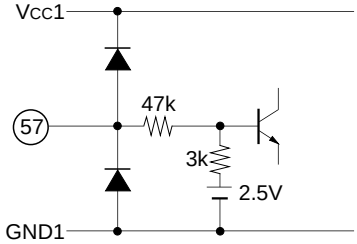
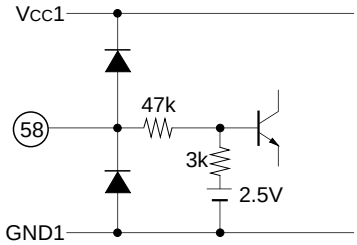
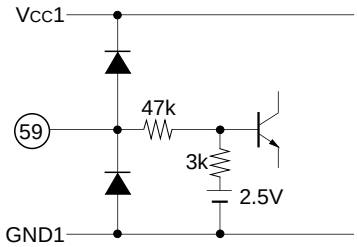
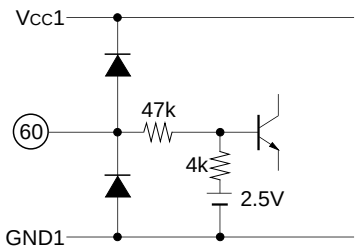
Pin No.	Symbol	I/O	Description	Input pin for open status
33	V_{DD}		Digital 5V power supply	
34	RGT	I	Switches between Normal scan (H) and Reverse scan (L)	H
35	TEST6	I	Leave this pin open.	H
36	TEST7	I	Leave this pin open.	H
37	TEST8	I	Leave this pin open.	H
38	GND2		Analog 12V GND	
39	R OUT	O	R output	
40	FB R	I	R signal DC voltage feedback input	
41	G OUT	O	G output	
42	FB G	I	G signal DC voltage feedback input	
43	B OUT	O	B output	
44	FB B	I	B signal DC voltage feedback input	
45	$V_{CC}2$		Analog 12V power supply	
46	BLKLIM	I	Black peak limiter level adjustment	
47	$V_{CC}1$		Analog 5V power supply	
48	REG	O	Constant voltage capacitor connection	
49	B-YIN	I	B-Y demodulator input (or B-Y/color difference signal input)	
50	R-YIN	I	R-Y demodulator input (or R-Y/color difference signal input)	
51	COUT	O	Chroma signal output (for PAL 1HDL)	
52	HUE/RST	I	Hue adjustment/system reset	
53	COLOR	I	Color adjustment	
54	XVXO	I	VXO crystal oscillator connection	
55	R-BRT	I	R brightness adjustment	
56	B-BRT	I	B brightness adjustment	
57	RGB-GAIN	I	RGB gain adjustment	
58	GAMMA2	I	γ 2 adjustment	
59	GAMMA1	I	γ 1 adjustment	
60	BRIGHT	I	Brightness adjustment	
61	CONTRAST	I	Contrast adjustment	
62	CIN	I	Chroma signal input	
63	R-GAIN	I	R gain adjustment	
64	B-GAIN	I	B gain adjustment	

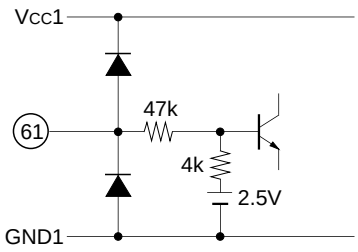
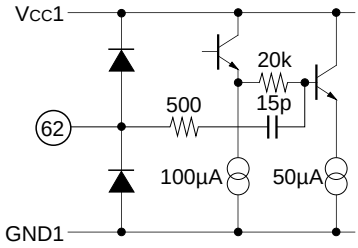
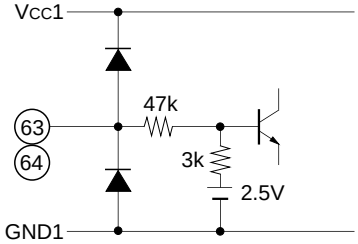
Analog Block Pin Description

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
1	SYNC IN			Sync input. Normally inputs the Y signal. The standard signal input level is 0.5Vp-p (up up to 100% white level from the sync chip).
2	YIN	3.2V		Y signal input. The standard signal input level is 0.5Vp-p (up to 100% white level from the sync chip). Input at low impedance (75Ω or less).
3	AGCADJ	Vcc1/2		AGC gain adjustment pin.
4	AGCTC			AGC detection filter connection.
5	PICT	Vcc1/2		Adjusts frequency characteristics of luminance signal. Increasing the voltage emphasizes contours.

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
9	EXT-R			External digital signal input. There are two threshold values: Vth1 (approximately 1.2V) and Vth2 (approximately 2.2V). When one of the EXT-RGB signals exceeds Vth1, all of the RGB outputs go to black level (black side clip level); when an input exceeds Vth2, only the corresponding output goes to white level (white side limiter level).
10	EXT-G			
11	EXT-B			
39	R OUT	$\frac{Vcc2}{2}$		RGB primary color signal output.
41	G OUT			
43	B OUT			
40	FB R			Smoothing capacitor connection for the feedback circuit of RGB output DC level control. Use a low-leakage capacitor because of high impedance.
42	FB G			
44	FB B			
46	BLKLIM			Sets the RGB output amplitude (black-black) clip level.
48	REG	4.2V		Smoothing capacitor connection for the internally generated constant voltage source circuit. Connect a capacitor of 1µF or more.

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
49	B-YIN			Color difference demodulation circuit inputs during DPAL mode. Leave this pin open for NTSC. Color difference signal is input respectively when Y/color difference input. (Standard input is 0.15Vp-p.) At this time, the bias is 3.5V.
50	R-YIN			
51	COUT	2.3V		Color adjusted chroma signal is output. When taking the chroma signal, connect to GND with a load resistor (approximately 5kΩ).
52	HUE/RST	3.2V		Color phase adjustment pin during NTSC. Use for detective axis adjustment of the R-Y/B-Y axes during SPAL. Also doubles as the reset pin. The system is reset when this pin is connected to GND.
53	COLOR	3.2V		Color adjustment.
54	XVXO	3.5V		Crystal oscillator connection.

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
55	RBRT	Vcc1/2		Fine adjustment for R and B signal brightness.
56	BBRT			
57	RGB-GAIN	Vcc1/2		Adjusts RGB output amplitude gain.
58	GAMMA2	Vcc1/2		Adjusts voltage gain change point γ 2.
59	GAMMA1	Vcc1/2		Adjusts voltage gain change point γ 1.
60	BRIGHT	Vcc1/2		RGB output brightness adjustment. It does not influence the γ compensation curve.

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
61	CONTRAST	Vcc1/2		Contrast adjustment.
62	CIN			Video signal input when using composite input. Chroma signal input when using Y/C input. Leave this pin open when Y/color difference input.
63	R-GAIN	Vcc1/2		Fine adjustment for R and B signal contrast.
64	B-GAIN			

Setting Conditions for Measuring Electrical Characteristics

When measuring the DC characteristics, the TG block must be horizontally synchronized by performing Setting 2. Setting 2 must also be performed when measuring the AC characteristics. When measuring items with bands greater than 2MHz such as the Y frequency response or sharpness characteristics, settings 1 and 3 must also be performed and measurements made with the sample-and-hold circuit set to through status.

Setting 1. System reset

After turning on the power, set SW52 to ON and start up V52 from GND in order to activate the timing controller system reset. (See Fig. 1-1.)

Setting 2. Horizontal AFC adjustment

Input SIG6 (VL = 0mV) to (A) and adjust VR12 so that WL and WH of the TP12 output waveform are the same. (See Fig. 1-2.)

Setting 3. S/H off

Input the signals shown in Fig. 1-3 to Pins 16, 17, 18 and 19 in order to set the sample-and-hold circuit to through status.

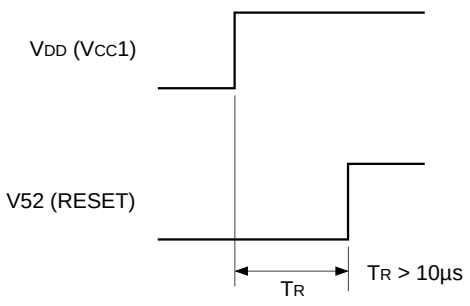


Fig. 1-1. System reset

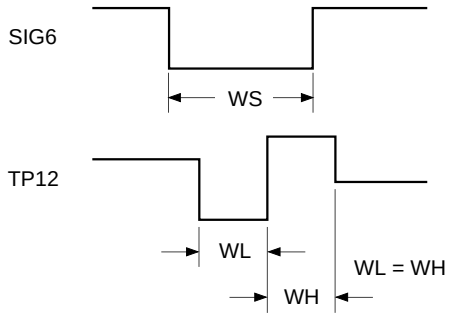


Fig. 1-2. Horizontal AFC adjustment

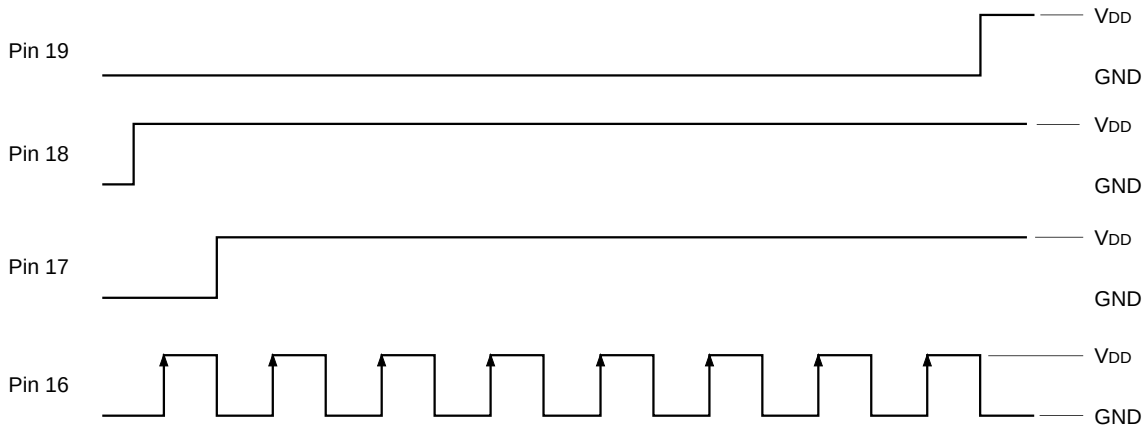


Fig. 1-3. S/H off input pattern

Electrical Characteristics – DC Characteristics (1)

Unless otherwise specified, Setting 2 and the following setting conditions are required.

$V_{CC}1$ = 5.0V, $V_{CC}2$ = 12.0V, GND1 = GND2 = GND, V_{DD} = 5.0V, V_{SS} = GND

V3, V5, V46, V55, V56, V57, V58, V59, V60, V61, V63, V64 = 2.5V

V52, V53 = 3.2V

SW3, SW5, SW46, SW52, SW53, SW55, SW56, SW57, SW58, SW59, SW60, SW61, SW63, SW64 = ON

Set SW7, SW8, SW9, SW10, SW11 and SW19 are setting A.

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power supply characteristics						
Current consumption $V_{CC}1$	$I_{CC}11$	Input SIG5 to (A) and SIG3 (0dB) to (B). Measure the $I_{CC}1$ current value. COMP input mode	35	44	53	mA
	$I_{CC}12$	Input SIG5 to (A) and SIG3 (0dB) to (B). Set SW8 to C. Measure the $I_{CC}1$ current value. Y/C input mode	34	42.5	51	mA
	$I_{CC}13$	Input SIG5 to (A) and SIG5 to (F) and (G). Set SW8 to B. Measure the $I_{CC}1$ current value. Y/color difference input mode	32	40	48	mA
Current consumption $V_{CC}2$	$I_{CC}2$	Input SIG5 to (A) and SIG3 (0dB) to (B). Measure the $I_{CC}2$ current value.	3	5.5	8	mA
Current consumption V_{DD}	$I_{DD}1$	Input SIG5 to (A) and SIG3 (0dB) to (B). Measure the I_{DD} current value. LCX009 mode	7	10.5	14	mA
	$I_{DD}2$	Input SIG5 to (A) and SIG3 (0dB) to (B). Set SW19 to B. Measure the I_{DD} current value. LCX005 mode	5	8	10.5	mA
	$I_{DD}3$	Input SIG5 to (A) and SIG3 (0dB) to (B). Set SW19 to B. Measure the I_{DD} current value. V_{DD} = 3.0V LCX005 mode	2	3	4.5	mA

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Digital block I/O characteristics							
Input current 1	II1	Input pin with pull-up resistor*1 VIN = V_{SS}	V_{DD} = 5.0V	–240	–100	–40	µA
			V_{DD} = 3.0V	–144	–60	–24	
Input current 2	II2	Input pin with pull-down resistor*2 VIN = V_{DD}	V_{DD} = 5.0V	40	100	240	µA
			V_{DD} = 3.0V	24	60	144	
High level output voltage Output pins except CKO and RPD	VOH1	IOH = –2mA*3	V_{DD} = 5.0V	V_{DD} –0.8			V
			V_{DD} = 3.0V	V_{DD} –1.0			
Low level output voltage Output pins except CKO and RPD	VOL11	IOL = 2mA*3	V_{DD} = 5.0V			0.5	V
			V_{DD} = 3.0V			0.6	
	VOL12	IOL = 500µA*3				0.3	V
High level output voltage CKO pin	VOH2	IOH = –3mA		0.5V_{DD}			V
Low level output voltage CKO pin	VOL2	IOL = 3mA				0.5V_{DD}	V
High level output voltage RPD pin	VOH3	IOH = –1mA		V_{DD} –1.2			V
Low level output voltage RPD pin	VOL3	IOL = 1.5mA				1.0	V
Output off leak current RPD pin	IOFF	High impedance status VOUT = V_{SS} or VOUT = V_{DD}		–40		40	µA
High level input voltage SLCK and RGT pins	VIH	CMOS input cell		0.7V_{DD}			V
Low level input voltage SLCK and RGT pins	VIL	CMOS input cell				0.3V_{DD}	V
Ternary input switching threshold voltage (MODE1/MODE2)	MDTHL	MODE M → L level threshold SW7, SW8 = B		0.2V_{DD}	0.3V_{DD}	0.4V_{DD}	V
	MDTHH	MODE M → H level threshold SW7, SW8 = B		0.6V_{DD}	0.7V_{DD}	0.8V_{DD}	V

*1 Input pins with pull-up resistors: RGT, TEST6, TEST7, TEST8

*2 Input pins with pull-down resistors: SLCK, TEST0, TEST1, TEST2, TEST5

*3 Output pins except CKO and RPD: HD, VD, VST1, VCK1, VCK2, CLR, EN, HST1, HCK1, HCK2, TEST3, TEST4

Electrical Characteristics – AC Characteristics (1)

Unless otherwise specified, Setting 2 and the following setting conditions are required.
Vcc1 = 5.0V, Vcc2 = 12.0V, GND1 = GND2 = GND, (V_{DD} = 5.0V, V_{SS} = GND)
V5, V55, V56, V57, V60, V61, V63, V64 = 2.5V V3, V58 = 0V V46, V59 = 5.0V
V52, V53 = 3.2V
SW3, SW5, SW46, SW52, SW53, SW55, SW56, SW57, SW58, SW59, SW60, SW61, SW63, SW64 = ON
Set SW7, SW8, SW9, SW10, SW11 and SW19 are setting A.
Unless otherwise specified, measure the non-reversed outputs for TP39, TP41 and TP43.

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Y signal block							
Video maximum gain	GV	Input SIG5 to (A) and measure the ratio between the output amplitude (white-black) and input amplitude at TP41.		13.5	16.5	19.5	dB
Y signal frequency Characteristics	FCYYC	Assume the output amplitude at TP41 when SIG2 (0dB, no burst, 100kHz) is input to (A) as 0dB. Vary the frequency of the input signal to obtain the frequency with an output amplitude of –3dB. Settings 1 and 3 are required.	Y/C input, SW8 = C	5.0			MHz
	FCYCMN		Composite input (NTSC)	2.5			MHz
	FCYCMP		Composite input (PAL), SW7 = C	3.0			MHz
Sharpness characteristics MAX	GSHPMXC	Assume the output amplitude at TP41 when SIG8 (100kHz) is input to (A) as 0dB. Obtain the output amplitude ratio for the input SIG8 (2.0MHz). V5 = 4.0V Settings 1 and 3 are required. Composite input		7	12		dB
	GSHPMXY	Assume the output amplitude at TP41 when SIG8 (100kHz) is input to (A) as 0dB. Obtain the output amplitude ratio for the input SIG8 (2.5MHz). V5 = 4.0V, SW8 = C Settings 1 and 3 are required. Y/C input		10	16		dB
Sharpness characteristics MIN	GSHPMNC	Assume the output amplitude at TP41 when SIG8 (100kHz) is input to (A) as 0dB. Obtain the output amplitude ratio for the input SIG8 (2.0MHz). V5 = 0V Settings 1 and 3 are required. Composite input			–1	2	dB
	GSHPMNY	Assume the output amplitude at TP41 when SIG8 (100kHz) is input to (A) as 0dB. Obtain the output amplitude ratio for the input SIG8 (2.5MHz). V5 = 0V, SW8 = C Settings 1 and 3 are required. Y/C input			1	4	dB

Item		Symbol	Conditions		Min.	Typ.	Max.	Unit
AGC characteristics	APL = 90%	GAPL90	Adjust the output amplitude at TP41 when SIG1 (APL: 50%) is input to (A) to 1.5Vp-p with V61. Assume this as 0 dB, and obtain the TP41 output amplitude ratio when input SIG1 (APL: 90%) is input. V3 = 2.5V, V60 = 3.5V		–4	–2.5	–1	dB
	APL = 10%	GAPL10	Adjust the output amplitude at TP41 when SIG1 (APL: 50%) is input to (A) to 1.5Vp-p with V61. Assume this as 0dB, and obtain the TP41 output amplitude ratio when input SIG1 (APL: 10%) is input. V3 = 2.5V, V60 = 3.5V		1	2.5	4	dB
Contrast characteristics MAX		GCNTMX	Input SIG5 to (A) and obtain the ratio between the TP41 output amplitude when V61 = 2.5V and the TP41 output amplitude when V61 = 5V.		2	5		dB
Contrast characteristics MIN		GCNTMN	Input SIG5 to (A) and obtain the ratio between the TP41 output amplitude when V61 = 2.5V and the TP41 output amplitude when V61 = 1V.			–10	–6	dB
Carrier leak (residual carrier)		CRRLK	Input SIG3 (0dB) to (A) and (B). Adjust the chroma signal phase so that the amplitude (black – white) at TP43 is at a maximum. Using a spectrum analyzer, measure the input and the 3.58MHz or 4.43MHz component, and obtain CRRLK = 150mV $\times$ $10^{\Delta d/20}$ using their difference Δd. SW7 = A for NTSC measurement, and C for PAL measurement.				30	mVpp
Y signal I/O delay time		TDYYC	Input SIG6 (VL = 150mV) to (A). Measure the delay time from the rising edge of the input signal to the rising edge of the non-reversed output. V5 = 2V	Y/C input SW8 = C	250	400	550	ns
		TDYCMN		Composite input (NTSC)	630	780	930	ns
		TDYCMP		Composite input (PAL), SW7 = C	610	760	910	ns

Electrical Characteristics – AC Characteristics (2)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Chroma signal block							
ACC amplitude characteristics 1	ACC1N	Input SIG6 (VL = 0mV) to (A) and SIG3 (0dB/+6dB/–20dB, 3.58MHz burst/chroma phase = 180°, or 4.43MHz burst/chroma phase = ±135°) to (B). Measure the output amplitude at TP51, assuming the output corresponding to 0dB, +6dB and –20dB as V0, V1 and V2, respectively. ACC1 = 20log (V1/V0) ACC2 = 20log (V2/V0)	NTSC	–3	0	+3	dB
	ACC1P		PAL SW7 = C	–3	0	+3	dB
ACC amplitude characteristics 2	ACC2N		NTSC	–3	0	+3	dB
	ACC2P		PAL SW7 = C	–3	0	+3	dB
APC pull-in range	FAPCNU	Input SIG6 (VL = 0mV) to (A) and SIG3 (0dB, 3.58MHz burst/chroma phase = 180°, or 4.43MHz burst/chroma phase = ±135°) to (B), and measure the output amplitude at TP43. Changing the SIG3 burst frequency, mesure the frequency fl which TP43 output changes (the killer mode is canceled). (The crystal parallel floating capacitance is 2pF or less) NTSC: FAPCN = fl – 3579545Hz PAL: FAPCP = fl – 4433619Hz	NTSC upper limit CL = 20pF	350			Hz
	FAPCND		NTSC lower limit CL = 20pF			–350	Hz
	FAPCPU		PAL upper limit SW7 = C CL = 16pF	350			Hz
	FAPCPD		PAL lower limit SW7 = C CL = 16pF			–350	Hz
Color adjustment characteristics MAX	GCOLMX	Input SIG6 (VL = 0mV) to (A) and SIG3 (0dB, 3.58MHz burst/chroma phase = 180°) to (B). Assume the chroma amplitude when V53 = 3.2V, 5V and 2.1V as V0, V1 and V2, respectively, and calculate GCOLMX = 20log (V1/V0) and GCOLMN = 20log (V2/V0).		3	5.5		dB
Color adjustment characteristics MIN	GCOLMN				–20	–15	dB
HUE adjustment range MAX	TNTMX	Input SIG6 (VL = 0mV) to (A) and SIG3 (0 dB) to (B). Assume the phase at which the output amplitude at TP43 reaches a minimum when V53 = 3.2V, 5V and 1.6V as $\theta 0$, $\theta 1$ and $\theta 2$, respectively, and calculate TNTMX = $\theta 1 - \theta 0$ and TNTMN = $\theta 2 - \theta 0$.		30			deg
HUE adjustment range MIN	TNTMN					–30	deg
Killer operation input level	ACKN	Input SIG6 (VL = 0mV) to (A) and SIG3 (level variable, 3.58MHz burst/chroma phase = 180°, or 4.43MHz burst/chroma phase = ±135°) to (B), and measure the output amplitude at TP43. Gradually reduce the SIG3 amplitude and measure the level at which the killer operation is activated.	NTSC		–36	–30	dB
	ACKP		PAL SW7 = C		–33	–27	dB

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Demodulation output amplitude ratio (NTSC)	VRBN	Input SIG6 (VL = 0mV) to (A) and SIG3 (0dB, 3.58MHz) to (B) and change the chroma phase. Assume the maximum amplitude at TP39 as VR, the maximum amplitude at TP41 as VG, and the maximum amplitude at TP43 as VB, and calculate VRBN = VR/VB and VGBN = VG/VB. V60 = 3.5V	0.53	0.63	0.73	
	VGBN		0.25	0.32	0.39	
Demodulation output phase difference (NTSC)	θRBN	Input SIG6 (VL = 0mV) to (A) and SIG3 (0dB, 3.58MHz) to (B) and change the chroma phase. Assume the phase at which the maximum amplitude at TP39, TP41 and TP43 as θR, θG and θB, respectively, and calculate θRBN = θR – θB and θGBN = θG – θB. V60 = 3.5V	99	109	119	deg
	θGBN		230	242	254	deg
Demodulation output amplitude ratio (PAL)	VRBP	Input SIG6 (VL = 0mV) to (A) and SIG3 (0 dB, 4.43MHz) to (B) and change the chroma phase. Assume the maximum amplitude at TP39 as VR, the maximum amplitude at TP41 as VG, and the maximum amplitude at TP43 as VB, and calculate VRBP = VR/VB and VGBP = VG/VB. V60 = 3.5V, SW7 = C	0.65	0.75	0.85	
	VGBP		0.33	0.40	0.47	
Demodulation output phase difference (PAL)	θRBP	Input SIG6 (VL = 0mV) to (A) and SIG3 (0 dB, 4.43MHz) to (B) and change the chroma phase. Assume the phase at which the maximum amplitude at TP39, TP41 and TP43 as θR, θG and θB, respectively, and calculate θRBP = θR – θB and θGBP = θG – θB. V60 = 3.5 V, SW7 = C	80	90	100	deg
	θGBP		232	244	256	deg

Electrical Characteristics – AC Characteristics (3)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
RGB signal output characteristics						
RGB output DC voltage	VOUT	Input SIG6 (VL = 0mV) to (A). Adjust V60 so that the output (black-black) at TP41 is 9Vp-p and measure the DC voltage at TP39, TP41 and TP43.	5.85	6.05	6.25	V
RGB output DC voltage difference	ΔVOUT	Input SIG6 (VL = 0mV) to (A). Adjust V60 so that the output (black-black) at TP41 is 9Vp-p, measure the DC voltage at TP39, TP41 and TP43, and obtain the maximum difference between these values.		0	100	mV
Amount of change in brightness	BRTMX	Input SIG6 (VL = 0mV) to (A) and measure the output (black-black) at TP39, TP41 and TP43 when V60 = 0V.	9.0			V
	BRTMN	Input SIG6 (VL = 0mV) to (A) and measure the output (black-black) at TP39, TP41 and TP43 when V60 = 5V.			3.0	V
Amount of change in sub-brightness	SBBRT	Input SIG6 (VL = 0mV) to (A) and measure the difference between the outputs (black-black) at TP39 and TP43 and the output (black-black) at TP41 when V55 and V56 = 1V and when V55 and V56 = 4V.	±2	±4		V
Amount of change in sub-contrast	SBCNT	Input SIG5 to (A) and measure the difference between the outputs (white-black) at TP39 and TP43 and the output (white-black) at TP41 when V63 and V64 = 1V and when V63 and V64 = 4V.	±2			dB
Difference in RGB reversed/ non-reversed gain	ΔG (NR)	Input SIG5 to (A) and obtain the gain difference between the non-reversed output amplitudes (white-black) and the reversed output amplitudes at TP39, TP41 and TP43.	–0.6	0	0.6	dB
γ characteristics						
γ gain	G γ 1	Input SIG9 to (A) and adjust the non-reversed output amplitude (white-black) at TP41 to 4Vp-p with V61. Calculate the following: G γ 1 = 20log (VG1/0.0357) G γ 2 = 20log (VG2/0.0357) G γ 3 = 20log (VG3/0.0357) (See Fig. 6 for definitions of VG1, VG2 and VG3.)	21.5	25.5	29.5	dB
	G γ 2		9.5	12.5	15.5	dB
	G γ 3		18.5	23.5	26.5	dB
V γ 1 adjustment variable range	V γ 1MN	Input SIG4 to (A) and adjust the output amplitude (white-black) at TP41 to 4Vp-p with V61 when V57 and V58 = 0V and V59 = 5V. Measure the point where the gain of the non-reversed output at TP41 changes and the voltage difference V γ 1 between this output and V_{CC}2/2 when V59 = 0V and when V59 = 2.7V. V γ 1MN when V59 = 0V, and V γ 1MX when V59 = 2.7V (See Fig. 7.)			2.0	V
	V γ 1MX		3.5			V
V γ 2 adjustment variable range	V γ 2MN	Input SIG4 to (A) and adjust the output amplitude (white-black) at TP41 to 4Vp-p with V61 when V57 and V58 = 0V. Measure the point where the gain of the non-reversed output at TP41 changes and the voltage difference V γ 2 between this output and V_{CC}2/2 when V58 = 5V and when V58 = 1.5V. V γ 2MN when V58 = 5V and V γ 2MX when V58 = 1.5V. (See Fig. 7.)			0.9	V
	V γ 2MX		2.0			V

Electrical Characteristics – AC Characteristics (4)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Sync separation, TG block							
Sync separation input voltage sensitivity	VSSEP	Input SIG6 (VL = 0mV, WS = 4.7µs, VS variable) to (A) and confirm that it is synchronized with the output at TP30. Gradually reduce the VS of SIG6 from 143mV and obtain the VS at which input and output become non-synchronized.			40	60	mV
HD output delay time	TDHDH	Input SIG6 (VL = 0mV, VS = 143mV, WS = 4.7µs) to (A) and measure the delay time with the output at TP30. TDHDH is from the falling edge of the input sync signal to the rising edge of TP30, and TDHDL from the rising edge of the input sync signal to the falling edge of TP30.		2.9	3.2	3.5	µs
	TDHDL			4.4	4.7	5.0	µs
Horizontal pull-in range	HPLLN	Input SIG6 (VL = 0mV, VS = 143mV, WS = 4.7µs, horizontal frequency variable) to (A) and confirm that it is synchronized with the output at TP30. Obtain the frequency fH where the input and output are synchronized by changing the horizontal frequency of SIG6 from the non-synchronized condition. HPLLN = fH – 15734, HPLLP = fH – 15625	NTSC	±500			Hz
	HPLLP		PAL SW7 = C	±500			Hz
External I/O characteristics							
External RGB input threshold voltage	VT1EXT	Input SIG6 (VL = 0mV) to (A) and SIG7 (VL variable) to (C), (D) and (E). Raise the amplitude from 0 V and assume the voltage, where the outputs at TP39, TP41 and TP43 go to black level as VT1EXT. Then raise the amplitude further and assume the voltage where these outputs go to white level as VT2EXT. SW9 = B, SW10 = B, SW11 = B		1.0	1.2	1.4	V
	VT2EXT			2.0	2.2	2.4	V
Propagation delay time between external RGB input and output	TD1EXT	Input SIG6 (VL = 0 mV) to (A) and SIG7 (VL = 3 V) to (C), (D) and (E), and adjust the output amplitudes at TP39, TP41 and TP43 to 2.0V with V57. Measure the rise delay time TD1EXTand the fall delay time TD2EXT. SW9 = B, SW10 = B, SW11 = B (See Fig. 2.)		100	200	300	ns
	TD2EXT			100	200	300	ns
Black level voltage during external RGB input	EXTBK	Input SIG6 (VL = 0mV) to (A) and SIG7 (VL = 1.7V) to (C), (D) and (E), and measure the difference from the black level of the outputs at TP39, TP41 and TP43. SW9 = B, SW10 = B, SW11 = B				0	V
White level voltage during external RGB input	EXTWT	Input SIG6 (VL = 0mV) to (A) and SIG7 (VL = 2.7V) to (C), (D) and (E), and measure the difference from the black level of the outputs at TP39, TP41 and TP43. SW9 = B, SW10 = B, SW11 = B		1.8	2.2		V

Electrical Characteristics – AC Characteristics (5)

Item	Symbol	Conditions			Min.	Typ.	Max.	Unit
Filter characteristics								
BPF center frequency	F0BPFN	Input SIG6 (VL =0 mV) to (A) and SIG2 (0dB, frequency variable) to (B). Obtain frequencies fc1 and fc2 which reduce the output amplitude by 3dB from the maximum output at TP51 by changing the frequency, and calculate F0BPF = (fc1 + fc2)/2. Settings 1 and 3 are required.		NTSC	3.33	3.58	3.83	MHz
	F0BPFP			PAL SW7 = C	4.13	4.43	4.73	MHz
Amount of BPF attenuation	ATBPF	Input SIG6 (VL = 0mV) to (A) and SIG2 (0dB, frequency variable) to (B). Assume TP51 when the center frequency is input as 0dB and measure the output level at TP51 when the frequencies noted on the right are input. Settings 1 and 3 are required.	NTSC	2.78MHz	–7	–3	–1	dB
				1.50MHz		–23	–15	dB
			PAL SW7 = C	3.23MHz	–8	–3	–1	dB
				2.00MHz		–20	–15	dB
Amount of TRAP attenuation	ATRAPN	Input SIG2 (0dB, 3.58MHz, 4.43MHz) to (A) and measure the output at TP41 with a spectrum analyzer. Assume the output during Y/C mode (SW8 = A) as 0dB and measure the amount of attenuation during COMP mode (SW8 = C). Settings 1 and 3 are required.		NTSC			–35	dB
	ATRAPP			PAL SW7 = C			–35	dB
R-Y, B-Y and LPF characteristics	DEMLP	Input SIG6 (VL = 0mV) to (A) and SIG2 (amplitude 100mV, frequency variable) to (F) and (G). Assume the output amplitude at TP41 when 100kHz is input as 0dB, and measure the frequency which attenuates the output amplitude by –3dB.			0.6	0.8	1.2	MHz
Digital block I/O characteristics								
Output transition time (Note 3 pins)	tTLH	Input SIG6 (VL = 0mV) to (A). Load 30pF (See Fig. 4.) V3, V46, V58, V59 = 2.5V					30	ns
	tTHL						25	ns
Cross-point time difference	ΔT	Input SIG6 (VL = 0 mV) to (A). Load 30pF (see Fig. 5.) HCK1/HCK2 V3, V46, V58, V59 = 2.5V					10	ns
HCK duty	DTYHC	Input SIG6 (VL = 0mV) to (A). Measure the HCK1 and HCK2 output duty. Load 30pF V3, V46, V58, V59 = 2.5V			47	50	53	%

Description of Electrical Characteristics Measurement Methods

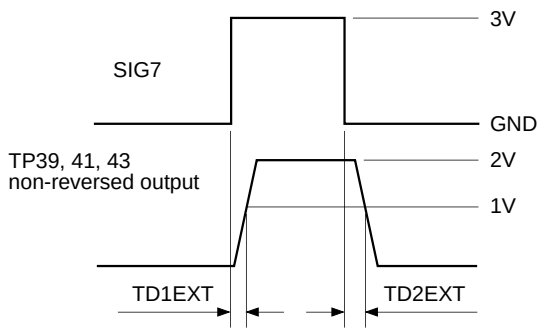


Fig. 2. Measuring the delay between external RGB input and output

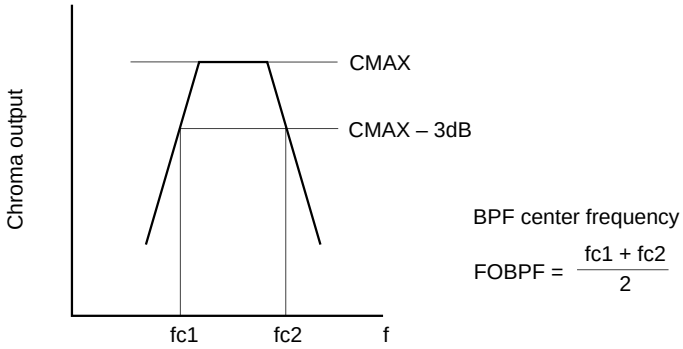


Fig. 3. BPF center frequency

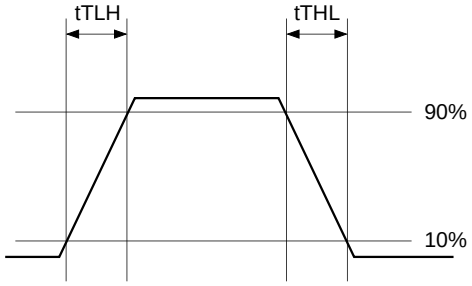


Fig. 4. Output transition time measurement condition

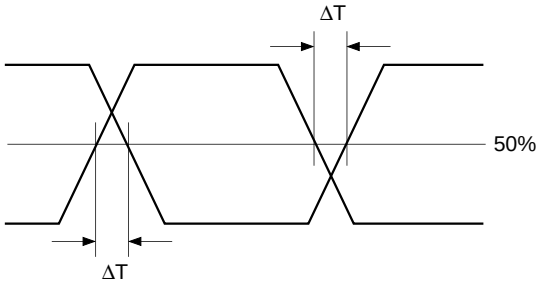


Fig. 5. Cross-point time difference measurement condition

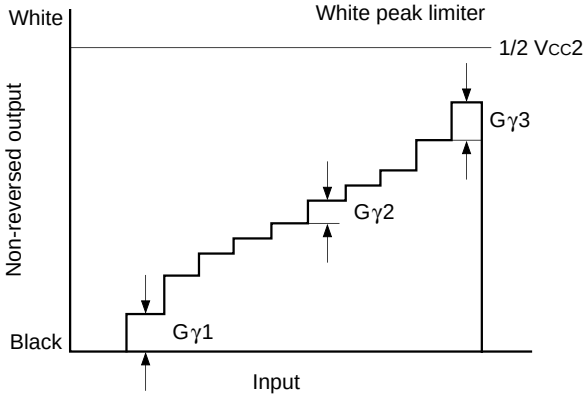


Fig. 6. γ characteristics measurement condition

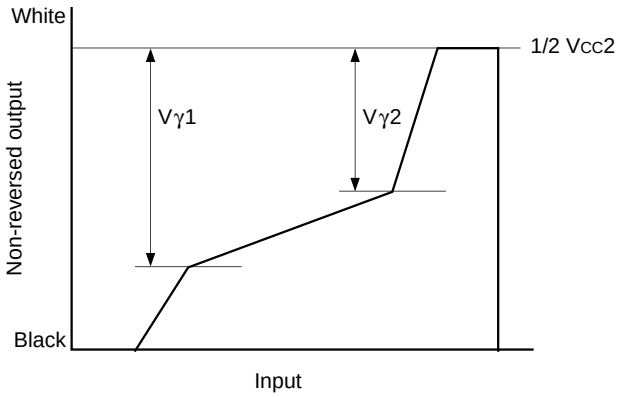
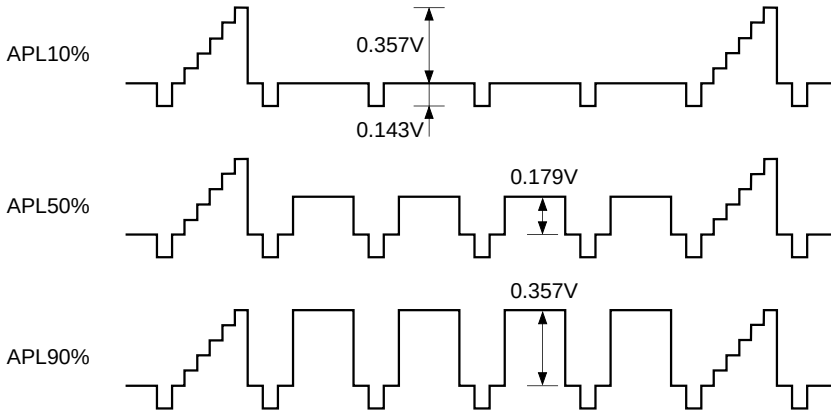
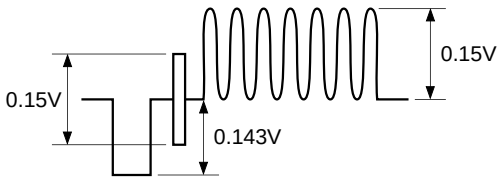
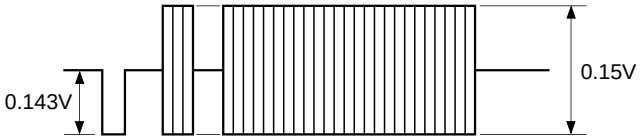
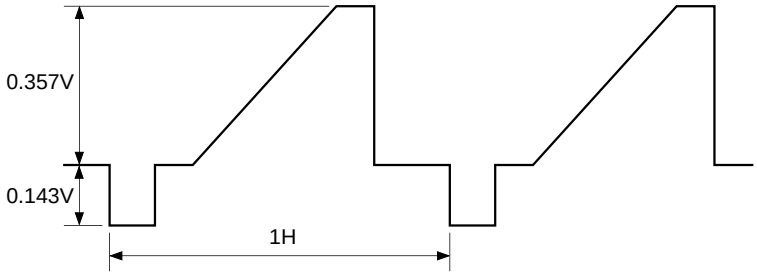
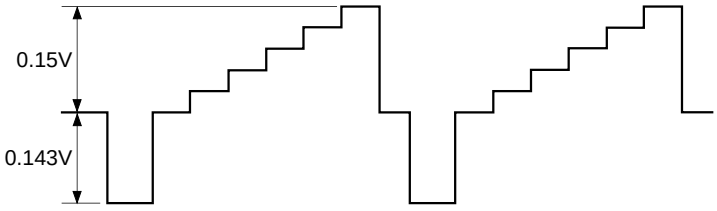
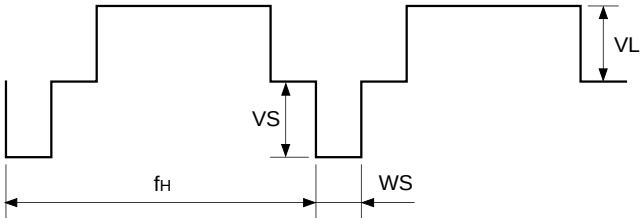
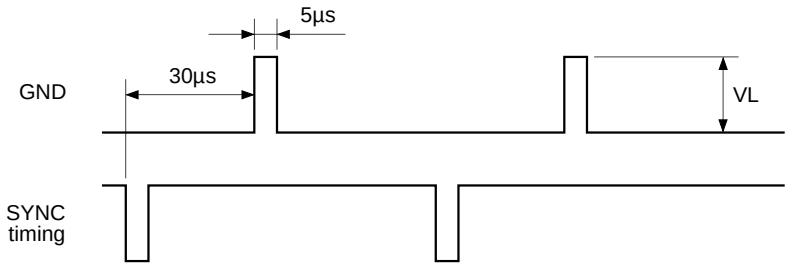
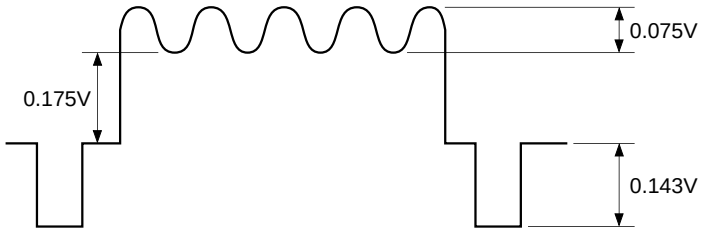
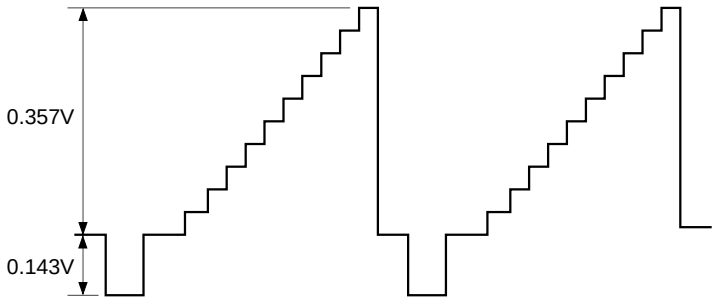


Fig. 7. γ adjustment variable range

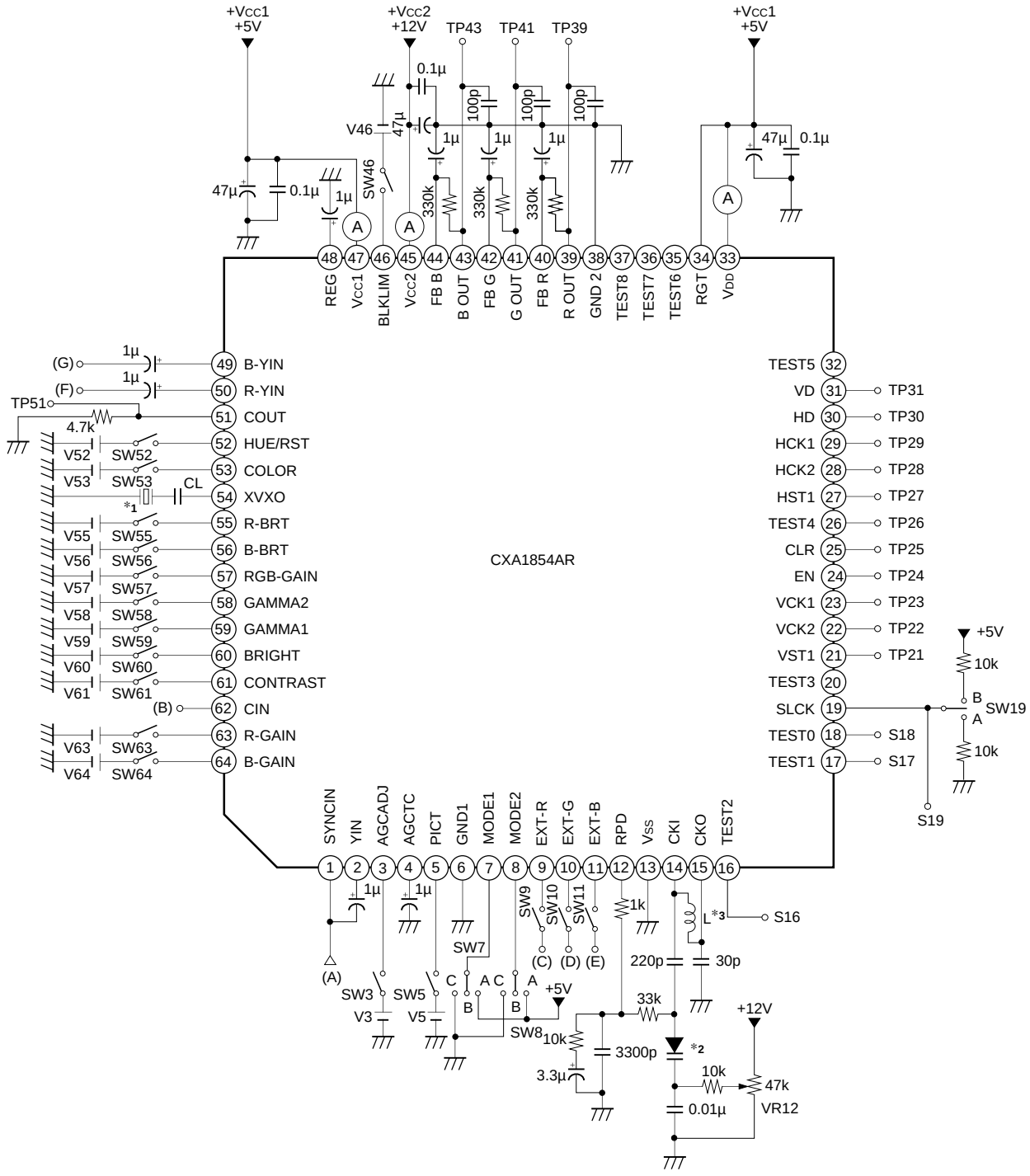
Input Waveforms (1)

SG No.	Waveform
SIG1	APL variable, 5-step waveform 
SIG2	 Sine wave video signal with burst. (Amplitude and frequency are variable.) VSWEEP
SIG3	Chroma signal: Burst, chroma frequency (3.579545MHz, 4.433619MHz) Chroma phase and burst frequency variable 
SIG4	Lamp waveform 
SIG5	5-step waveform 

Input Waveforms (2)

SG No.	Waveform
SIG6	 VL amplitude is variable. VS variable: 143mV unless otherwise specified WS variable: 4.7µs unless otherwise specified fH variable: 15.734kHz (NTSC) or 15.625kHz (PAL) unless otherwise specified
SIG7	 VL amplitude is variable.
SIG8	 Frequency variable
SIG9	10-step waveform 

Electrical Characteristics Measurement Circuit



*1 Used crystal: KINSEKI CX-5F
Frequency deviation: within ±30ppm,
frequency temperature characteristics: within ±30ppm
During NTSC: 3.579545MHz, load capacity: 16pF, CL = 20pF
During PAL: 4.433619MHz, load capacity: 16pF, CL = 16pF
Measure under the condition that the crystal parallel floating capacitance is within 2pF.

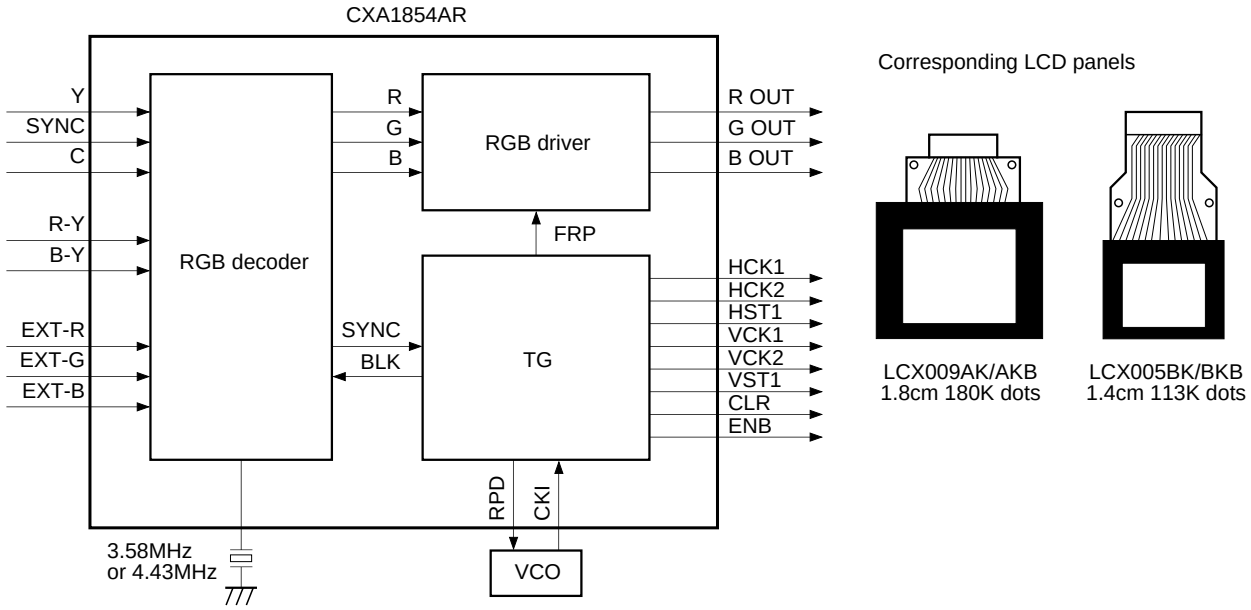
*2 Vari-cap diode: 1T369 (SONY)

*3 L value: 10µH when using the LCX005
4.7µH when using the LCX009

Description of Operation

The CXA1854AR incorporates the three functions of an RGB decoder block, an RGB driver block and a timing generator (TG) block onto a single chip using BiCMOS technology. This section describes these functions and their mutual relationship.

1) Description of the overall configuration



2) Description of RGB decoder block operation

• Input mode switching

Signal input: Composite input, Y/C input and Y/color difference input switching is supported by Pin 8 (MODE2).

During composite input: The composite signal is input to Pins 1, 2 and 62.

During Y/C input: The Y signal is input to Pins 1 and 2, and the C signal to Pin 62.

During Y/color difference input: The Y signal is input to Pins 1 and 2, the R-Y signal to Pin 50, and the B-Y signal to Pin 49.
(Chroma signal input (delay line output) is also used during PAL, but is switched with the MODE1 setting.)

Recommended input signal voltages for each mode are shown in the Pin Description table. The Y signal enters the TRAP circuit in composite mode, but through operation is performed in all other modes. Also, the picture center frequency is set separately for composite input and Y/C input. (See the AC Characteristics tables.)

• NTSC/PAL switching

NTSC and PAL (DPAL using an external delay line and SPAL) are switched by MODE1.

The built-in TRAP and BPF center frequencies are switched automatically according to the external crystal. The center frequency is stabilized by the APC operation.

The R-Y demodulation detective axis is set internally to 90° during SPAL/DPAL. However, optimally adjust the demodulation phase axis with the HUE adjustment pin.

• Video AGC/ACC circuit

Different AGC characteristics are obtained depending on the APL level of the luminance signal. The gain for the luminance signal is adjusted with the average value. The sync amplitude of the burst signal output is detected and used to adjust the ACC amplifier gain.

• VXO, APC detection

The VXO local oscillation circuit is crystal oscillation circuit. The phases of the input burst signal and the VXO oscillator output are compared in the APC detection block, and the detective output is used to form a PLL loop that controls the VXO oscillation frequency, which means that the need for adjustments is eliminated. In addition, the filter f0 is automatically adjusted, since the BPF and TRAP center frequency is feedback controlled by VXO.

• Crystal oscillator for the XVXO pin connection

A 3.579545MHz crystal vibrator is connected to the XVXO pin during NTSC, and a 4.433619MHz crystal vibrator during PAL. (Use KINSEKI CX-5F crystal vibrator with a load capacity of 16pF, frequency deviation within ±30ppm, and frequency temperature characteristics within ±30ppm.)

• External inputs

Digital input with two thresholds is optimal for multiplexed character output to screens. When one of the RGB inputs is higher than the lower threshold Vth1, all RGB outputs go to black level. When the higher threshold Vth2 is exceeded, the output for only the signal in question goes to white level, while the other outputs remain at black level. Externally connect a pull-down resistor (10kΩ or more).

3) Description of RGB driver block operation

• 2-point γ compensation circuit

In order to support the characteristic of LCD panels, the I/O characteristics are as shown in Fig. 1. The voltage at γ gain change point A can be changed to that shown in Fig. 2 by adjusting the GAMMA1 pin (Pin 59). Also, the voltage at the γ2 gain change point can be changed to that shown in Fig. 3 by adjusting the GAMMA2 pin (Pin 58). The drive for LCD panels can be optimized by adjusting the overall gain with these two gain change points and the RGB-GAIN pin (Pin 57).

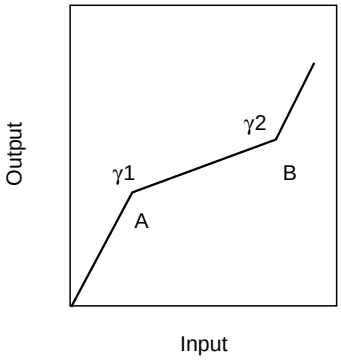


Fig. 1

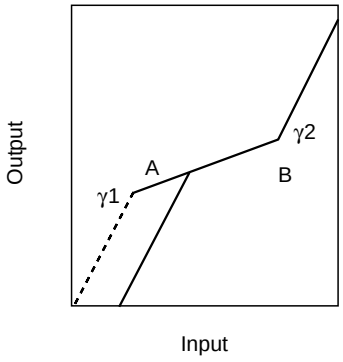


Fig. 2

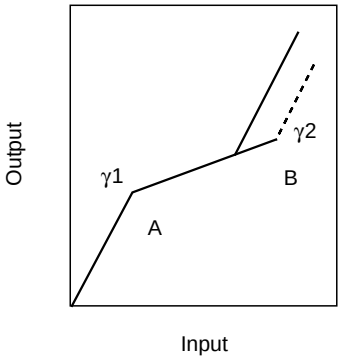
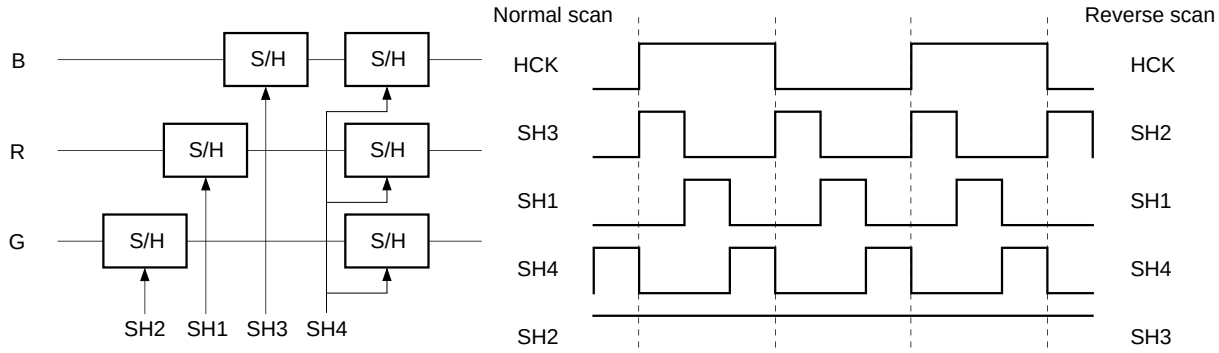


Fig. 3

• Sample-and-hold circuit

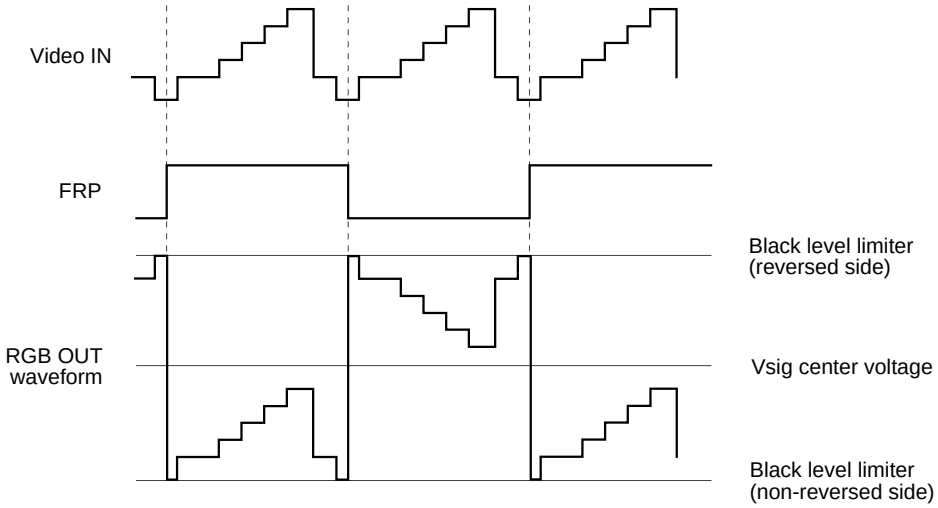
As the LCD panels sample-and-hold RGB signals simultaneously, RGB signal output from CXA1854R must be synchronized to LCD panel drive pulses and sample-and-hold performed. Sample-and-hold is performed by receiving the SH1 to SH4 pulses from the TG block. Since LCD panels perform color coding using an RGB delta arrangement, each horizontal line must be compensated by 1.5 dots. This relationship is reversed during right/left inversion. These timing pulses are generated by the TG block. Accordingly, RGB signals are each sampled-and-held at the optimal timing and output by the RGB driver block.



Example of sample-and-hold circuits and S/H timing

• RGB output

RGB outputs (Pins 39, 41, and 43) are reversed each horizontal line by the FRP pulse supplied from the TG block as shown in the figure below. Feedback is applied so that the center voltage of the output signal matches the reference voltage ($V_{CC}2$ + GND1)/2. In addition, the white level output is clipped by the Vsig center voltage level, and the black level output is clipped by the limiter operation point that is adjusted at the BLKLIM pin (Pin 46).



4) Description of TG block operation

This section describes the main functions of the TG block. (See individual description materials for details.)

- PLL circuit block

  The PLL circuit block contains a phase comparator and frequency division counter circuit in order to accurately align the timing, and performs PLL operation by externally connecting a VCO circuit. The average voltage of the RPD pin (Pin 12) is locked roughly in the center by adjusting it to $V_{DD}/2$. (See the attached Application Circuit for the external circuit diagram. The 1T369 is recommended as the vari-cap diode used in the VCO circuit.)

- SYNC detection circuit

  This circuit separates the input SYNC signal into HSYNC and VSYNC, and recognizes the EVEN and ODD fields and line numbers, etc. This circuit is necessary for the reasons (1) and (2).

  (1) Shifts 1.5 dots each horizontal line for the RGB delta arrangement.

  (2) Field recognition and accurate line number recognition for changing the eliminated lines for each EVEN and ODD field and smoothing the picture during PAL.

  In addition, if the SYNC waveform is not detected for more than a certain interval, the unit shifts automatically to the free running state and the LCD panel is driven by self oscillation.

- Pulse generator block

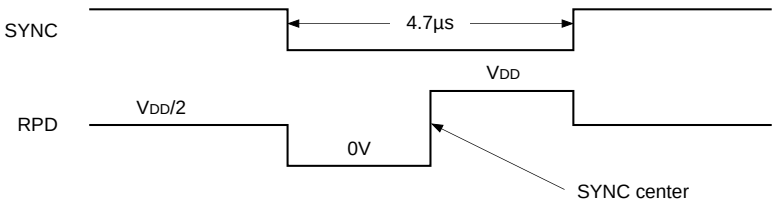
  The pulse generator circuit is synchronized to the previously mentioned SYNC detection circuit and PLL circuit, and generates the pulses necessary to drive the LCD panel. (The main output pulse timings are shown for each mode in a later section.) At the same time, the pulse generator circuit also generates the BGP, BLK and other waveforms for the RGB decoder. Therefore, TG block PLL circuit operation is necessary for RGB decoder functions.

- AC drive during no signal

  HST1, HCK1, HCK2, FRP, VST1, VCK1, VCK2, HD and VD are made to run free so that the LCD panel is AC driven even when there is no composite sync from the SYNC pin. During this time, the HSYNC separation circuit stops and the PLL counter is made to run free. In addition, the reference pulse for generates VD and VST, and the auxiliary V counter creates the reference pulse for generates VD and VST. The VSYNC separation circuit is also stopped and The period of the V counter is designed to be 269H for NTSC and 321H for PAL. When there is no VSYNC during 269H or 321H, the free running state is assumed. In addition, RPD is kept at high impedance in order to prevent the AFC circuit from producing a phase error due to phase comparison when there is no signal.

- AFC circuit (702/1050fh generation)

  A fully synchronized AFC circuit is built in. PLL error signal is generated at the following timing. The phase comparison output of the entire bottom of SYNC and the internal H counter becomes RPD. RPD output is converted to DC error with the lag-lead filter, and then it changes the vari-cap diode capacitance and the oscillation frequency is stabilized at 702fh in the LCX005BK/BKB and 1050fh in the LCX009AK/AKB.



5) Description of TG block mode settings

• SLCK: Selects the driven LCD panel.

L	Selects the LCX009
H	Selects the LCX005

Note) The VCO frequency varies depending on the used panel.

VCO center frequency

LCX005 (702fh)

NTSC	11.06MHz
PAL	10.97MHz

LCX009 (1050fh)

NTSC	16.52MHz
PAL	16.41MHz

The external VCO circuit diagram is shown in the Application Circuit.

Recommended value: L value LCX005: 10µH, LCX009: 4.7µH

• RGT: Switches the horizontal scan direction.

H	Normal scan mode
L	Reverse scan mode

The HST1, HCK1 and HCK2 timing are switched by the RGT selection. The timing of the internal sample-and-hold pulse is also switched at the same time. Connect the panel RGT pin directly, as it does not support output.

• MODE1/MODE2: Sets the type of video signal input.

MODE1

H	NTSC
M	D-PAL
L	SPAL

MODE2

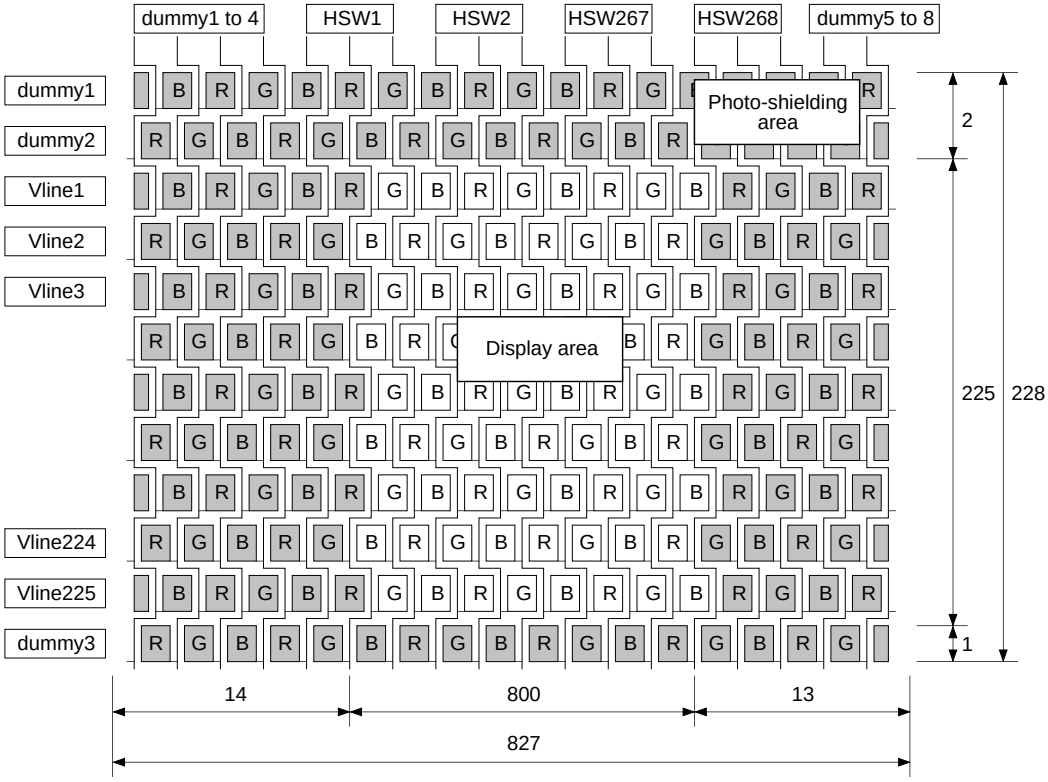
H	Composite input
M	Y/color difference input
L	Y/C input

Signal input connections for each mode are noted in the RGB decoder block.

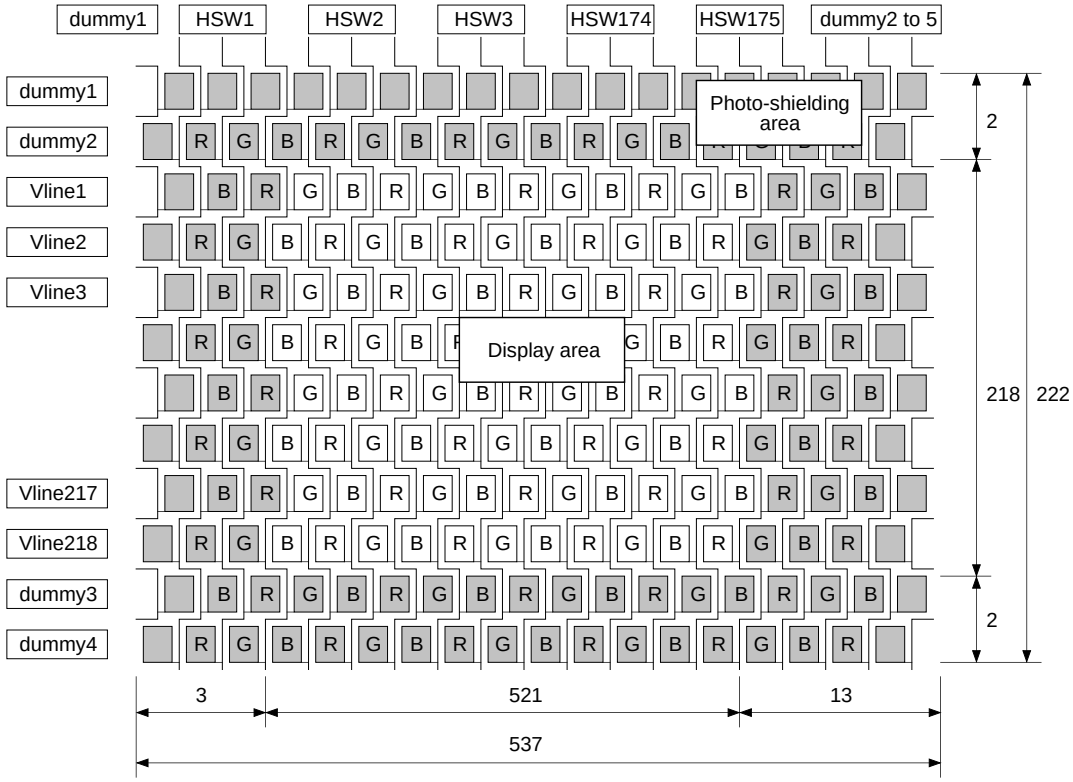
LCX009AK/AKB and LCX005BK/BKB Color Coding Diagram

The delta arrangement is used for the color coding in the LCD panels with which this IC is compatible. Note that the shaded region within the diagram is not displayed.

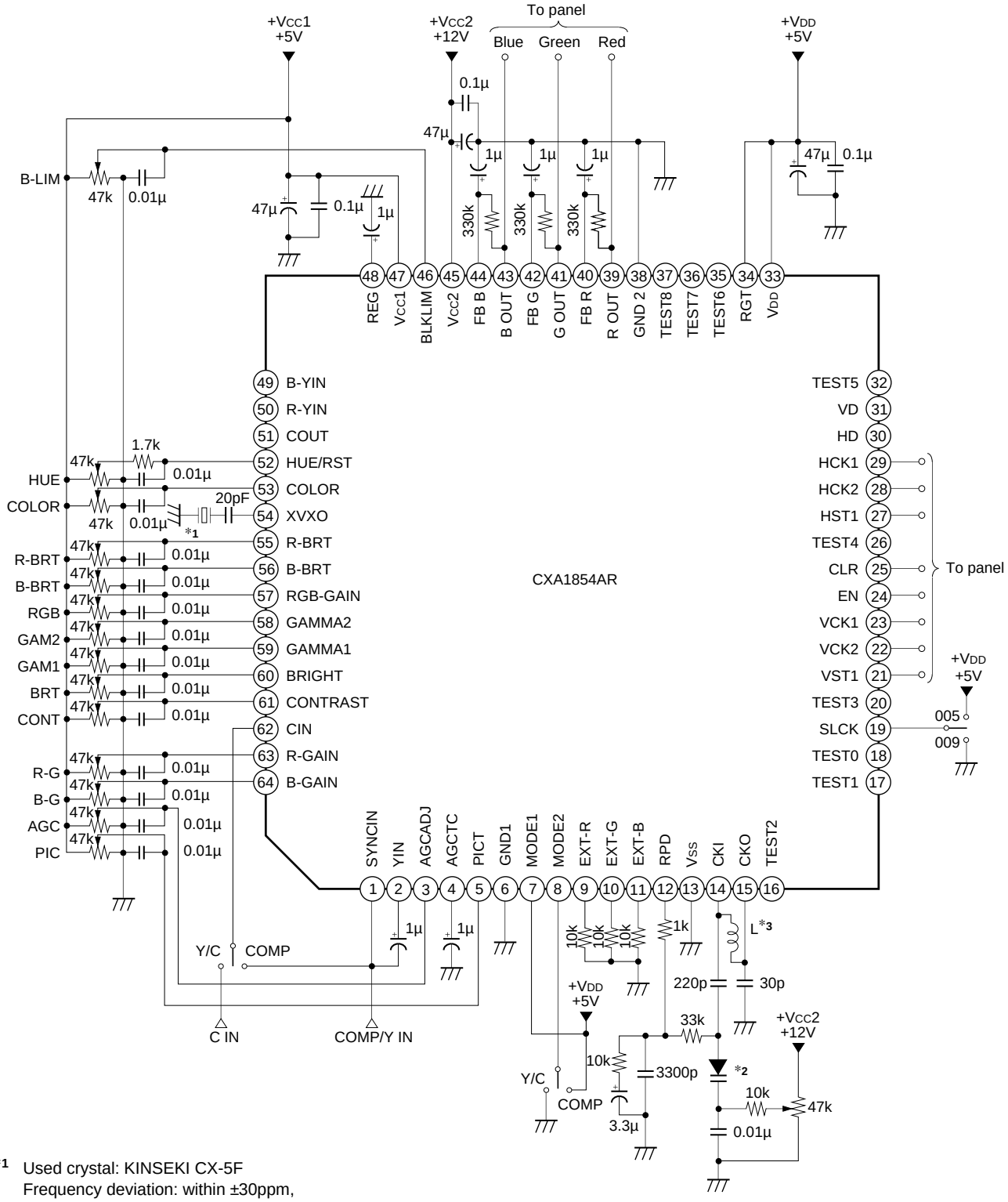
LCX009AK/AKB pixel arrangement



LCX005BK/BKB pixel arrangement



Application Circuit – NTSC (COMP and Y/C input)



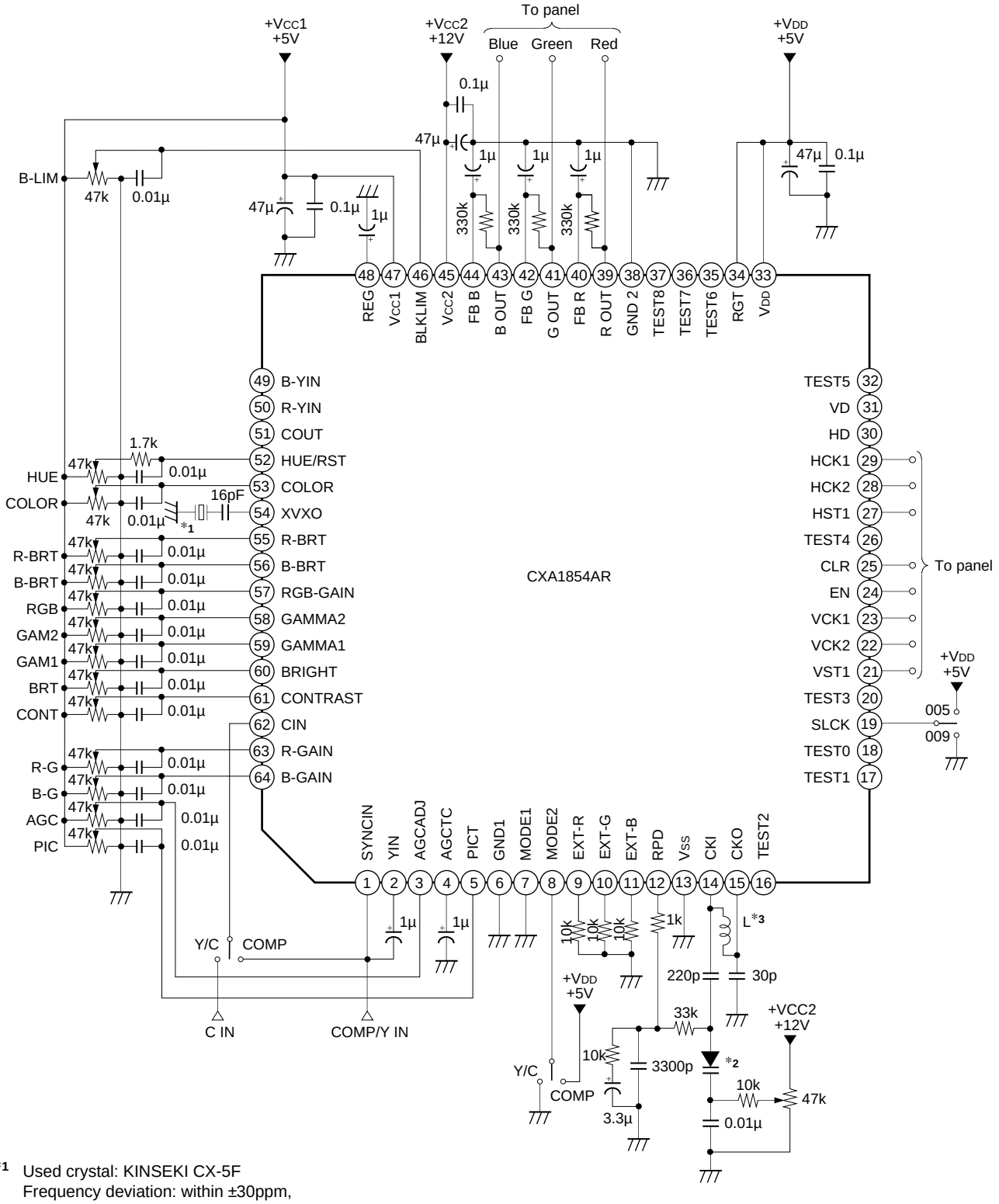
*1 Used crystal: KINSEKI CX-5F
Frequency deviation: within ±30ppm,
frequency temperature characteristics: within ±30ppm
3.579545MHz, load capacity: 16pF

*2 Vari-cap diode: 1T369 (SONY)

*3 L value: 10µH when using the LCX005
4.7µH when using the LCX009

Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Application Circuit – PAL (COMP and Y/C input)



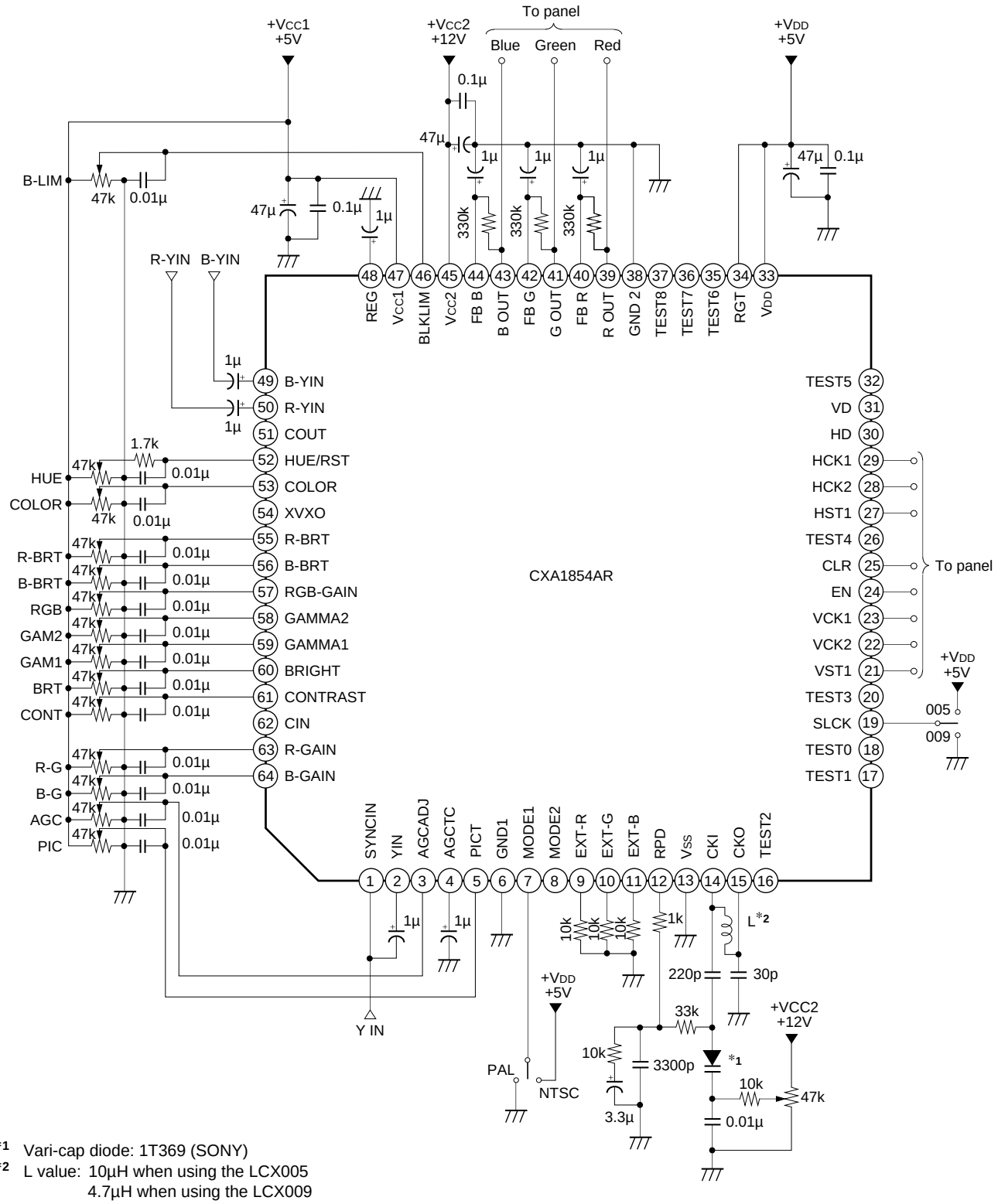
*1 Used crystal: KINSEKI CX-5F
Frequency deviation: within ±30ppm,
frequency temperature characteristics: within ±30ppm
4.433619MHz, load capacity: 16pF

*2 Vari-cap diode: 1T369 (SONY)

*3 L value: 10µH when using the LCX005
4.7µH when using the LCX009

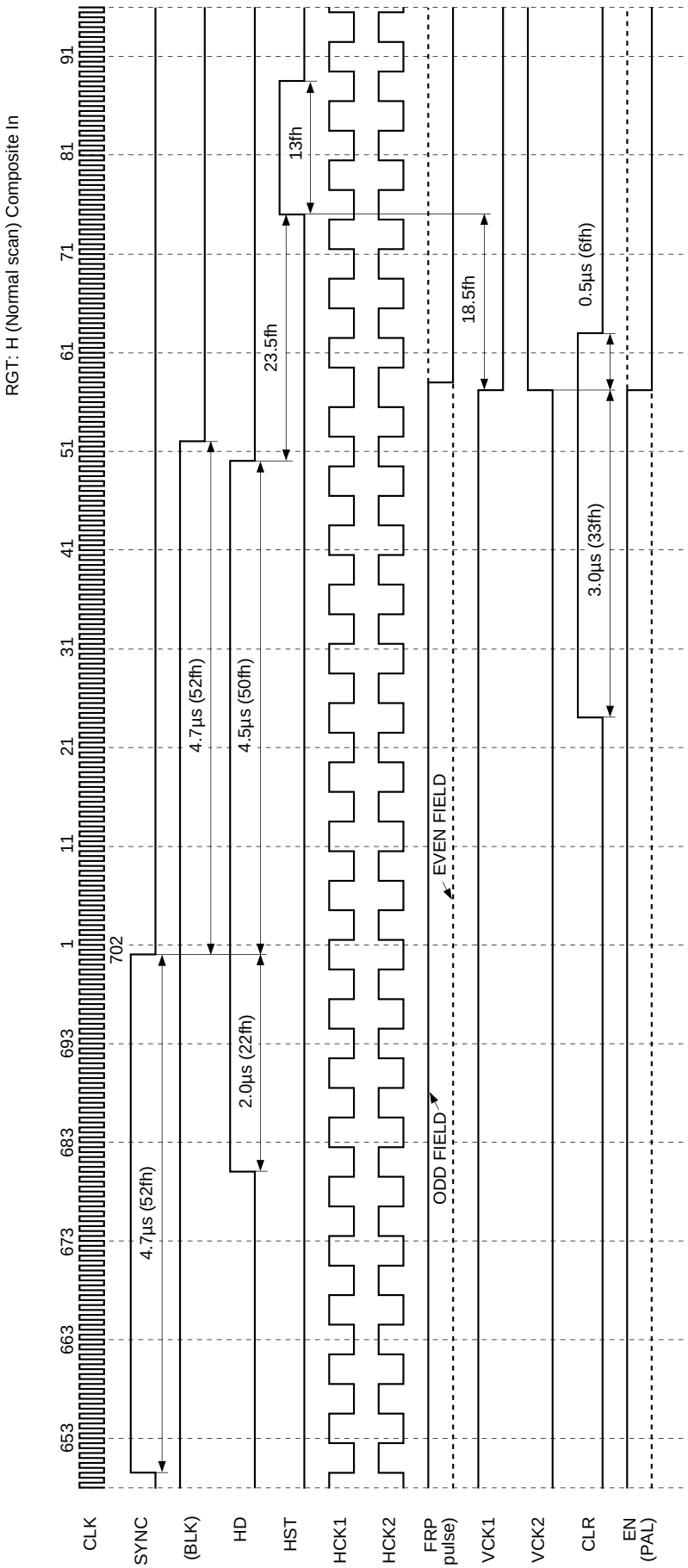
Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Application Circuit – Y/color difference input (NTSC/PAL)



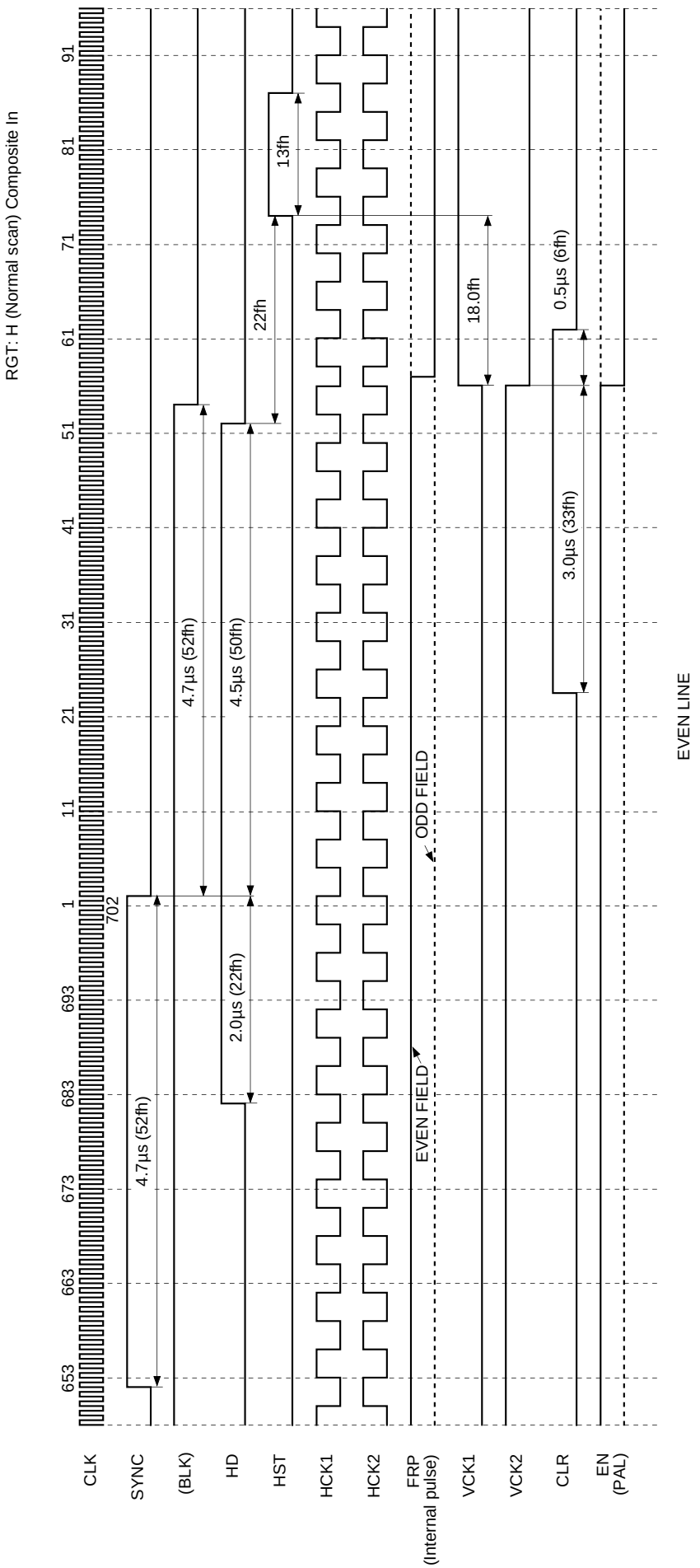
*1 Vari-cap diode: 1T369 (SONY)
*2 L value: 10µH when using the LCX005
4.7µH when using the LCX009

LCX005 Horizontal Direction Timing Chart (NTSC, PAL)



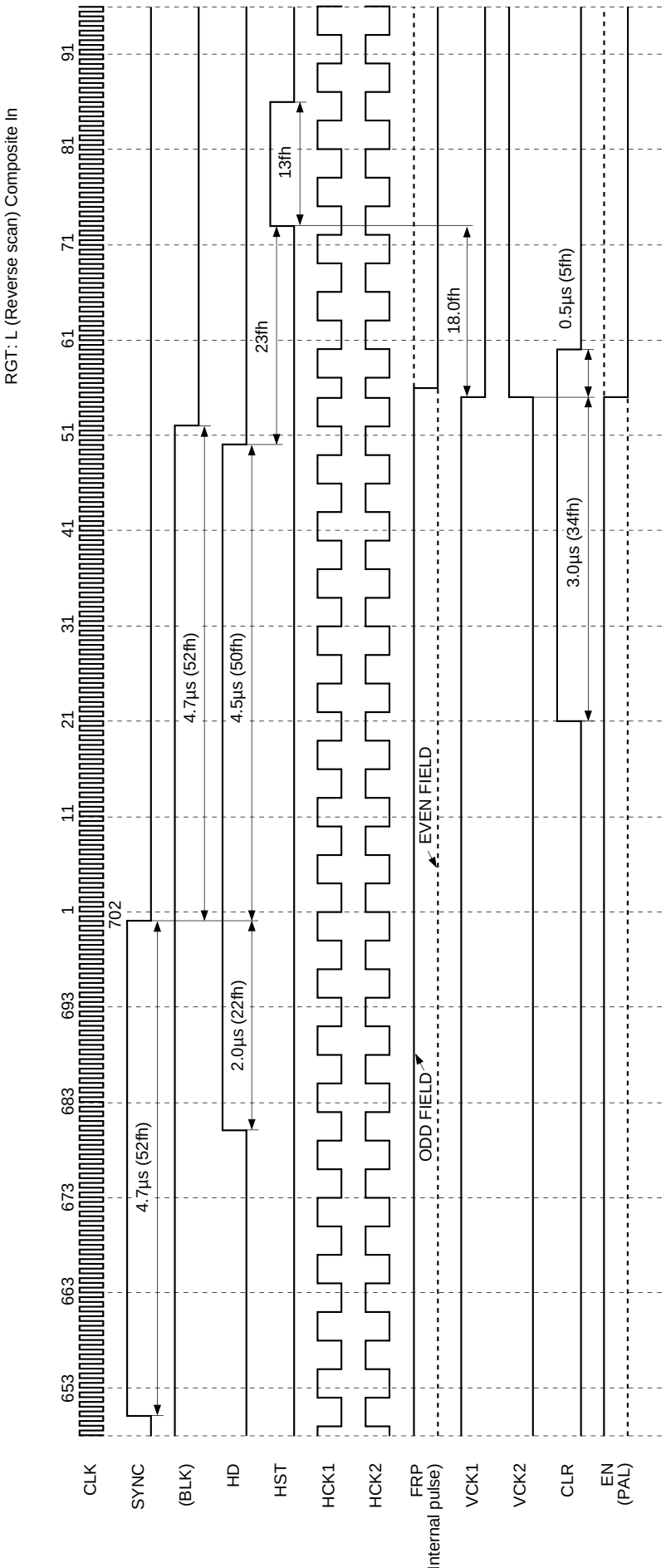
Note) During Y/C input, the HST timing is delayed 6fh from the above timing.
The third row of the timing chart "BLK" is a pulse indicated as a reference and is not a pulse output from pins.
FRP polarity is not specified.

LCX005 Horizontal Direction Timing Chart (NTSC, PAL)



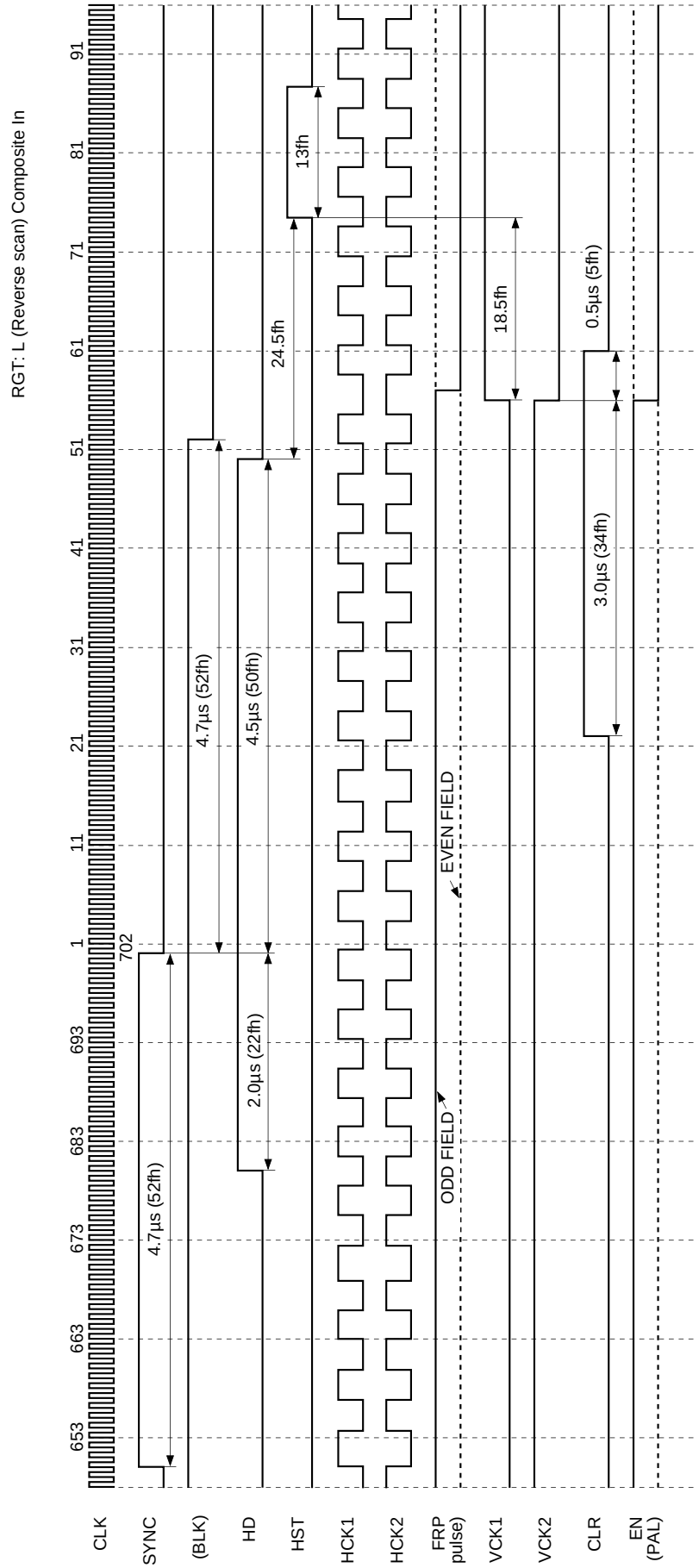
Note) During Y/C input, the HST timing is delayed 6fh from the above timing.
The third row of the timing chart "BLK" is a pulse indicated as a reference and is not a pulse output from pins.
FRP polarity is not specified.

LCX005 Horizontal Direction Timing Chart (NTSC, PAL)



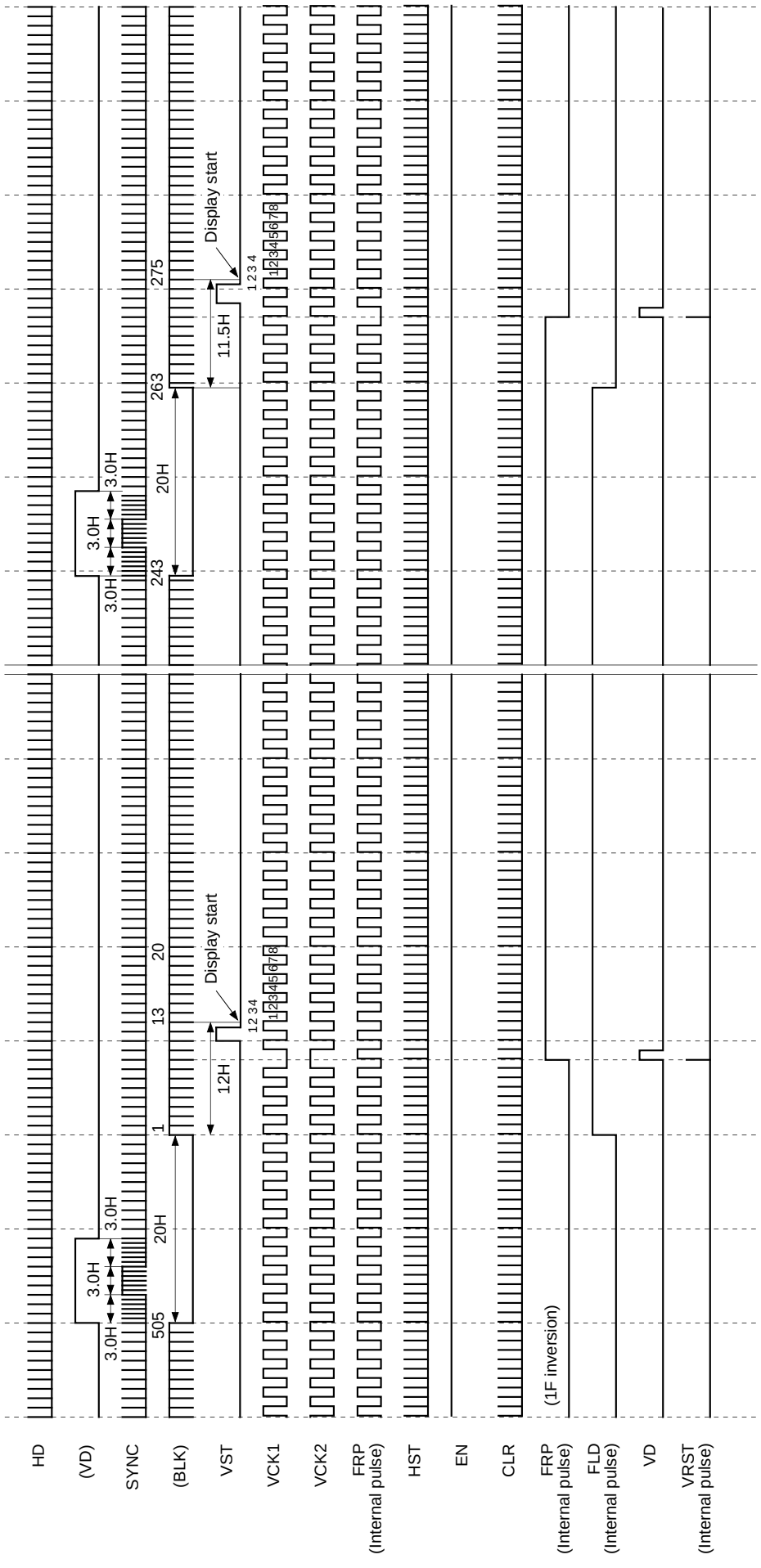
Note) During Y/C input, the HST timing is delayed 6fh from the above timing.
The third row of the timing chart "BLK" is a pulse indicated as a reference and is not a pulse output from pins.
FRP polarity is not specified.

LCX005 Horizontal Direction Timing Chart (NTSC, PAL)



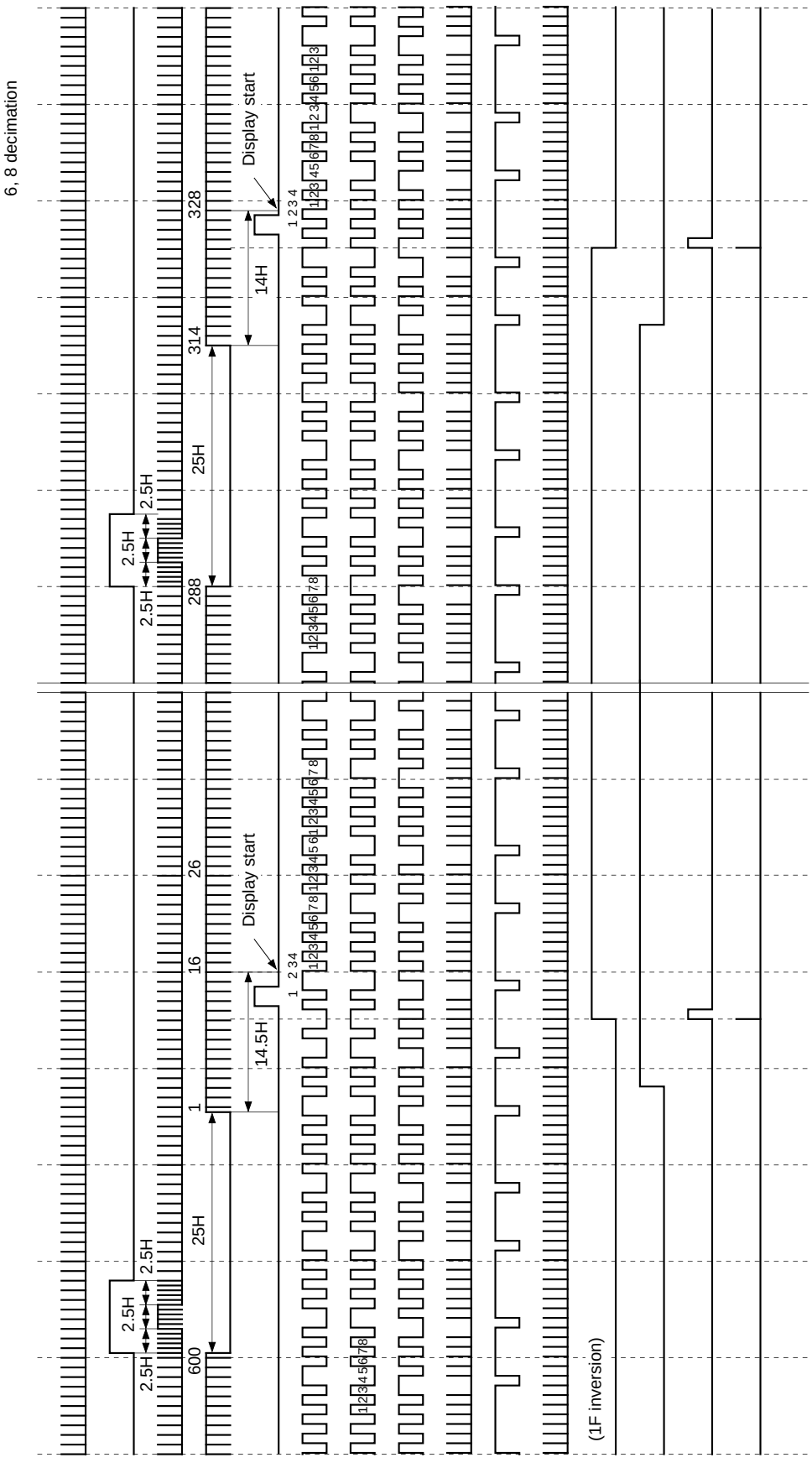
Note) During Y/C input, the HST timing is delayed 6fh from the above timing.
The third row of the timing chart "BLK" is a pulse indicated as a reference and is not a pulse output from pins.
FRP polarity is not specified.

LCX005 Vertical Direction Timing Chart (NTSC)



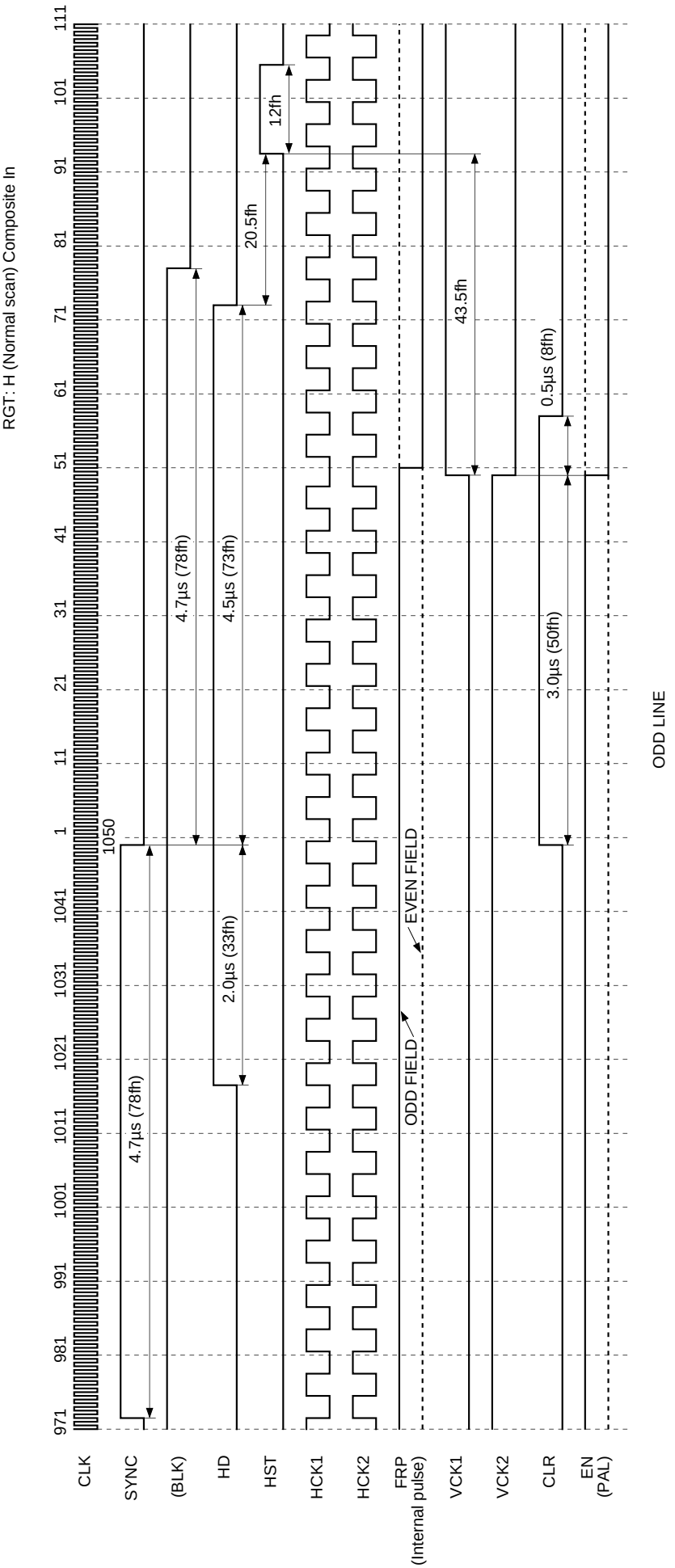
Note) The second and fourth rows of the timing chart "VD" and "BLK" are pulses indicated as a reference and are not pulses output from pins.

LCX005 Vertical Direction Timing Chart (PAL)



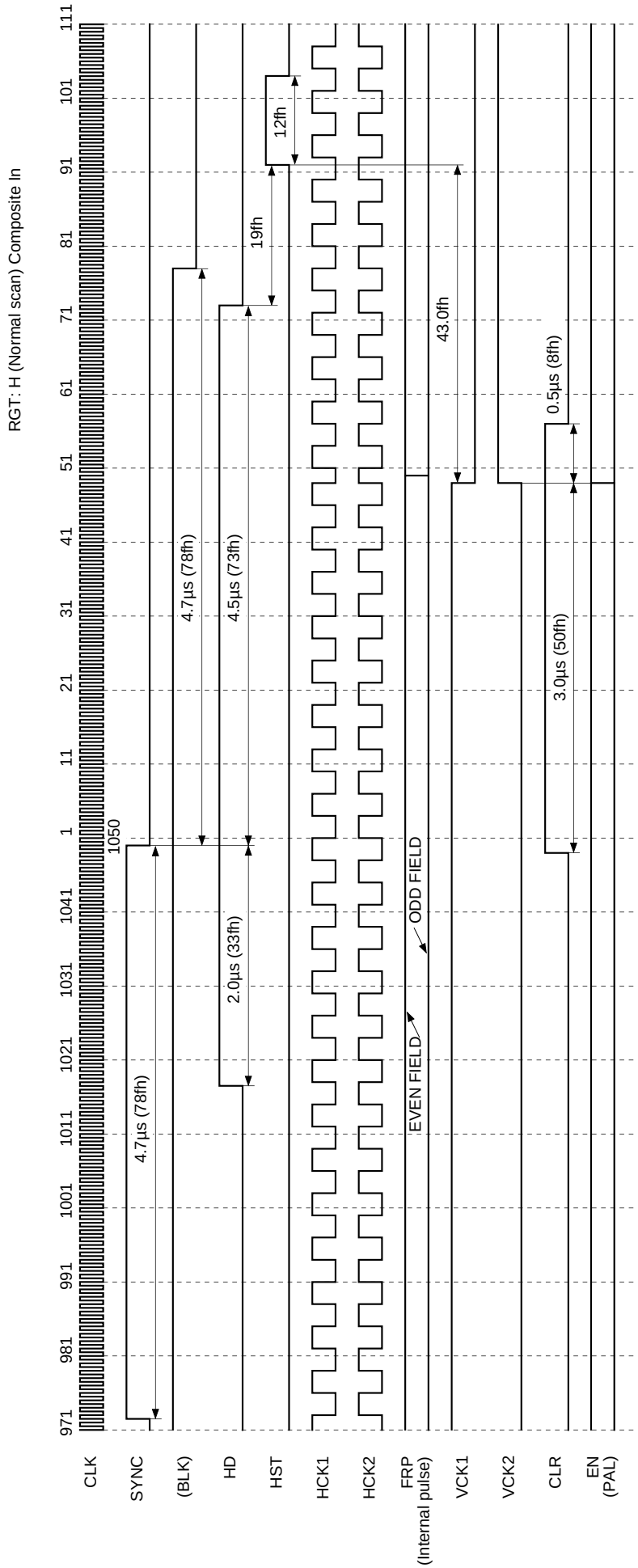
Note) The second and fourth rows of the timing chart "VD" and "BLK" are pulses indicated as a reference and are not pulses output from pins.

LCX009 Horizontal Direction Timing Chart (NTSC, PAL)



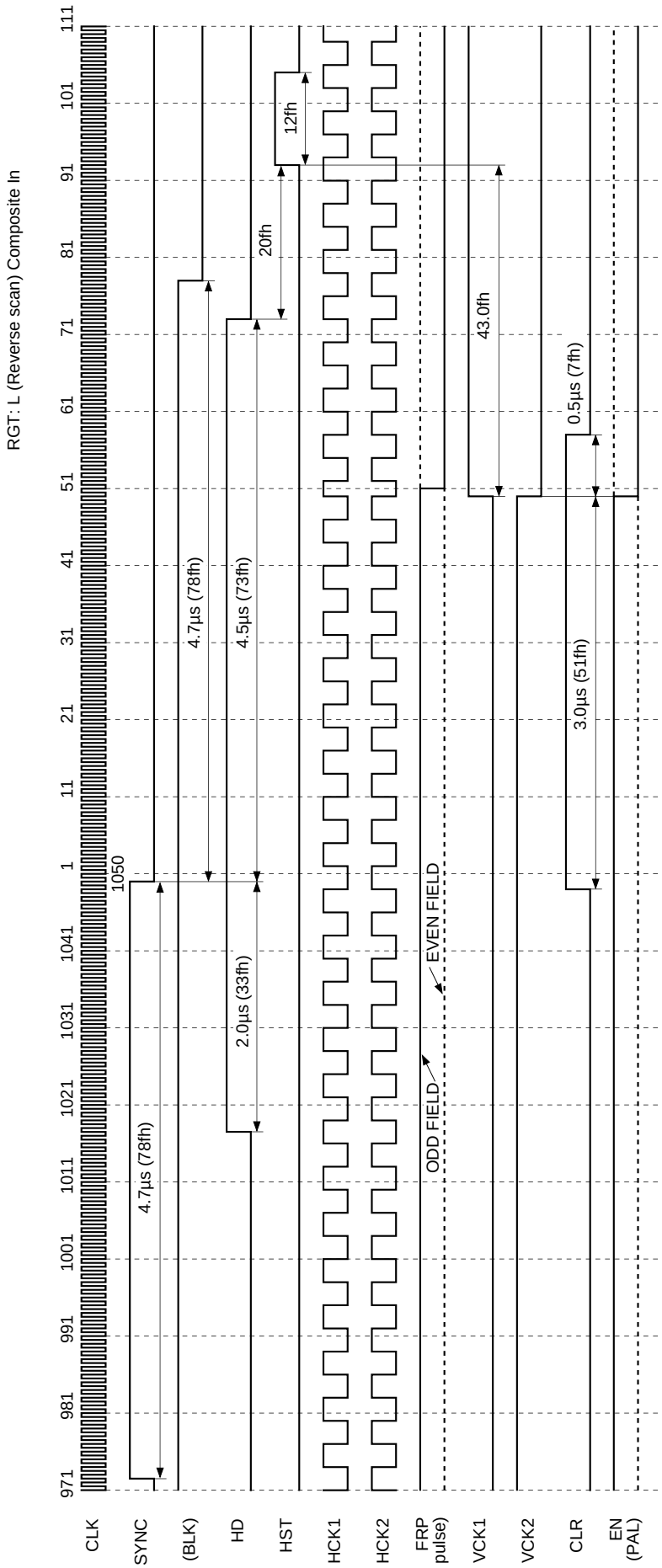
Note) During Y/C input, the HST timing is delayed 6fh from the above timing.
The third row of the timing chart "BLK" is a pulse indicated as a reference and is not a pulse output from pins.
FRP polarity is not specified.

LCX009 Horizontal Direction Timing Chart (NTSC, PAL)



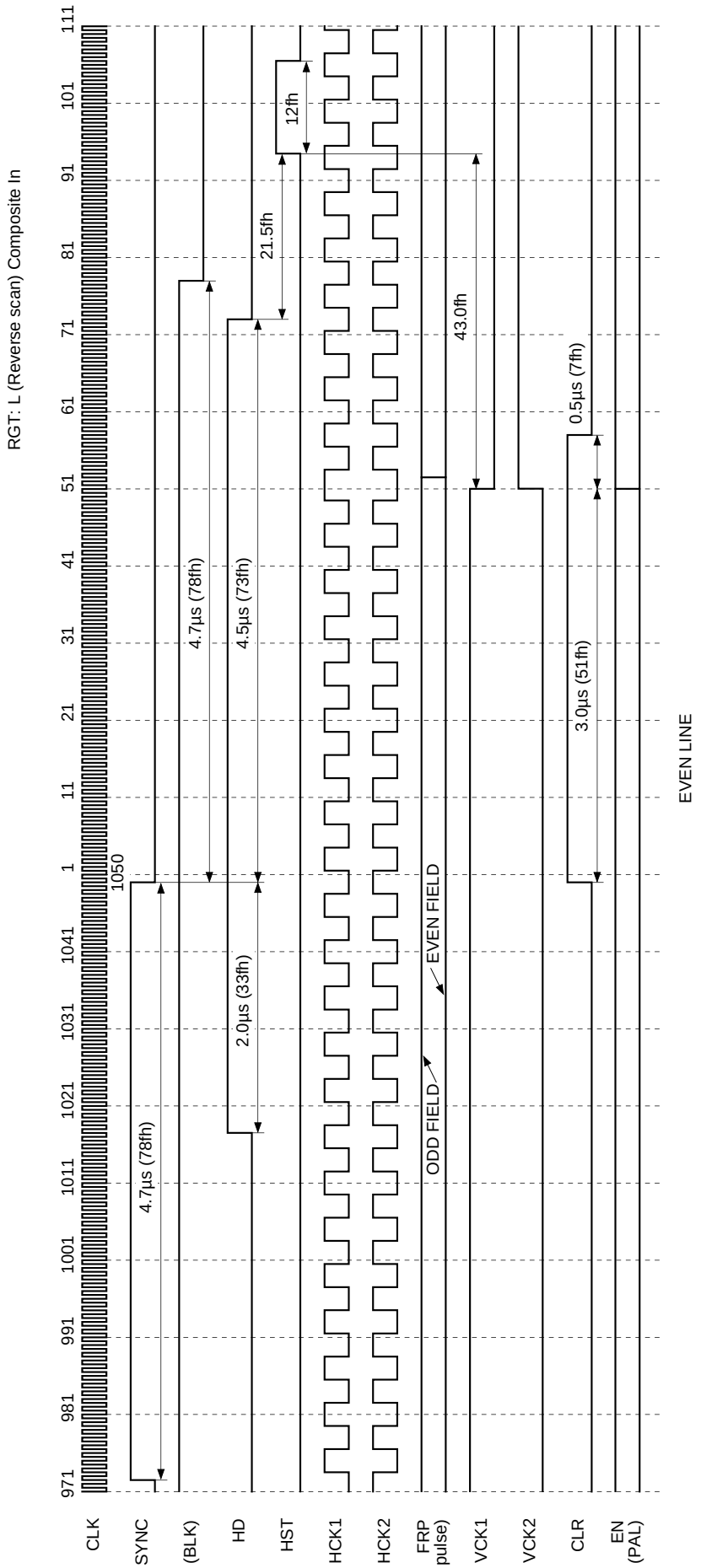
Note) During Y/C input, the HST timing is delayed 6fh from the above timing.
The third row of the timing chart "BLK" is a pulse indicated as a reference and is not a pulse output from pins.
FRP polarity is not specified.

LCX009 Horizontal Direction Timing Chart (NTSC, PAL)



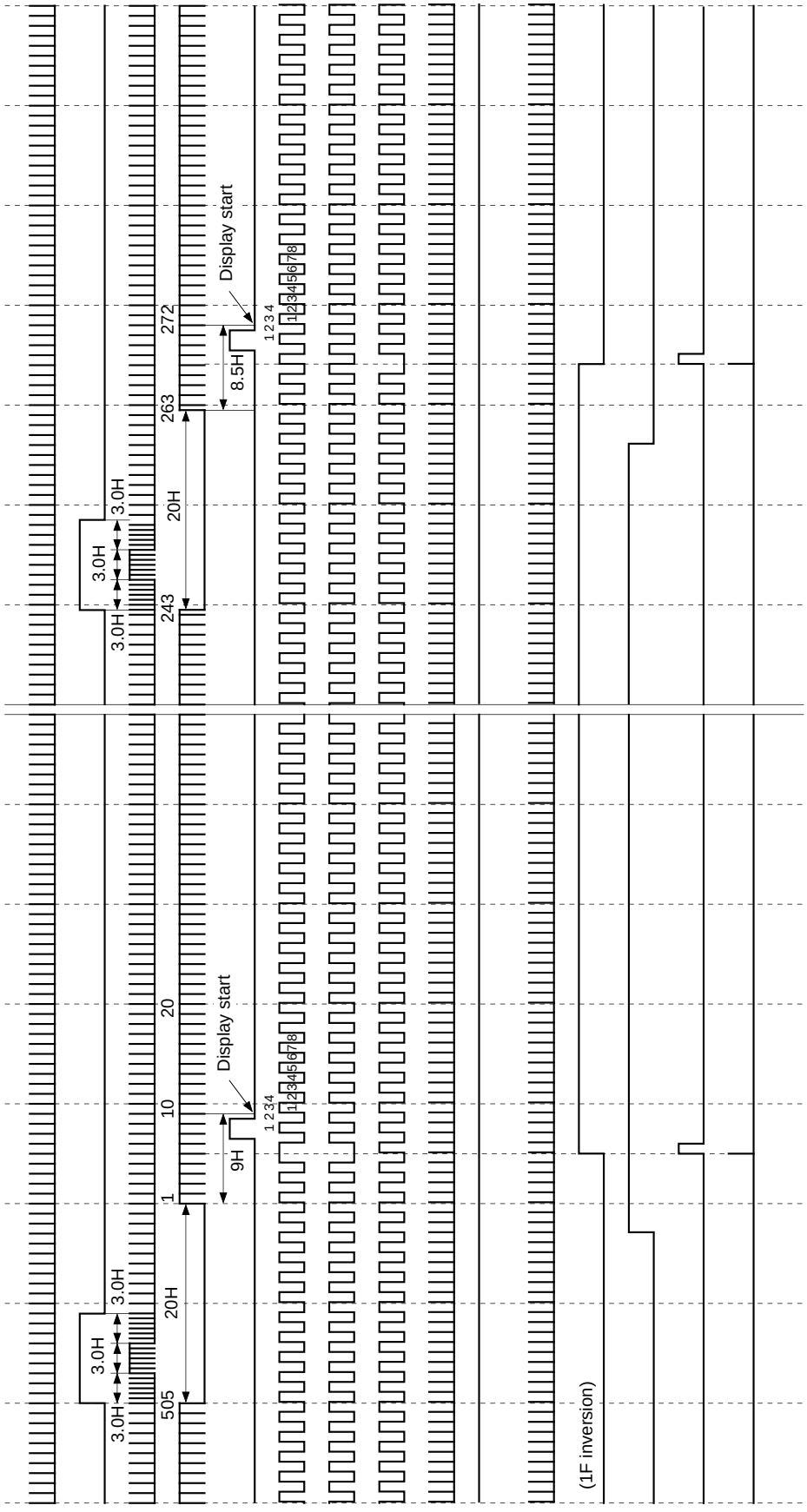
Note) During Y/C input, the HST timing is delayed 6fh from the above timing.
The third row of the timing chart "BLK" is a pulse indicated as a reference and is not a pulse output from pins.
FRP polarity is not specified.

LCX009 Horizontal Direction Timing Chart (NTSC, PAL)



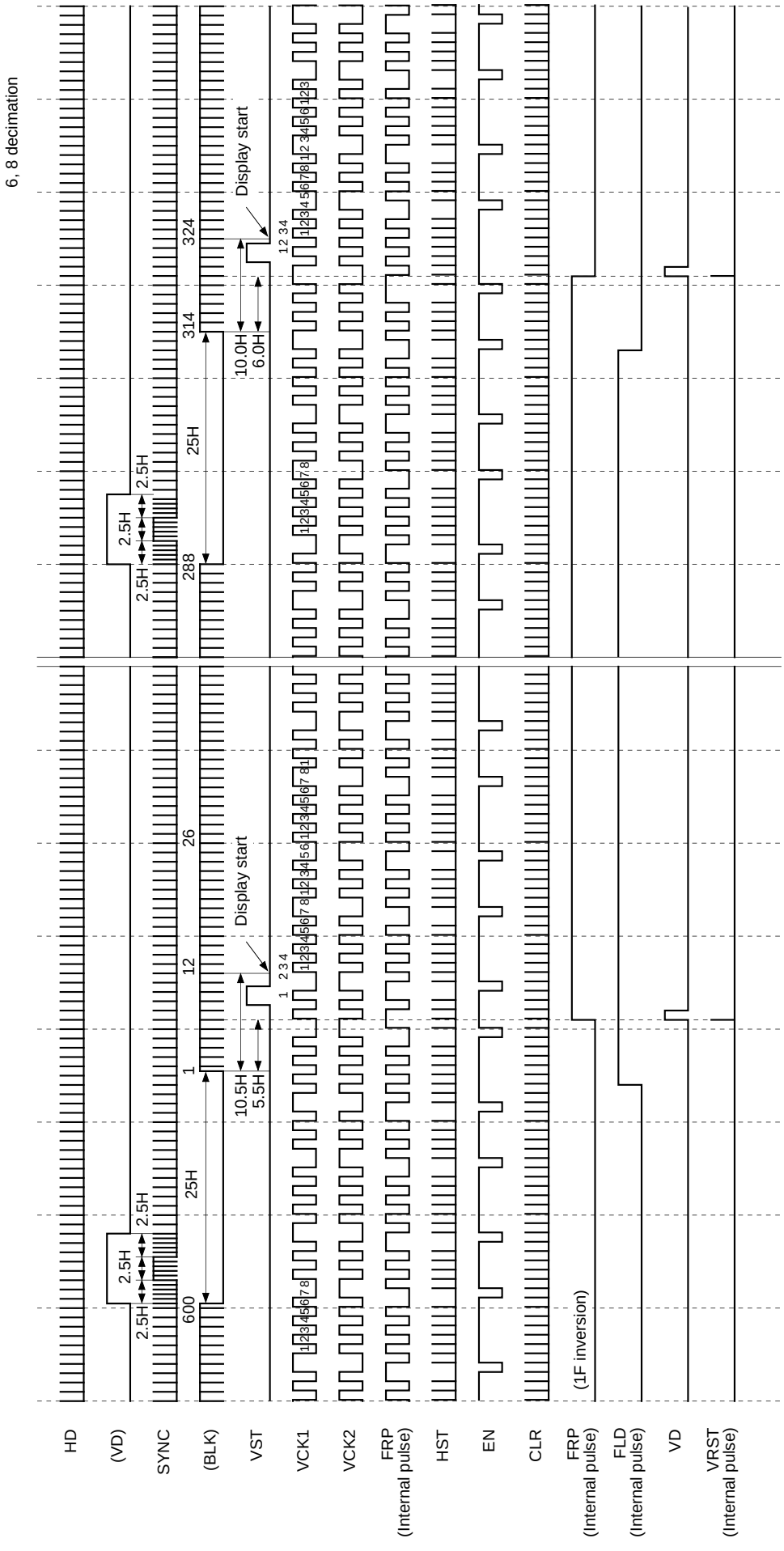
Note) During Y/C input, the HST timing is delayed 6fh from the above timing.
The third row of the timing chart "BLK" is a pulse indicated as a reference and is not a pulse output from pins.
FRP polarity is not specified.

LCX009 Vertical Direction Timing Chart (NTSC)



Note) The second and fourth rows of the timing chart "VD" and "BLK" are pulses indicated as a reference and are not pulses output from pins.

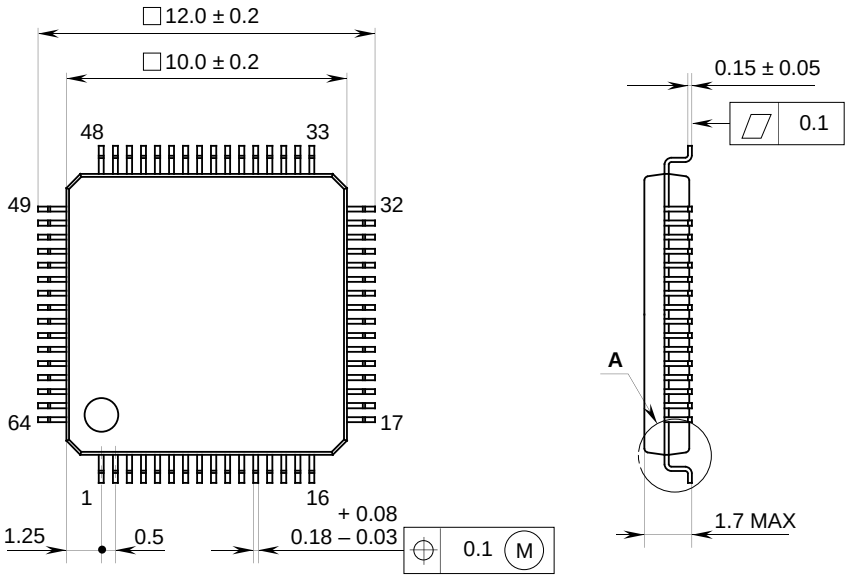
LCX009 Vertical Direction Timing Chart (PAL)

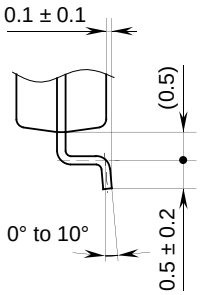


Note) The second and fourth rows of the timing chart "VD" and "BLK" are pulses indicated as a reference and are not pulses output from pins.

Package Outline Unit: mm

64PIN LQFP (PLASTIC)





DETAIL **A**

SONY CODE	LQFP-64P-L061
EIAJ CODE	LQFP064-P-1010-AY
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	0.3g