Ordering number: EN 5228A

Thick Film Hybrid IC

STK672-050

Microstep Operation-Supported 4-Phase Stepping Motor Driver (I_O = 3.0A)

Overview

The STK672-050 is a unipolar constant-current chopper-type externally-excited 4-phase stepping motor driver hybrid IC which uses MOSFET power devices. It has a microstep operation-supported 4-phase distributed controller built-in to realize a high torque, low vibration, low noise stepping motor driver using a simple control circuit.

Applications

- Printer, copier, and X-Y plotter stepping motor drivers

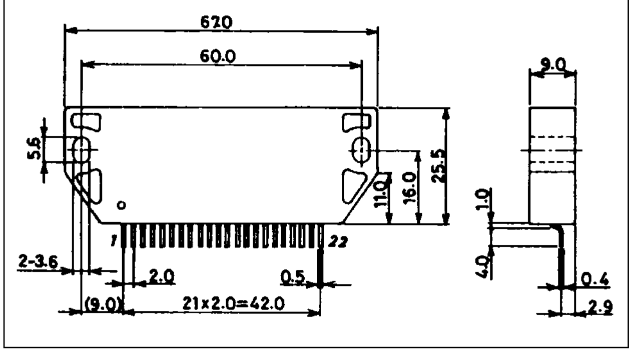
Features

- Microstep sine-wave driver operation using only an external clock input (0.2Ω current detection resistor built-in)
- Microstep drive using only an external reference voltage setting resistor
- 2, 1-2, W1-2, 2W1-2, 4W1-2 phase excitation selectable using external pins
- Selectable vector locus (perfect circle mode, inside 1 mode, outside 2 modes) to match motor characteristics in microstep drive state
- Phase hold function during excitation switching
- Schmitt trigger inputs with built-in pull-up resistor (20kΩ)
- Monitor output pin enabling real-time confirmation of IC excitation
- The CLK and RETURN inputs provide an internal noise elimination circuit as well as CMOS Schmitt circuit to prevent malfunction due to impulse noise.
- 4-phase distribution switch timing selected externally to either CLK rising-edge only detection mode or both rising-edge and falling-edge detection mode
- ENABLE pin for excitation current cutoff, thereby reducing system current drain when driver is stopped

Package Dimensions

unit: mm

4164



Series Organization

The following devices form a series with differing output capacity.

Type No.	Output current (A)
STK672-040	1.5
STK672-050	3.0

Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage 1	$V_{CC}1$ max	No signal	52	V
Maximum supply voltage 2	$V_{CC}2$ max	No signal	–0.3 to +7.0	V
Input voltage	V_{IN} max	Logic input block	–0.3 to +7.0	V
Phase output current	I_{OH} max	One 0.5s pulse, $V_{CC}1$ applied, Load/phase: R = 5Ω, L = 10mH	4.0	A
Repetitive avalanche handling capability	Ear max		38	mJ
Maximum output dissipation	Pd max	θc-a = 0	25	W
Operating substrate temperature	Tc max		105	°C
Junction temperature	Tj max		150	°C
Storage temperature	Tstg		–40 to +125	°C

Allowable Operating Ranges at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage 1	$V_{CC}1$	With signal	10 to 45	V
Supply voltage 2	$V_{CC}2$	With signal	5.0 ± 5%	V
Input voltage	V_{IH}		0 to $V_{CC}2$	V
Phase driver withstand voltage	V_{DSS}	Tr1, 2, 3, 4 (A, $\overline{A}$, B, $\overline{B}$ outputs)	100 (min)	V
Phase current	I_{OH} max	50% duty	3.0 (max)	A

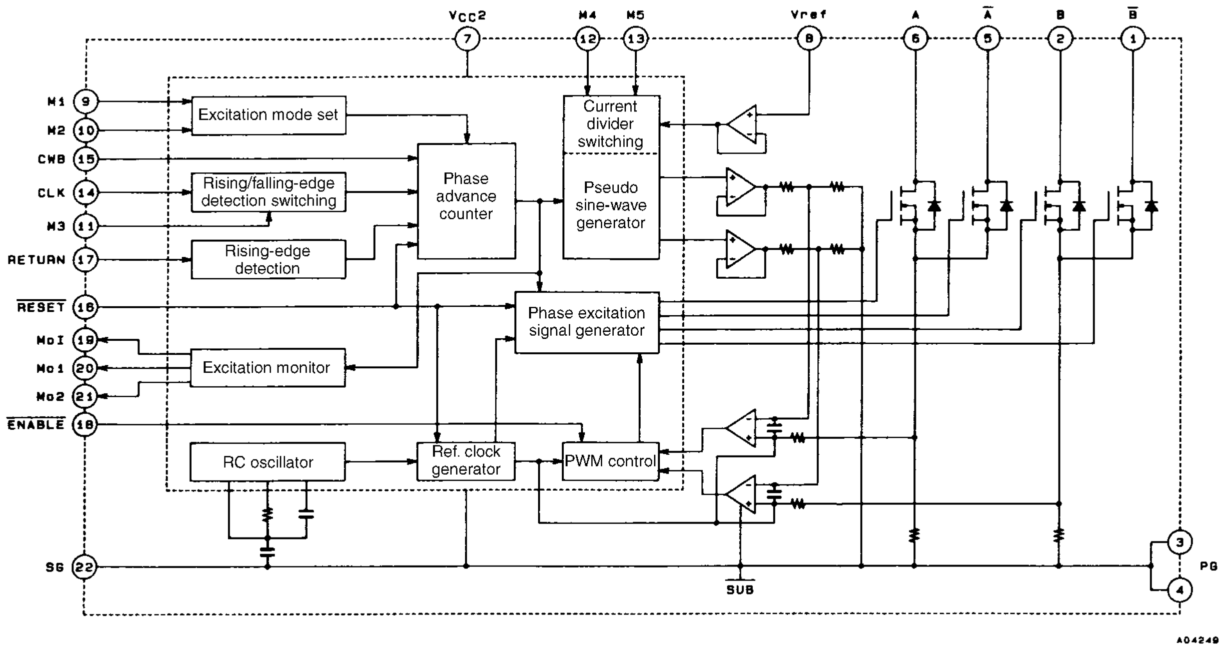
Electrical Characteristics at Tc = 25°C, $V_{CC}1$ = 24V, $V_{CC}2$ = 5V

Parameter	Symbol	Conditions	min	typ	max	Unit
Control supply current	I_{CC}	Pin 7 input, ENABLE = low	–	4.5	15	mA
Output saturation voltage	Vsat	R_L = 7.5Ω (I = 3A)	–	1.4	2.6	V
Average output current	Io ave	Vref = 0.6V, Load/phase: R = 3.5Ω, L = 3.8mH	0.45	0.50	0.55	A
FET diode forward voltage	Vdf	If = 1.0A	–	1.2	1.8	V
[Control inputs]						
Input voltage	V_{IH}	Excluding Vref pin	4.0	–	–	V
	V_{IL}	Excluding Vref pin	–	–	1.0	V
Input current	I_{IH}	Excluding Vref pin	0	1	10	µA
	I_{IL}	Excluding Vref pin	125	250	510	µA
[Vref input]						
Input voltage	V_I	Pin 8	0	–	2.5	V
Input current	I_I	Pin 8	–	1	–	µA
[Control outputs]						
Output voltage	V_{OH}	I = –3mA (MoI, Mo1, Mo2 pins)	2.4	–	–	V
	V_{OL}	I = +3mA (MoI, Mo1, Mo2 pins)	–	–	0.4	V
PWM frequency	fc		37	47	57	kHz
[Current division ratio (A/B)]						
2W1-2, W1-2, 1-2	Vref	θ = 1/8			100	%
2W1-2, W1-2	Vref	θ = 2/8			92	%
2W1-2	Vref	θ = 3/8			83	%
2W1-2, W1-2, 1-2	Vref	θ = 4/8			71	%

2W1-2	Vref	θ = 5/8	55	%
2W1-2, W1-2	Vref	θ = 6/8	40	%
2W1-2	Vref	θ = 7/8	20	%
2	Vref		100	%

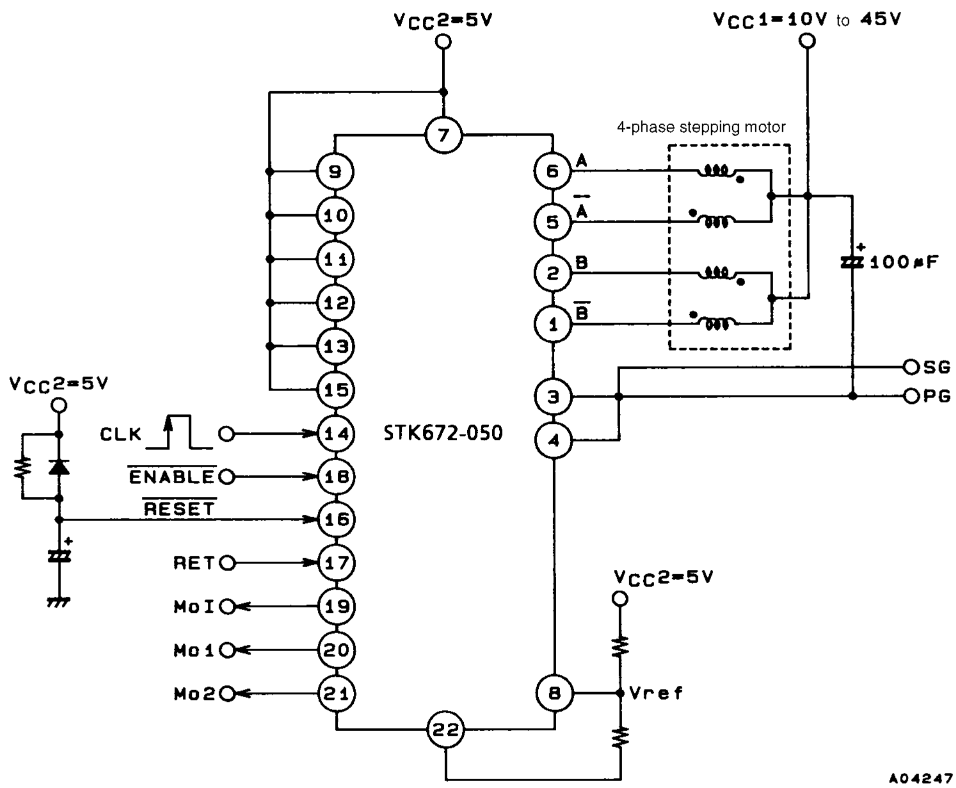
Note: All tests are made using a constant-voltage supply.
The current division ratio shows the design value.

Equivalent Block Diagram



Sample Application Circuit

2W1-2 phase excitation (microstep operation)



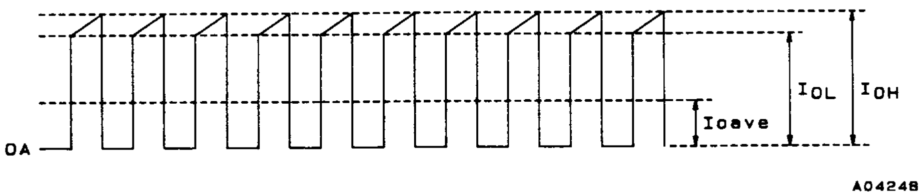
Motor Current Calculation

The motor current I_{OH} is determined by the reference voltage on pin 8 (Vref). The relationship between I_{OH} and Vref is given by the following equation.

$$I_{OH} = \frac{1}{3} \times Vref / Rs$$

where Rs is the built-in current detection resistance (0.2Ω ± 3%).

The motor current ranges from the current due to the frequency duty set by the oscillator (0.05 to 0.1A) to the allowable operating range maximum of I_{OH} = 3.0A.



Motor current waveform

Function Tables

M1	M2	M3	Excitation	Phase switching CLK edge timing
0	0	0	Phase 1-2	Rising and falling edge
0	1	0	Phase 2W1-2	
1	0	0	Phase W1-2	
1	1	0	Phase 4W1-2	
0	0	1	Phase 2	Rising edge only
0	1	1	Phase W1-2	
1	0	1	Phase 1-2	
1	1	1	Phase 2W1-2	

CWB	Direction
0	Forward
1	Reverse

Input	Active level
$\overline{\text{ENABLE}}$	Low
$\overline{\text{RESET}}$	Low

Mo1	Mo2	Output
0	0	$\overline{A}$
0	1	B
1	0	A
1	1	$\overline{B}$

Design material

1. Explanation of input pins

Pin No.	Name	Function	Pin format
14	CLK	Phase switching clock	CMOS Schmitt configuration with pull-up resistor
15	CWB	Setting of rotation direction (CW/CCW)	CMOS Schmitt configuration with pull-up resistor
17	RETURN	Phase origin forced return	CMOS Schmitt configuration with pull-up resistor
18	$\overline{\text{ENABLE}}$	Output cut-off	CMOS Schmitt configuration with pull-up resistor
9, 10, 11	M1, M2, M3	Setting of excitation mode	CMOS Schmitt configuration with pull-up resistor
12, 13	M4, M5	Setting of vector locus	CMOS Schmitt configuration with pull-up resistor
16	$\overline{\text{RESET}}$	System reset	CMOS Schmitt configuration with pull-up resistor
8	Vref	Setting of current value	CMOS Schmitt configuration with pull-up resistor

2. Functions and timing of input signals

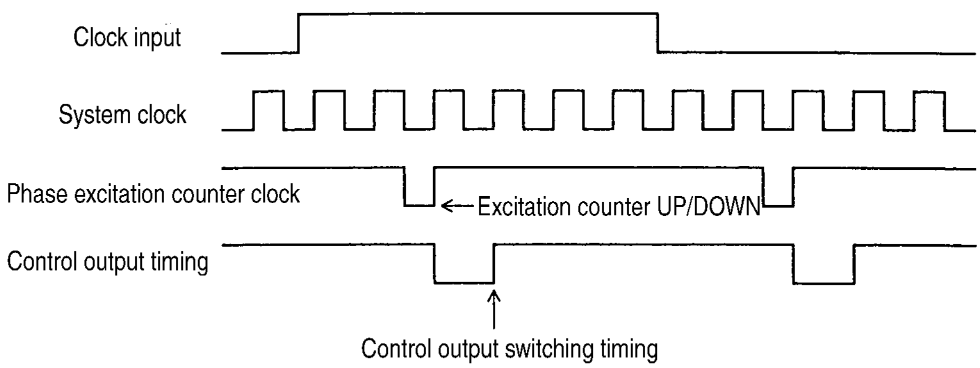
2-1. CLK (Phase switching clock)

1. Input frequency range ■DC to 50 kHz
2. Minimum pulse width ■10 µs
3. Duty ■40 to 60%
4. Pin format ■CMOS Schmitt configuration containing pull-up resistor (20 kΩ typical value)
5. Noise eliminating circuit with multiple stages is contained.
6. Functions

   a. When the signal M3 is set to 1 or it is opened.
   The excitation phase moves at each step at the rising edge of the clock.

   b. When the signal M3 is set to 0.
   The excitation phase moves at each step at the rising and falling edges of the clock.

Clock input fetching timing (M3 = 0)



2-2. CWB (Setting of rotation direction)

1. Pin format ■CMOS Schmitt configuration containing pull-up resistor (20kΩ, typical value)
2. Function

   a. When the signal CWB is set to 1.
   It rotates clockwise.

   b. When the signal CWB is set to 0.
   It rotates counterclockwise.

3. Note ■When the signal M3 is set to 0, the CWB input signal must not be changed at the rising edge and falling edge of the clock input for the period of 5 µs.

2-3. RETURN (It forcibly returns the phase to the origin of current excitation phase.)

1. Pin format ■CMOS Schmitt configuration containing pull-up resistor (20kΩ, typical value)
2. Noise eliminating circuit is contained.
3. Function ■Forces to moves to the origin of current excitation phase by setting the RETURN signal to high state.

2-4. $\overline{\text{ENABLE}}$(ON/OFF control of excitation drive output A, $\overline{\text{A}}$, B, and $\overline{\text{B}}$ and selection of operation/hold state in hybrid-IC)

1. Pin format ■CMOS Schmitt configuration containing pull-up resistor (20 kΩ, typical value)
2. Function

   a. When the $\overline{\text{ENABLE}}$ signal is set to a high state or it is opened.
   It is usually placed in the operation status.

   b. When the $\overline{\text{ENABLE}}$ signal is set to a low state
   The hybrid-IC is placed into the hold state, forcing the excitation drive output to be turned off.
   At this time, the system clock of the HC stops, the H-IC is not affected if the input pin other than the reset input changes.

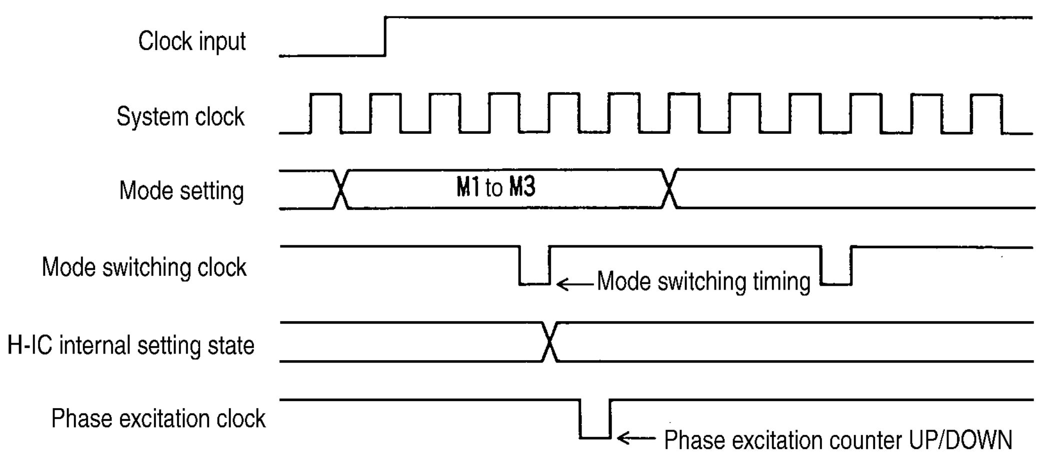
2-5. M1, M2, and M3 (Selection of excitation modes and clock input edge timing)

1. Pin format ■CMOS Schmitt configuration containing the pull-up resistor (20 kΩ typical value)
2. Functions

M2	0	0	1	1	Phase switching clock edge timing
M3 \ M1	0	1	0	1	
1	2 phase excitation	1-2 phase excitation	W1-2 phase excitation	2W1-2 phase excitation	Only the rising edge
0	1-2 phase excitation	W1-2 phase excitation	2W1-2 phase excitation	4W1-2 phase excitation	Rising edge and falling edge

3. Valid timing of mode setting
   ■The mode must not be changed within 5 µs from the rising edge and falling edge of the clock.

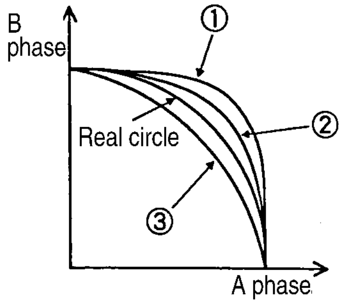
Fetching timing of mode setting



2-6. M4 and M5 (Setting of rotation vector locus at micro-step)

M4	1	0	1	0
M5	1	0	0	1
Mode	Real circle	①	②	③

For the current division ratio, see Section 4-3.



2-7. $\overline{\text{RESET}}$ (Reset of entire system)

1. Pin format ■CMOS Schmitt configuration containing the pull-up resistor (20 kΩ typical value)
2. Function ■All circuit states are set to the initial values by setting the RESET signal to the low state (pulse width of 10 µs or more). At this time, for all modes including the excitation mode, the A and $\overline{\text{B}}$ phases are set to the origin.

2-8. Vref(Setting of the current value used as the reference of constant current detection)

1. Pin format ■Analog input configuration
2. Function ■By applying the voltage of 2.5 V or less of the control system power source Vcc2, the constant current control can be performed over the excitation current of the motor at the 100% of the rated current value.
■The constant current can be controlled in proportional to the Vref voltage with this value specified as a high limit.

3. Explanation of output pins

Pin No.	Name	Function	Pin format
19	MoI	Phase excitation origin monitor	CMOS standard configuration
20, 21	Mo1, Mo2	Phase excitation state monitor	CMOS standard configuration

4. Functions and timing of output signals

4-1. A, $\overline{\text{A}}$, B, and $\overline{\text{B}}$ (Output for phase excitation use of motor)

1. Function ■In four phase two excitation mode, the interval of 3.75 µs (typical value) is set when the output signals of the phases A and $\overline{\text{A}}$, B and $\overline{\text{B}}$ change.

4-2. Mo1, Mo2, and MoI (Monitor of excitation state)

1. Pin format ■CMOS standard configuration
2. Function ■Outputs the state of the current phase excitation output.

Phase coordinate	A phase	B phase	$\overline{\text{A}}$ phase	$\overline{\text{B}}$ phase
Mo1	1	0	0	1
Mo2	0	1	0	1

For the MoI, 0 is output at the origin of each phase.
At other points, 1 is output.

4-3. Current division ratio based on M3, M4, and M5 . . . . Reference values

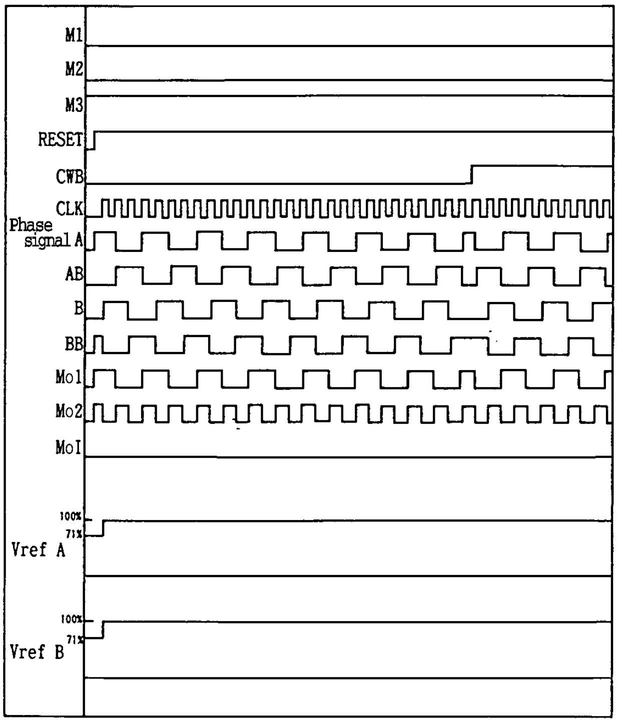
Mode			Real circle	①	②	③	Unit	Number of steps	
Setting	M3 = 0	M3 = 1	M4 = 1	M4 = 0	M4 = 1	M4 = 0			
			M5 = 1	M5 = 0	M5 = 1	M5 = 0			
Current division ratio	4W1–2		14	15	15	13	%		1 / 16
		2W1-2	20	25	23	19		1 / 8	2 / 16
			31	34	33	28			3 / 16
		2W1-2	40	44	42	39		2 / 8	4 / 16
			48	51	49	45			5 / 16
		2W1-2	55	62	57	54		3 / 8	6 / 16
			65	69	65	62			7 / 16
		2W1-2	71	77	71	69		4 / 8	8 / 16
			77	82	77	74			9 / 16
		2W1-2	83	88	85	82		5 / 8	10 / 16
			88	92	89	85			11 / 16
		2W1-2	92	95	95	92		6 / 8	12 / 16
			97	98	98	94			13 / 16
		2W1-2	100	100	100	100		7 / 8	14 / 16

[Load conditions]
$V_{CC}1$ = 24V, $V_{CC}2$ = 5V, R / L = 3.5Ω / 3.8mH

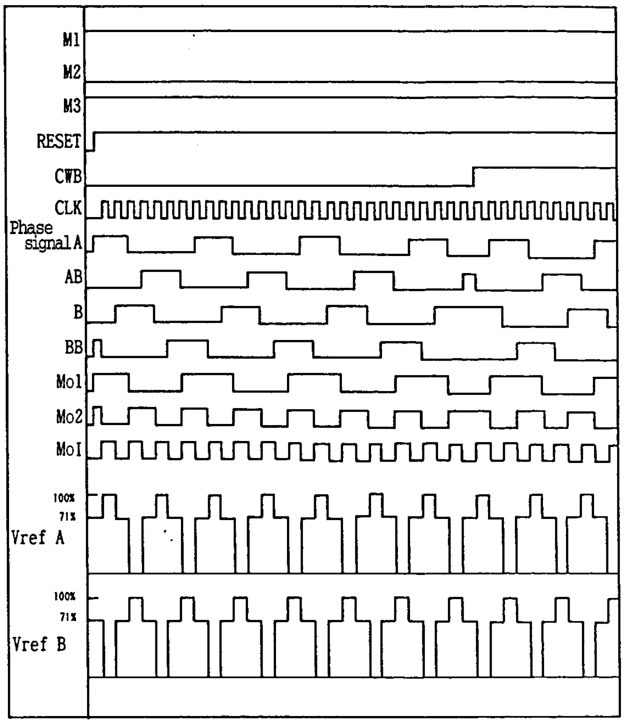
5. Phase excitation and timing chart

5-1. Rising edge operation of clock

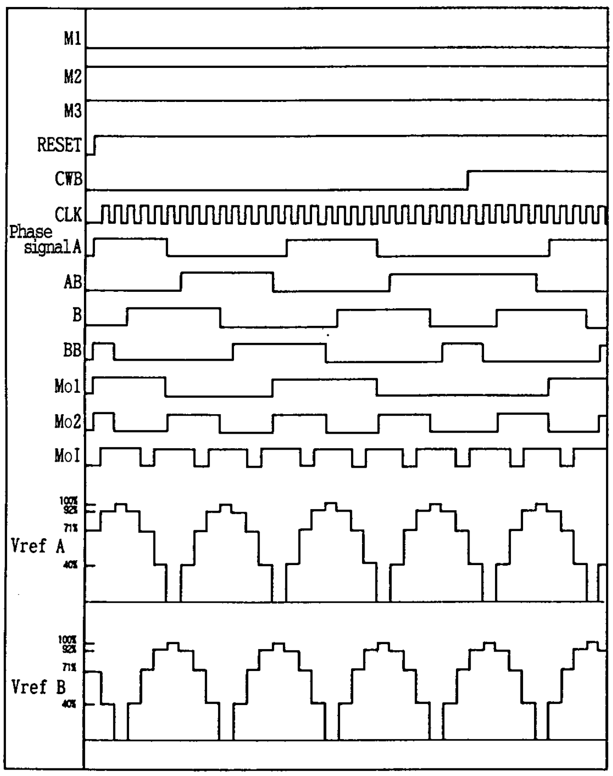
• **2 phase excitation**



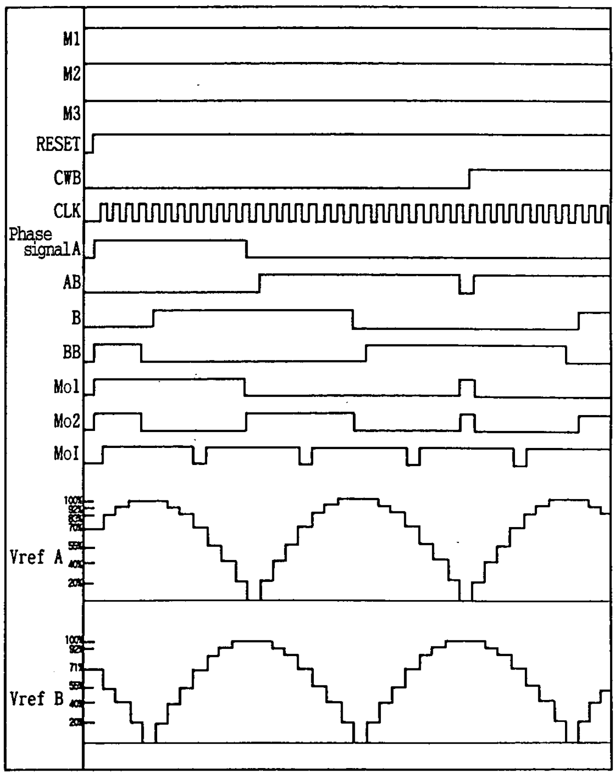
• **1-2 phase excitation**



• **W1-2 phase excitation**

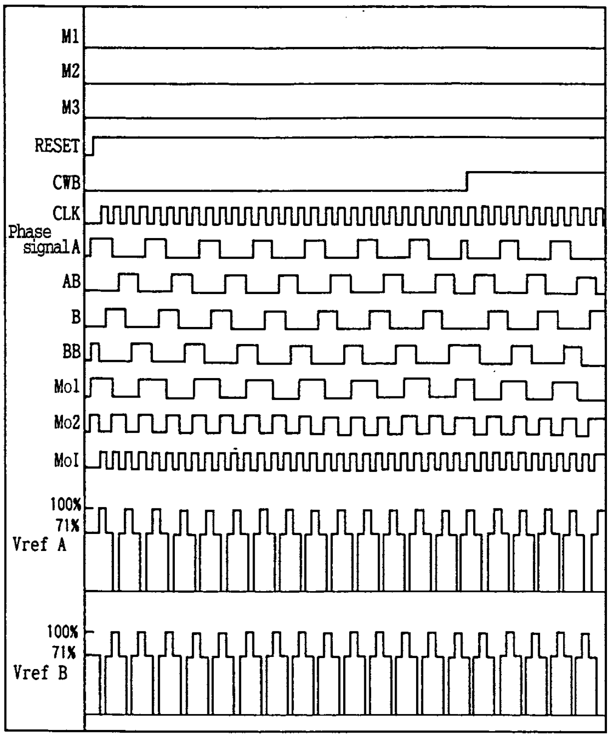


• **2W-2 phase excitation**

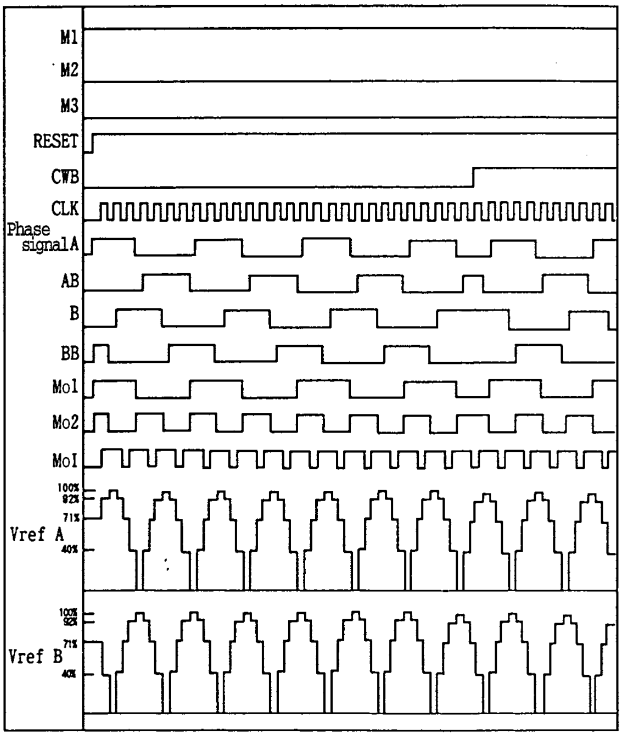


5-2. Rising edge and falling edge operation of clock

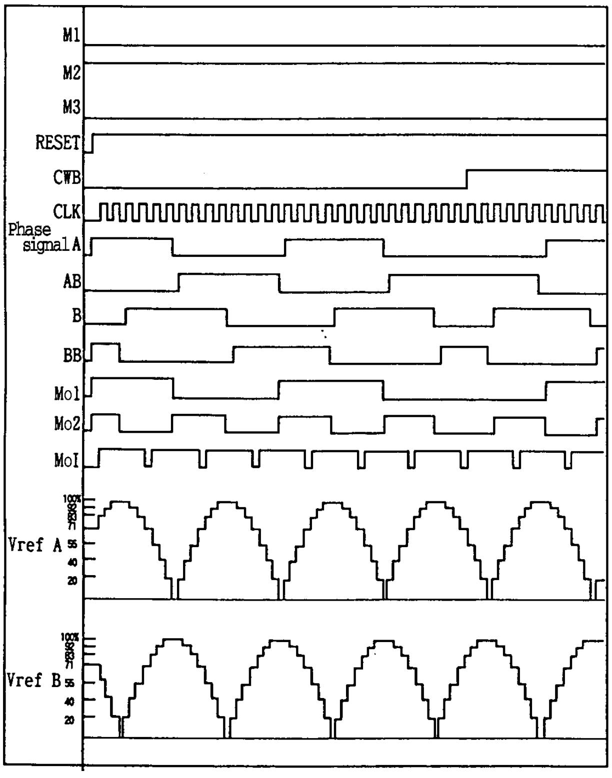
• 2 phase excitation



• 1-2 phase excitation



• W1-2 phase excitation



• 2W-2 phase excitation