TOSHIBA POWER MOS FET MODULE SILICON N & P CHANNEL MOS TYPE (L^2-π-MOSⅣ 6 IN 1)

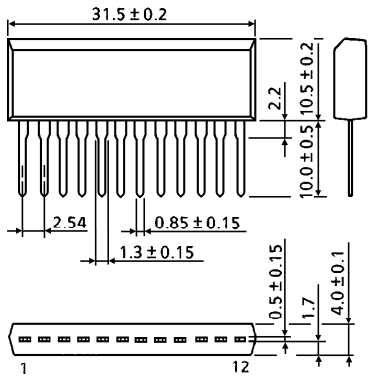
MP6403

HIGH POWER SWITCHING APPLICATION.
3-PHASE MOTOR DRIVE AND BIPOLAR DRIVE OF PULSE MOTOR.

INDUSTRIAL APPLICATIONS

- 4-Volt Gate Drive Available
- Small Package by Full Molding (SIP 12 Pin)
- High Drain Power Dissipation (6 Devices Operation)
  : P_T = 36W (Ta = 25°C)
- Low Drain-Source ON Resistance
  : $R_{DS\ (ON)}$ = 90mΩ (Typ.) (N-ch)
  170mΩ (Typ.) (P-ch)
- Low Leakage Current: I_{GSS} = ±10μA (Max.) (V_{GS} = ±16V)
  I_{DSS} = 100μA (Max.) (V_{DS} = 60V)
- Enhancement-Mode : V_{th} = 0.8~2.0V (I_D = 1mA)

Unit in mm



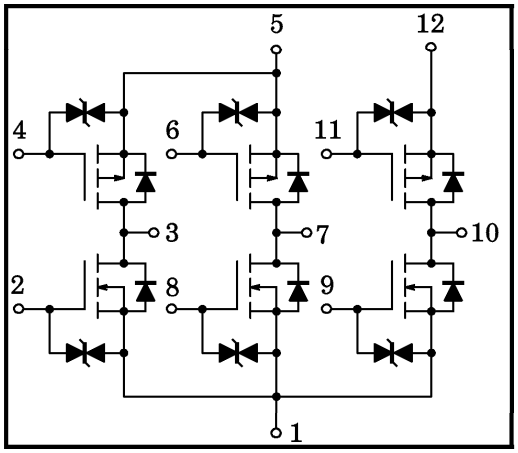
2, 4, 6, 8, 9, 11	GATE
3, 7, 10	DRAIN
1, 5, 12	SOURCE
JEDEC	—
EIAJ	—
TOSHIBA	2-32C1K

Weight : 3.9g

MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC		SYMBOL	RATING N ch	RATING P ch	UNIT
Drain-Source Voltage		V_{DSS}	60	−60	V
Gate-Source Voltage		V_{GSS}	±20	±20	V
Drain Current		I_D	5	−5	A
Peak Drain Current		I_{DP}	20	−20	A
Collector Power Dissipation (1 Device Operation)		P_D	2.2		W
Collector Power Dissipation (6 Devices Operation)	Ta = 25°C	P_T	4.4		W
	Tc = 25°C		36		
Channel Temperature		T_{ch}	150		°C
Storage Temperature Range		T_{stg}	−55~150		°C

ARRAY CONFIGURATION

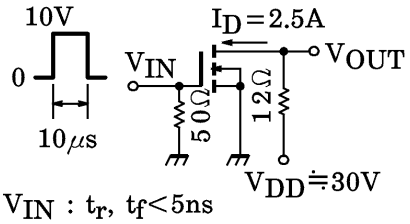


THERMAL CHARACTERISTICS

CHARACTERISTIC	SYMBOL	MAX.	UNIT
Thermal Resistance of Channel to Ambient (6 Devices Operation, Ta = 25°C)	$\Sigma R_{th\,(ch\text{-}a)}$	28.4	°C / W
Thermal Resistance of Channel to Case (6 Devices Operation, Tc = 25°C)	$\Sigma R_{th\,(ch\text{-}c)}$	3.47	°C / W
Maximum Lead Temperature for Soldering Purposes (3.2mm from Case for 10s)	T_L	260	°C

This Transistor is an Electrostatic Sensitive Device. Please Handle with Caution.

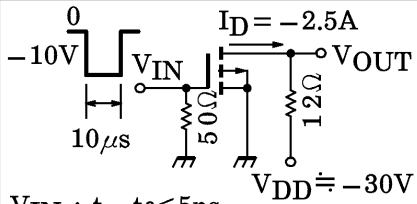
ELECTRICAL CHARACTERISTICS (Ta = 25°C) (Nch MOS FET)

CHARACTERISTIC		SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Gate Leakage Current		I_{GSS}	$V_{GS}=\pm16V$, $V_{DS}=0$	—	—	±10	μA
Drain Cut-off Current		I_{DSS}	$V_{DS}=60V$, $V_{GS}=0$	—	—	100	μA
Drain-Source Breakdown Voltage		$V_{(BR)\,DSS}$	$I_D=10mA$, $V_{GS}=0$	60	—	—	V
Gate Threshold Voltage		V_{th}	$V_{DS}=10V$, $I_D=1mA$	0.8	—	2.0	V
Forward Transfer Admittance		$\|Y_{fs}\|$	$V_{DS}=10V$, $I_D=2.5A$	3.0	6.0	—	S
Drain-Source ON Resistance		$R_{DS\,(ON)}$	$I_D=2.5A$, $V_{GS}=4V$	—	135	200	mΩ
		$R_{DS\,(ON)}$	$I_D=2.5A$, $V_{GS}=10V$	—	90	125	
Input Capacitance		C_{iss}	$V_{DS}=10V$, $V_{GS}=0$, f=1MHz	—	500	—	pF
Reverse Transfer Capacitance		C_{rss}		—	90	—	
Output Capacitance		C_{oss}		—	290	—	
Switching Time	Rise Time	t_r	 V_{IN} : t_r, $t_f<5ns$ Du.≦1% ($Z_{OUT}=50\Omega$)	—	20	—	ns
	Turn-on Time	t_{on}		—	60	—	
	Fall Time	t_f		—	80	—	
	Turn-off Time	t_{off}		—	300	—	
Total Gate Charge (Gate-Source Plus Gate-Drain)		Q_g	$I_D=5A$, $V_{GS}=10V$ $V_{DD}=48V$	—	20	—	nC
Gate-Source Charge		Q_{gs}		—	14	—	
Gate-Drain ("Miller") Charge		Q_{gd}		—	6	—	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Drain Reverse Current	I_{DR}	—	—	—	5	A
Peak Drain Reverse Current	I_{DRP}	—	—	—	20	A
Diode Forward Voltage	V_{DSF}	$I_{DR}=5A$, $V_{GS}=0$	—	—	−1.5	V
Reverse Recovery Time	t_{rr}	$I_{DR}=5A$, $V_{GS}=0$ $dI_{DR}/dt=-50A/\mu s$	—	140	—	ns
Reverse Recovery Charge	Q_{rr}		—	0.4	—	μC

ELECTRICAL CHARACTERISTICS (Ta = 25°C) (Pch MOS FET)

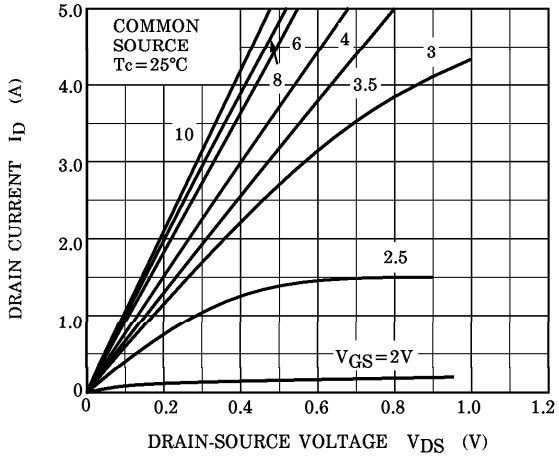
CHARACTERISTIC		SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Gate Leakage Current		I_{GSS}	$V_{GS} = \pm 16V$, $V_{DS} = 0$	—	—	±10	μA
Drain Cut-off Current		I_{DSS}	$V_{DS} = -60V$, $V_{GS} = 0$	—	—	−100	μA
Drain-Source Breakdown Voltage		$V_{(BR)\,DSS}$	$I_D = -10mA$, $V_{GS} = 0$	−60	—	—	V
Gate Threshold Voltage		V_{th}	$V_{DS} = -10V$, $I_D = -1mA$	−0.8	—	−2.0	V
Forward Transfer Admittance		$\|Y_{fs}\|$	$V_{DS} = -10V$, $I_D = -2.5A$	1.0	2.0	—	S
Drain-Source ON Resistance		$R_{DS\,(ON)}$	$I_D = -2.5A$, $V_{GS} = -4V$	—	250	400	mΩ
		$R_{DS\,(ON)}$	$I_D = -2.5A$, $V_{GS} = -10V$	—	170	245	
Input Capacitance		C_{iss}	$V_{DS} = -10V$, $V_{GS} = 0$, f = 1MHz	—	500	—	pF
Reverse Transfer Capacitance		C_{rss}		—	90	—	
Output Capacitance		C_{oss}		—	290	—	
Switching Time	Rise Time	t_r	 V_{IN} : t_r, $t_f < 5ns$ Du. ≦ 1% ($Z_{OUT} = 50\Omega$)	—	120	—	ns
	Turn-on Time	t_{on}		—	130	—	
	Fall Time	t_f		—	80	—	
	Turn-off Time	t_{off}		—	200	—	
Total Gate Charge (Gate-Source Plus Gate-Drain)		Q_g	$I_D = -5A$, $V_{GS} = -10V$ $V_{DD} = -48V$	—	22	—	nC
Gate-Source Charge		Q_{gs}		—	14	—	
Gate-Drain ("Miller") Charge		Q_{gd}		—	8	—	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (Ta = 25°C)

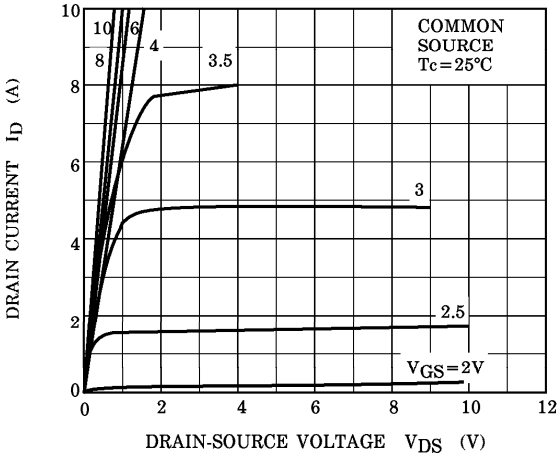
CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Drain Reverse Current	I_{DR}	—	—	—	−5	A
Peak Drain Reverse Current	I_{DRP}	—	—	—	−20	A
Diode Forward Voltage	V_{DSF}	$I_{DR} = -5A$, $V_{GS} = 0$	—	—	1.5	V
Reverse Recovery Time	t_{rr}	$I_{DR} = -5A$, $V_{GS} = 0$ $dI_{DR}/dt = -50A/\mu s$	—	120	—	ns
Reverse Recovery Charge	Q_{rr}		—	0.24	—	μC

Nch FET

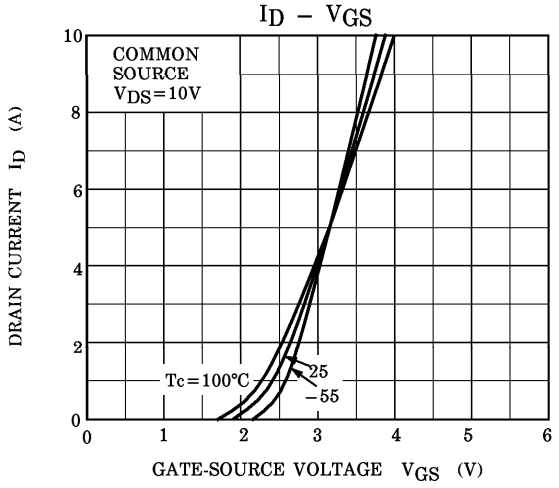
$I_D - V_{DS}$



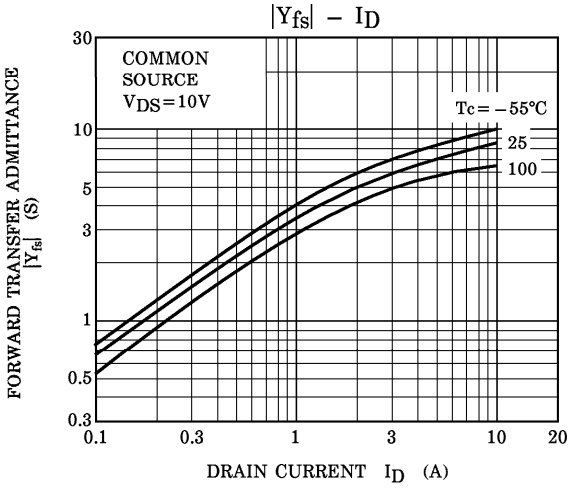
$I_D - V_{DS}$



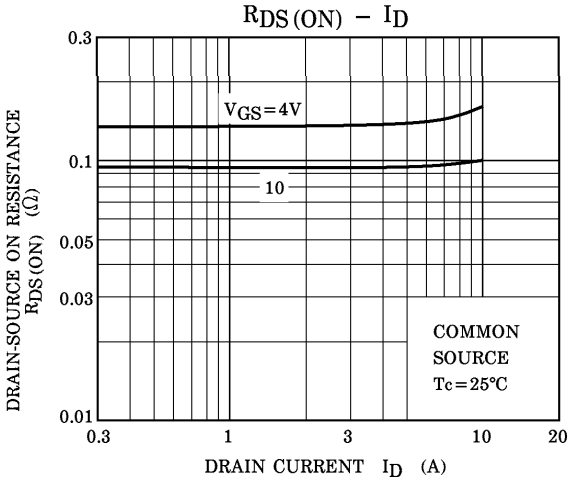
$I_D - V_{GS}$



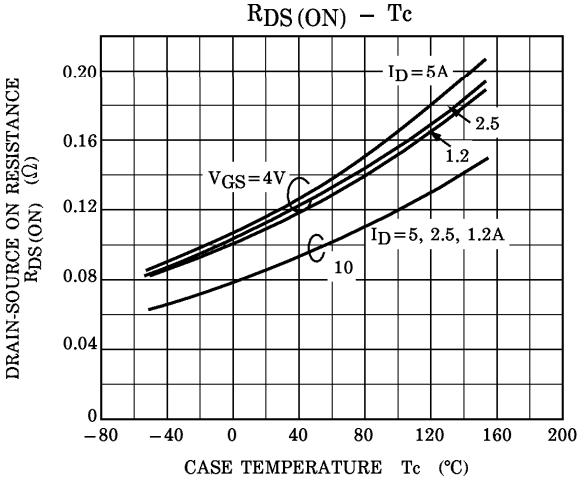
$|Y_{fs}| - I_D$



$R_{DS\,(ON)} - I_D$

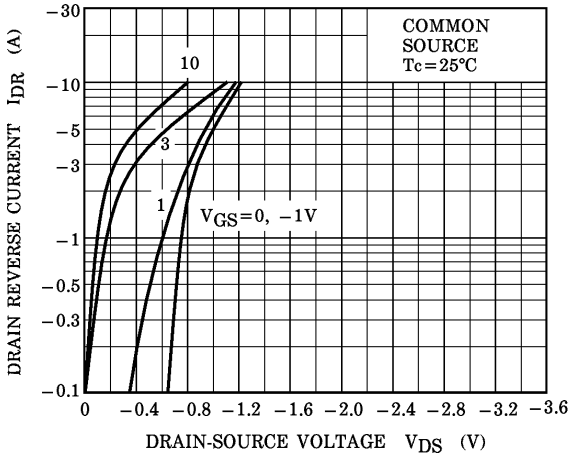


$R_{DS\,(ON)} - T_c$

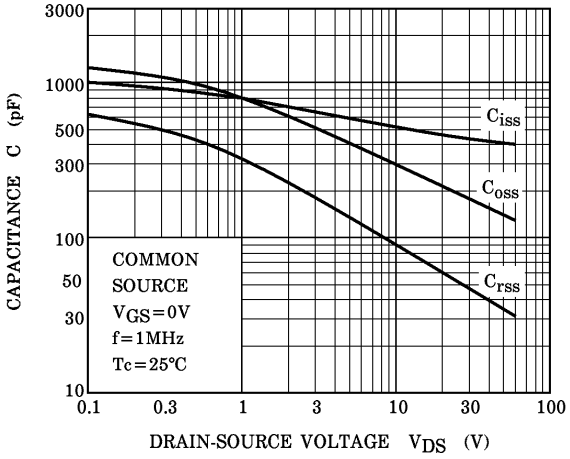


Nch FET

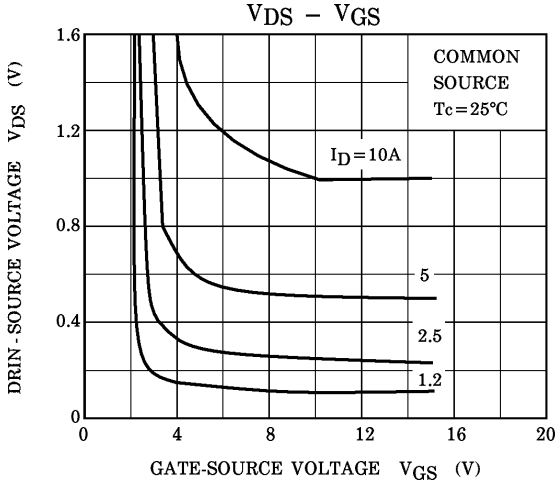
$I_D - V_{DS}$



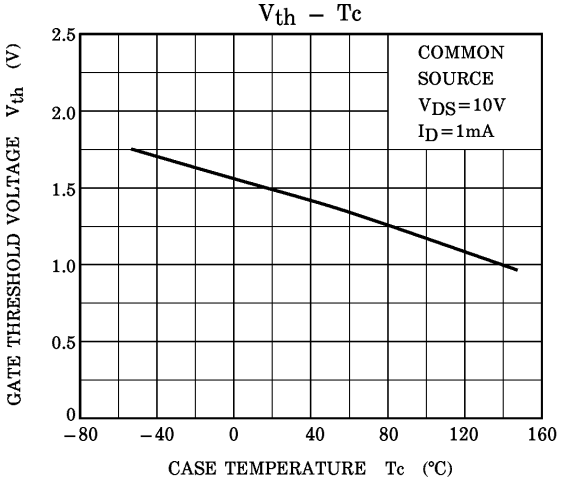
CAPACITANCE – V_{DS}



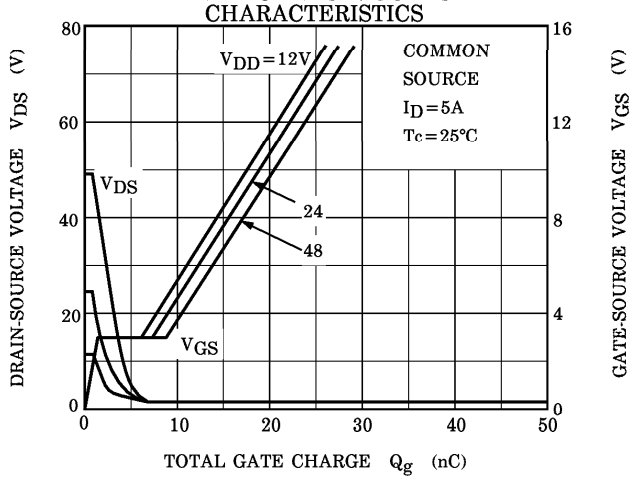
$V_{DS} - V_{GS}$



$V_{th} - Tc$

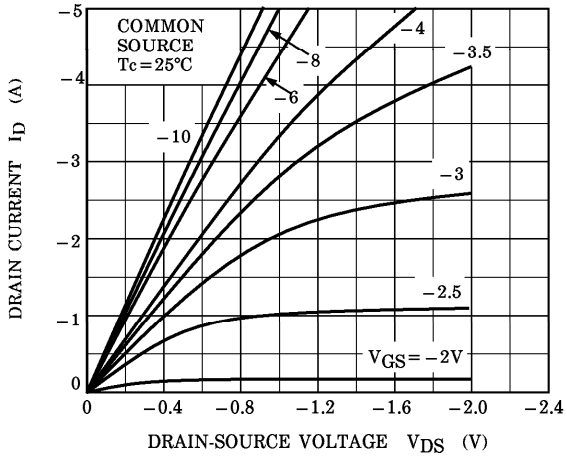


DYNAMIC INPUT / OUTPUT CHARACTERISTICS

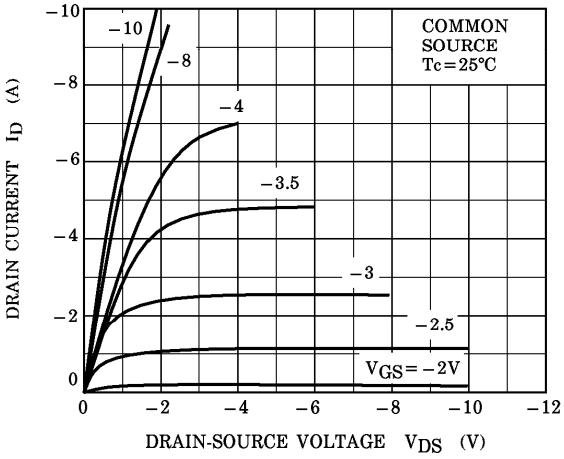


Pch FET

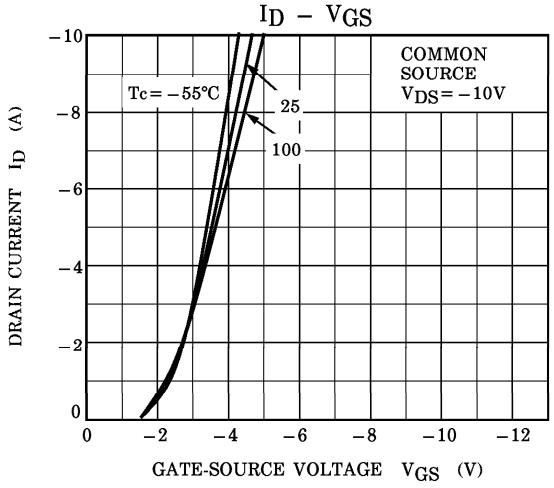
$I_D - V_{DS}$



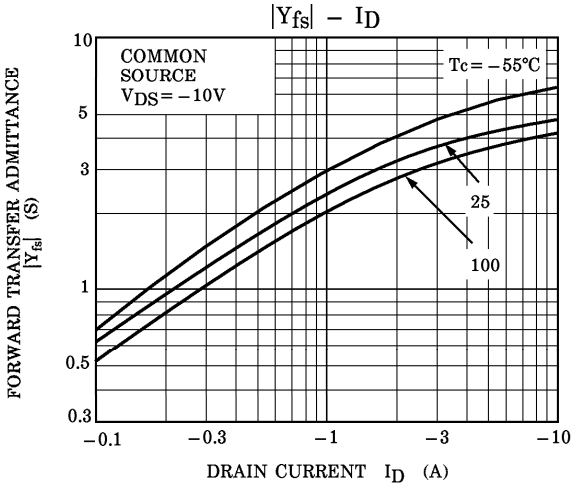
$I_D - V_{DS}$



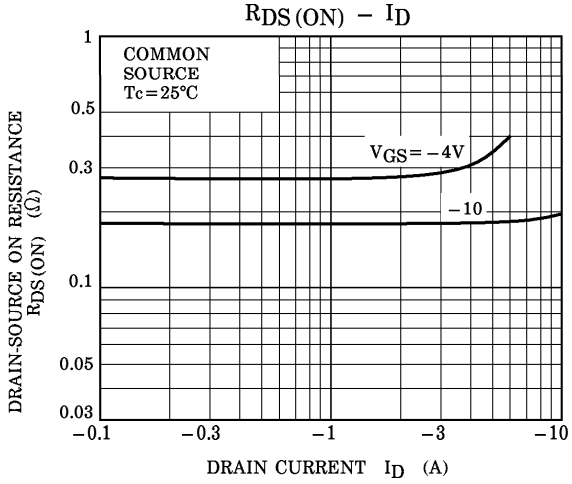
$I_D - V_{GS}$



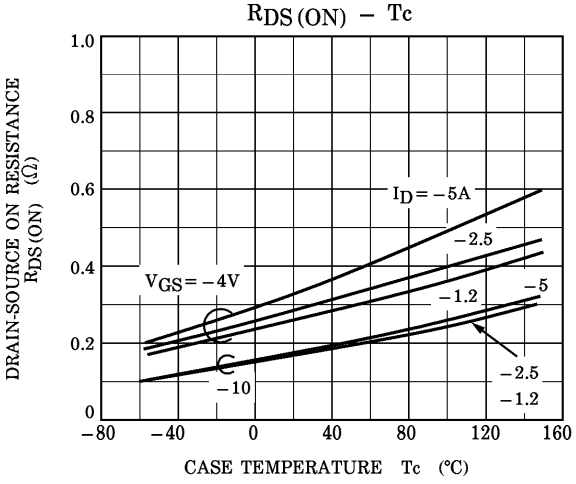
$|Y_{fs}| - I_D$



$R_{DS\,(ON)} - I_D$

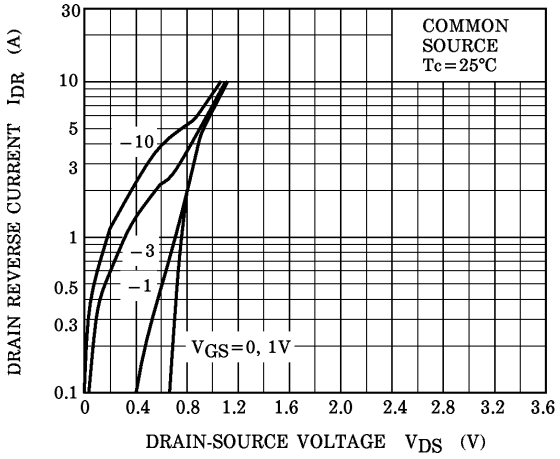


$R_{DS\,(ON)} - Tc$

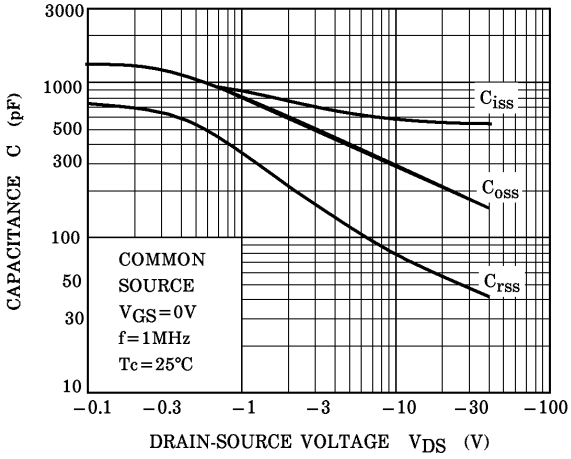


Pch FET

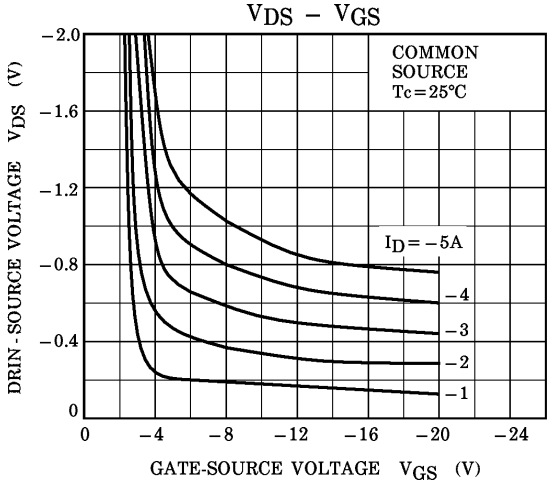
I_{DR} – V_{DS}



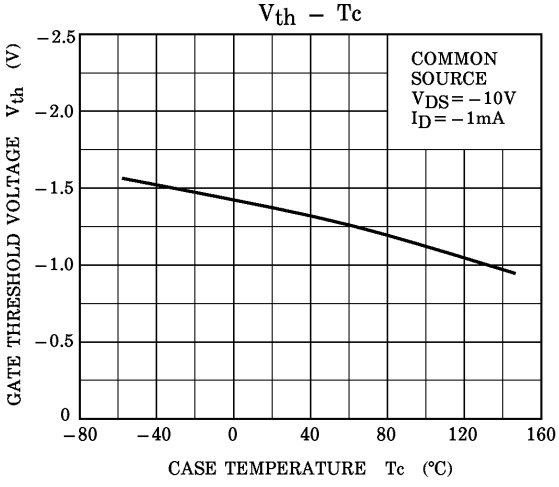
CAPACITANCE – V_{DS}



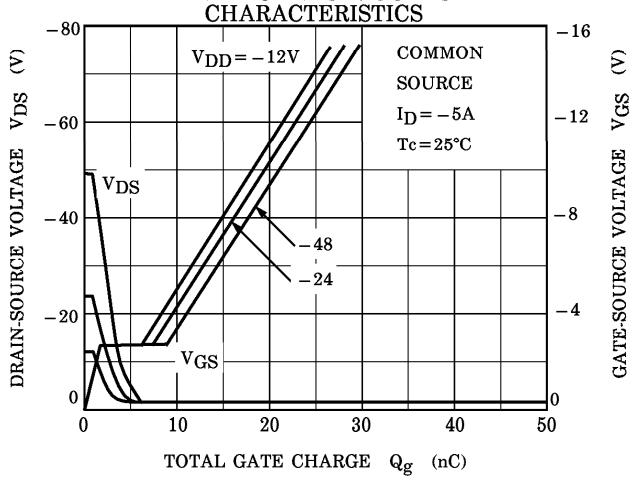
V_{DS} – V_{GS}



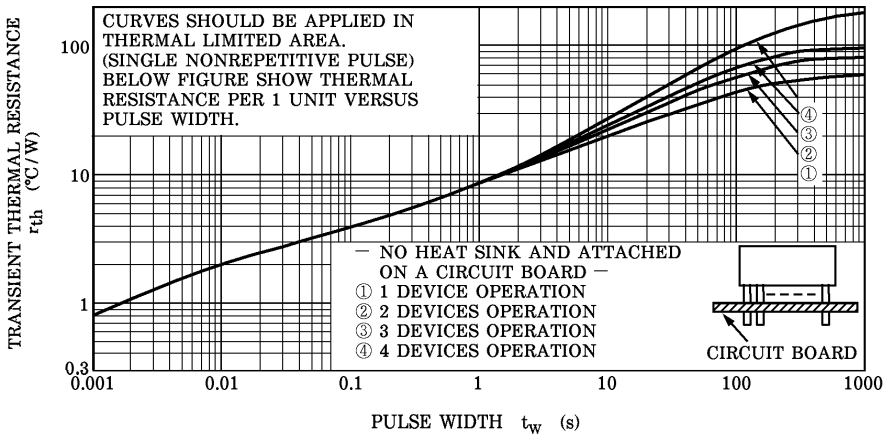
V_{th} – Tc



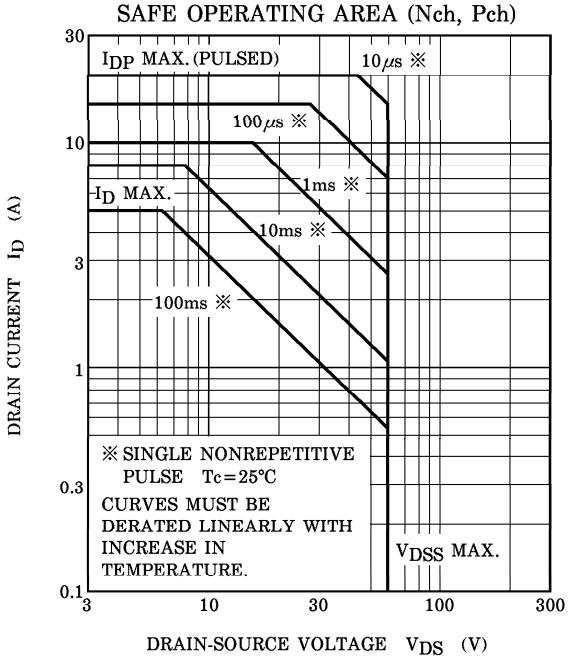
DYNAMIC INPUT / OUTPUT CHARACTERISTICS



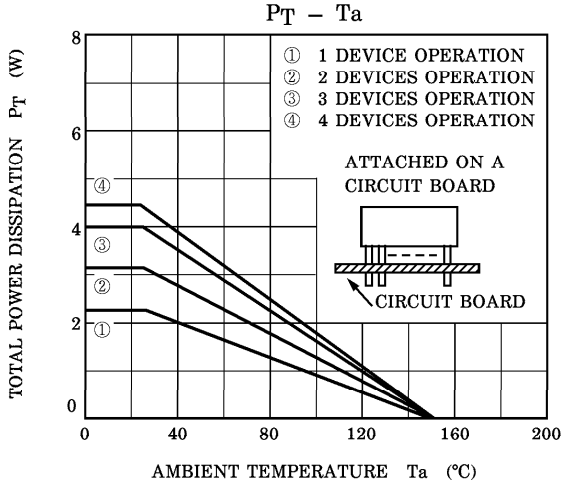
$r_{th} - t_w$



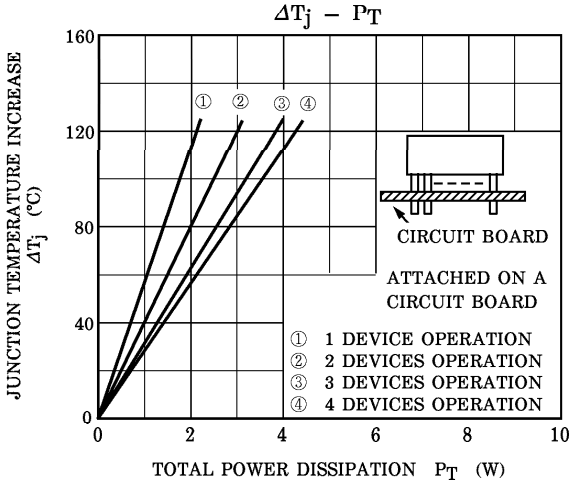
SAFE OPERATING AREA (Nch, Pch)



$P_T - Ta$



$\Delta T_j - P_T$



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000707EAA

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