No. RD-98Y08

# **SHARP**

## RELIABILITY TEST REPORT

Product Type: Smart voltage 32Mbit Flash Memory

Model No.: LH28F320S3NS

Package: 56Pin SSOP (SSOP056-P-0600)

Date: NOV. 10, 1998

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#### 1. Quality Assurance And Reliability Test During New Product Development

New product development begins with establishing reliability targets during the planning stage. During this stage the end applications functions and requirements are also considered in addition to the reliability targets.

Quality and reliability are built into the product from the start by having design and reliability review sessions in the development and design stages.

This insures that quality and reliability levels are maintained at the preproduction and mass production stages.

## 2. Reliability Test Methods

Reliability tests should always have good reproducibility. Thus, reliability tests for IC devices are based upon standardized test methods. Such uniform testing standards include those established by JIS(Japanese Industrial Standard) MIL-STD(U.S.MILitary Standard), EIAJ(Electronic Industries Association of Japan) and IEC(International Electrotechnical Commission). Sharp has based its own testing methods on these standards.

## 3. Evaluation Results

The results attached show that Sharp has met the high quality and reliability targets which are required by the above standards.

Note; This evaluation has been performed upon a representative product which is selected from a series of related products with the same basic design, all packaged in the same package type.

Therefore, these evaluation results are applicable for the following Sharp models:

LH28F320S3NS

#### 4. Other Considerations

Please confirm that the specifications of this product meet the requirements of the applications.

## 1-1. ENDURANCE TEST-1

No.	Test	Conditions		Reference Standards	Number of Samples	of /Test Time			LTPD
	High	Ta=125℃		JIS C 7022:B-1		240h	500h	1000h	
1	Temperature	Vpp/Vcc=4.0V		MIL-STD-883C	153	0	0	0	1.5%
	Operation		1000h	1005.6					
	High	Ta=140°C		JIS C 7022:B-3		240h	500h	1000h	
2	Temperature			MIL-STD-883C	45	0	0	0	5%
	Storage		1000 h	1008.2					
	Low	Ta=-65°C				240h	500h_	1000h	
3	Temperature			JIS C 7022:B-4	11	0	0	0	20%
	Storage		1000 <b>h</b>						
	High Temp.	Ta=60°C,90%RH				240h	500h	1000h	
4	High Humi.			JIS C 7022:B-5	22	0	0	0	10%
	Storage		1000h						
	High Temp.	Ta=85℃,85%RH				240h	500h	1000h	
5	High Humi.	Vpp/Vcc=3.6V		JIS C 7022:B-5	76	0	0	0	3%
	Bias		1000h						

## 1-2. ENDURANCE TEST-2

No.	Test	Conditions	Reference Standards	Number of Samples	Number Of Failures	LTPD
6	Thermal Shock	Ta=-65℃(5min)~150℃(5min) 100cyc.	JIS C 7022:A-3 MIL-STD-883C 1011.7	45	0	5%
7	Temperature Cycling	Ta=-65°C(30min) ~ 150°C(30min) 500cyc.	JIS C 7022:A-4 MIL-STD-883C 1010.7	76	0	3%
8	Temperature & Humidity Cycling	Ta=-10°C ~65°C,90~95% RH 1cyc./24h 10cyc.	JIS C 7022:A-5 MIL-STD-883C 1004.7	22	0	10%
9	Salt Atmosphere	Salt Concentration=5wt% Salt Fog Temp.=35°C Spray Rate=10~50g/m <sup>2</sup> /d 24h	MIL-STD-883C 1009.7	22	0	10%

## **CRITERIA**

- No.1  $\sim$  8 : To maintain electrical characteristics within the limits established in the specifications of each device.
- No.9 : To maintain electrical characteristics within the limits established in the specifications of each device. There is no evidence of damage to the body material or lead finish of each device.

  All package marking is remain visible to the naked eye.



## 1-3. ENDURANCE TEST-3

No.	Test	Conditions		Reference Standards	Number of Samples	Number of Failures	LTPD
10	[Series Test]  Baking  Moisture  Absorption	Ta=150°C Ta=30°C,70%	20h 96h	EIAJ ED-4701:B-101	22		10%
	I.R Soldering ↓ PCT	Highest Temp.=240°C $230$ °C $^{-}$ 240°C, $Ta=121$ °C, $100$ %RH, No $2\times10^{5}$ Pa{2atm}	15s Bias 100h			0	

## **CRITERIA**

No.10: To maintain electrical characteristics within the limits established in the specifications of each device. There is no evidence of damage to the body material(i.e. Package cracking).

## 2. Erase/Write Cycling Test

No.	Test	Conditions	Number of Cycles	Number of Samples	Number Of Failures	Failure Rate	Note
1	Erase/ Write	Ta=0,70°C	10k	520	0	28 DPM/Block	Confidence Level=60%
	Cycling		100k		0	110 DPM/Block	,

## **CRITERIA**

No.1: To maintain electrical characteristics within the limits established in the specifications of each device.



## 3. MECHANICAL TEST

	_		Reference	Number	Number	
No.	Test	Conditions	Standards	of	of	LTPD
L				Samples	Failures	
		$100\sim2000\sim100$ Hz, 4min	JIS C 7022:A-10			
1	Vibration	200m/s <sup>2</sup> {20G}	MIL-STD-883C 2007.1	11	0	20%
		X,Y,Z each 4times, total 48min.				
2	Shock	15000m/s <sup>2</sup> {1500G}	JIS C 7022:A-7	11	0	20%
		0.5ms, $\pm X, \pm Y, \pm Z$ each 3 times	MIL-STD-883C 2002.3			
3	Acceleration	200000m/s <sup>2</sup> {20000G}	JIS C 7022:A-9	11	0	20%
		$\pm X, \pm Y, \pm Z$ each 1 min.	MIL-STD-883C 2001.2			
		A specified load % is applied to the				
4	Terminal Strength	tip of each lead is bent once	JIS C 7022:A-11	5	0	50%
	(Bending)	through a 90° arc and back.	MIL-STD-883C 2004.5			
		<del>0.125, 0.25,</del> 0.5, <del>1.25</del> N 1time				
	Terminal Strength	A specified load % is applied in a	JIS C 7022:A-11			
5	(Tension)	direction parallel to the lead axis.	MIL-STD-883C 2004.5	5	0	50%
		<del>0.25, 0.5,</del> 1, <del>2.5</del> N 10s				
6	Solderability	230℃ 5s	JIS C 7022:A-2	11	0	20%
		Used with rosin flux	MIL-STD-883C 2003.5			

\* The specified load is determined by nominal cross section.

## **CRITERIA**

- No.1,2,3 :To maintain electrical characteristics within the limits established in the specifications of each device.
- No.4,5 :There is no evidence of damage to the body. There is no broken or cracked lead (terminals).
- No.6 :Lead coverage of at least 95% with a continuous solder coating. Pinholes and voids are not concentrated in one area and exceed 5% of the total area.



## 3. MISCELLANEOUS

			Reference	Number	Number	
No.	Test	Conditions	Standards	of	of	LTPD
				Samples	Failures	<u> </u>
			EIAJ ED-4701:C-121			
1	Permanence	20~25°C, Brushing 5 times	(Solvent): Acetone, Butyl acetate,	11(each)	0	20%
	of Marking	after dipping 10 minutes	Isopropyl alcohol,			
			Ethyl alcohol			

No.	Test	Conditions	Reference Standards	Number Of Samples	Conditions	ESD/Latch-up Strength			th
			Standards	Gampies		≥0.5kV	≥1.0kV	≥1.5kV	≥2.0kV
2	Electrostatic	C=100pF	MIL-STD	3(each)	GND+				
	discharges	$R=1.5k\Omega$	883C		GND-				0
			Method		VCC+				0
			3015		VCC-				0
						≥40mA	≧60mA	≥80mA	≥100mA
		Current application	EIAJ	3(each)	+				0
3	Latch-up	test	ED-4701-1		_				0
	_	tp=10ms, toff=500ms	C-113						
		VccMAX							

" $\bigcirc$ " Pass, " $\times$ " NG, "-" No measurement

## **CRITERIA**

No.1: There is no evidence of damage to the device and package marking which are no missing in whole or in part.

No.2: To maintain electrical characteristics within the limits established in the specifications of each device.

No.3: No latch-up occurs.



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