Ordering number : EN※4838

CMOS LSI

SANYO

No. ※4838

LC78834M

Stereo 18-bit Digital Audio D/A Converter with On-Chip 4 fs Digital Filters

Preliminary

Overview

The LC78834M is a CMOS stereo 18-bit D/A converter LSI that includes 4× oversampling digital filters, output op amps, and analog filter op amps on chip.

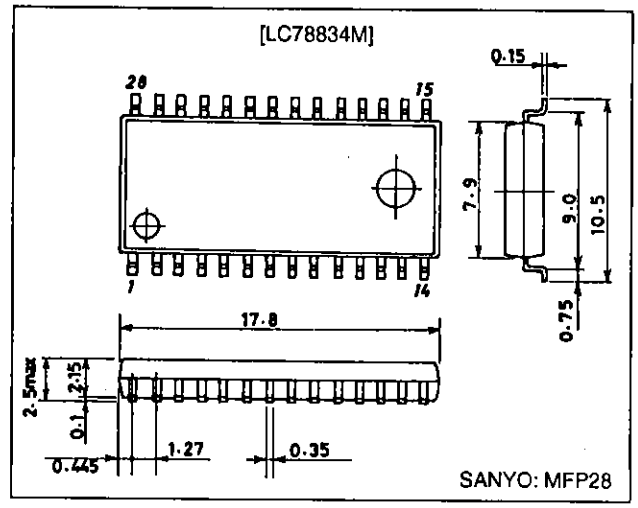
Functions and Features

- Digital filter block
  - — 4× oversampling filters: two-stage FIR filter structure (43rd order and 11th order)
  - — De-emphasis filters: support for fs = 32, 44.1, and 48 kHz
  - — Soft muting
- D/A converter block
  - — Dynamic level shifting 18-bit D/A converter
  - — Two D/A converter channels built in (in-phase outputs)
  - — Built-in output op amps
- Built-in analog filter op amps
- System clock: support for both 384 fs and 512 fs
- Single 5 V power supply
- Low voltage operation supported (3.5 V)
- Si gate CMOS process (low power)

Package Dimensions

unit: mm

3091-MFP28



Specifications

Absolute Maximum Ratings at V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max		–0.3 to +7.0	V
Input voltage	V_{IN}		–0.3 to V_{DD} + 0.3	V
Output voltage	V_{OUT}		–0.3 to V_{DD} + 0.3	V
Operating temperature	Topr		–30 to +75	°C
Storage temperature	Tstg		–40 to +125	°C

Allowable Operating Ranges

Parameter	Symbol	Conditions	min	typ	max	Unit
Supply voltage	V_{DD}		3.5	5.0	5.5	V
Operating temperature	Topr		–30		+75	°C

SANYO Electric Co., Ltd. Semiconductor Business Headquarters
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110 JAPAN

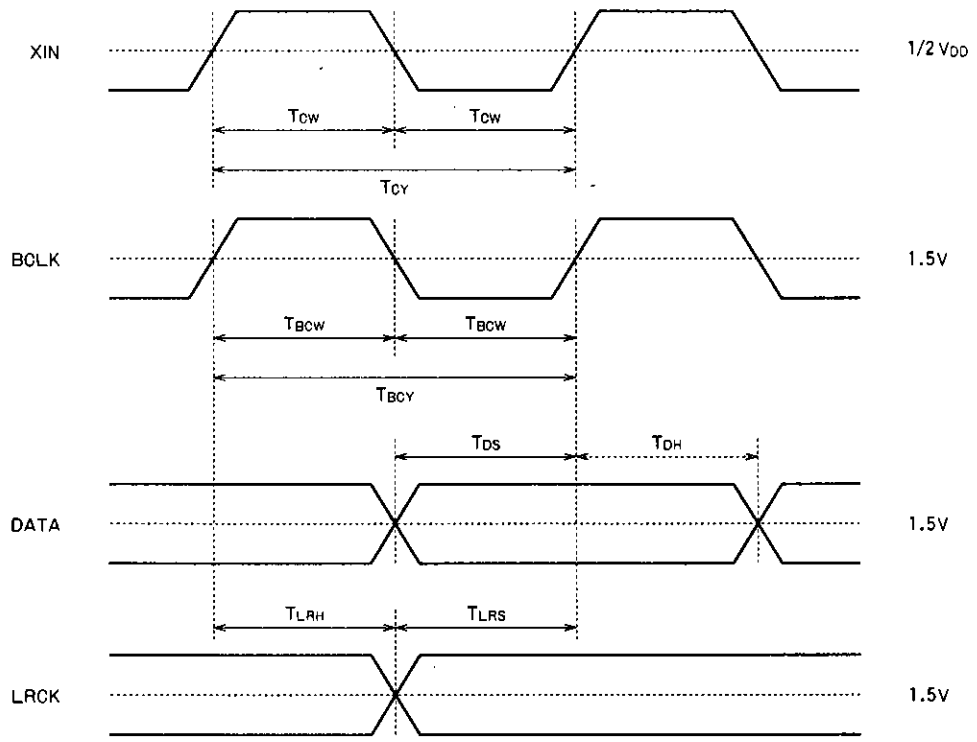
DC Characteristics at Ta = –30 to +75°C, V_{DD} = 3.5 to 5.5 V, V_{SS} = 0 V

Parameter	Symbol	Conditions	min	typ	max	Unit
Input high level voltage (1)	$V_{IH}1$	Pins 1, 2, 3, 4, 5, 6, 7, 8, 9, 15 and 16	2.2			V
Input low level voltage (1)	$V_{IL}1$	Pins 1, 2, 3, 4, 5, 6, 7, 8, 9, 15 and 16			0.8	V
Input high level voltage (2)	$V_{IH}2$	Pin 13	0.7 V_{DD}			V
Input low level voltage (2)	$V_{IL}2$	Pin 13			0.3 V_{DD}	V
Output high level voltage	V_{OH}	Pin 11, I_{OH} = –3 mA	2.4			V
Output low level voltage	V_{OL}	Pin 11, I_{OL} = 3 mA			0.4	V
Input leakage current	V_L	Pins 1, 2, 3, 4, 5, 6, 7, 8, 9, 13, 15 and 16, V_I = V_{SS}, V_{DD}	–25		+25	µA

AC Characteristics at Ta = –30 to +75°C, V_{DD} = 3.5 to 5.5 V, V_{SS} = 0 V

Parameter	Symbol	Conditions	min	typ	max	Unit
Oscillator frequency	f_X	The XIN pin when a crystal oscillator is used	1.0		25	MHz
Clock pulse width	t_{CW}	The XIN pin when an external clock signal is provided	18			ns
Clock pulse period	t_{CY}	The XIN pin when an external clock signal is provided	40		1000	ns
BCLK pulse width	t_{BCW}		60			ns
BCLK pulse period	t_{BCY}		120			ns
Data setup time	t_{DS}		40			ns
Data hold time	t_{DH}		40			ns
LRCK setup time	t_{LRS}		40			ns
LRCK hold time	t_{LRH}		40			ns

Audio Input Waveforms



Electrical Characteristics for D/A Converter (1)

at Ta = 25°C, AV_{DD} = DV_{DD} = 5.0 V, AGND = DGND = 0 V, unless otherwise specified

Parameter	Symbol	Conditions	min	typ	max	Unit
D/A converter resolution	RES			18		Bits
Total harmonic distortion	THD	1 kHz, at 0 dB, *1			0.08	%
Dynamic range	DR	1 kHz, at –60 dB	90			dB
Crosstalk	CT	1 kHz, at 0 dB, *1			–85	dB
Signal-to-noise ratio	S/N	JIS-A	96			dB
Full-scale output voltage	VFS		2.2	2.4	2.6	Vp-p
Power dissipation	Pd	1 kHz, at 0 dB, *2		135	200	mW
Output load resistance	RL	Pins 21 and 23	5			kΩ

Electrical Characteristics for D/A Converter (2)

at Ta = 25°C, AV_{DD} = DV_{DD} = 3.5 V, AGND = DGND = 0 V, unless otherwise specified

Parameter	Symbol	Conditions	min	typ	max	Unit
D/A converter resolution	RES			18		Bits
Total harmonic distortion	THD	1 kHz, at 0 dB, *1			0.12	%
Dynamic range	DR	1 kHz, at –60 dB	90			dB
Crosstalk	CT	1 kHz, at 0 dB, *1			–85	dB
Signal-to-noise ratio	S/N	JIS-A	96			dB
Full-scale output voltage	VFS		1.5	1.7	1.9	Vp-p
Power dissipation	Pd	1 kHz, at 0 dB, *3		50	75	mW
Output load resistance	RL	Pins 21 and 23	15			kΩ

Note: 1. "0 dB" means the full scale output level.
2. With the XIN pin (pin 13) at 1.5 to 3.5 V, f_X = 16.9344 MHz, fs = 44.1 kHz (384 fs)
3. With the XIN pin (pin 13) at 1.0 to 2.5 V, f_X = 16.9344 MHz, fs = 44.1 kHz (384 fs)

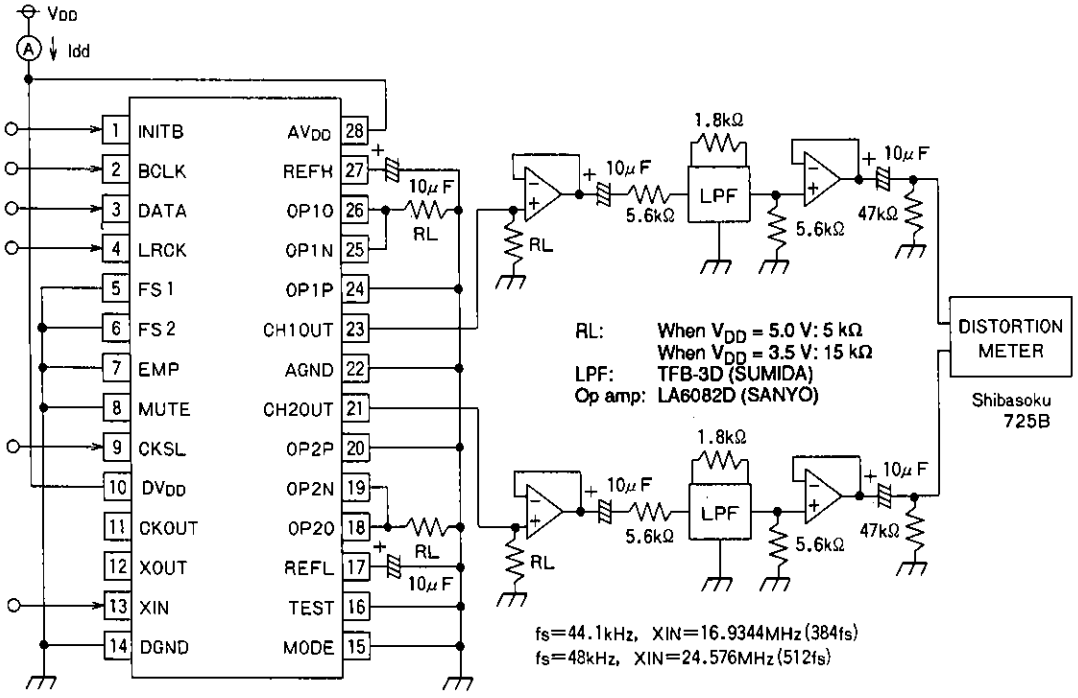
Operational Amplifier Block

at Ta = 25°C, AV_{DD} = DV_{DD} = 5.0 V, AGND = DGND = 0 V, unless otherwise specified

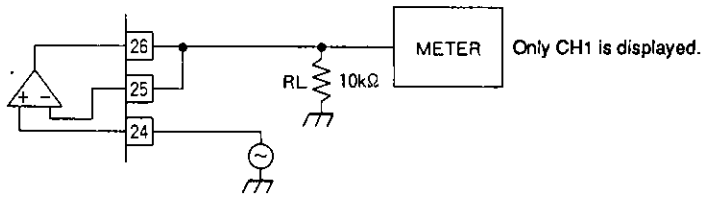
Parameter	Symbol	Conditions	min	typ	max	Unit
Slew rate	SR	RL = 10 kΩ		9		V/μs
Input offset voltage	VIO			1.5		mV
Gain-bandwidth product	FT	V_{IN} = 2 Vp-p		2.0		MHz
Maximum output voltage	VOPP	RL = 10 kΩ	0.3		4.7	V
Common-mode input voltage range	VIC		0.6		3.6	V
Output load resistance	RL	Pins 18 and 26	5			kΩ

Test Circuits

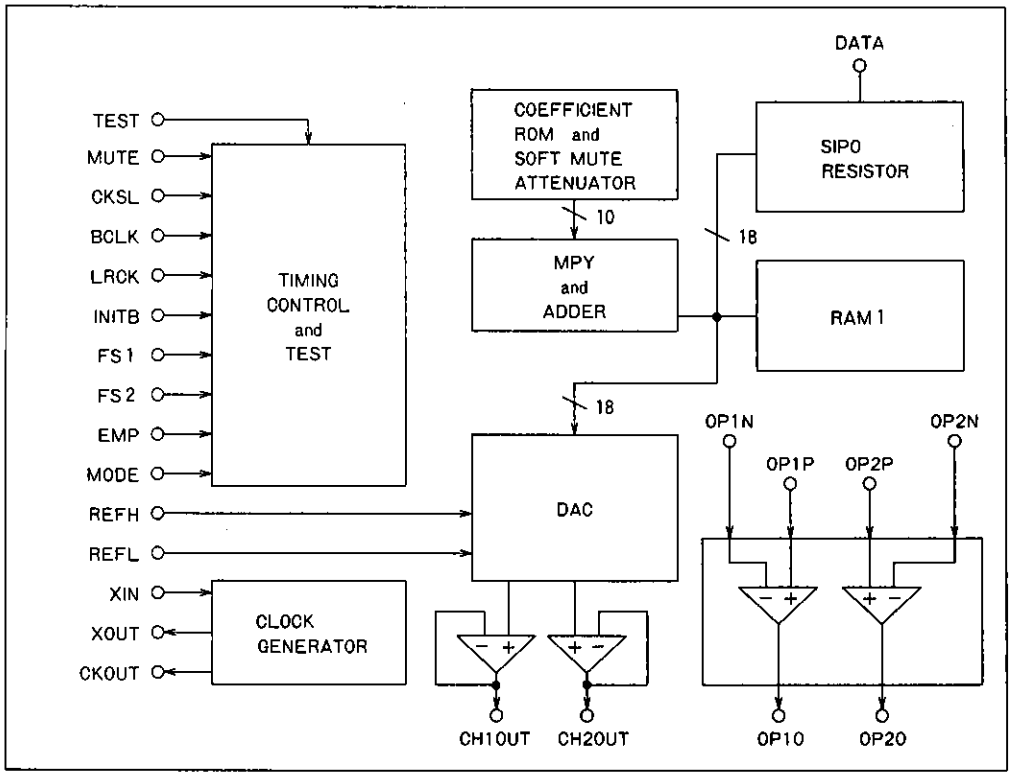
D/A Converter Block



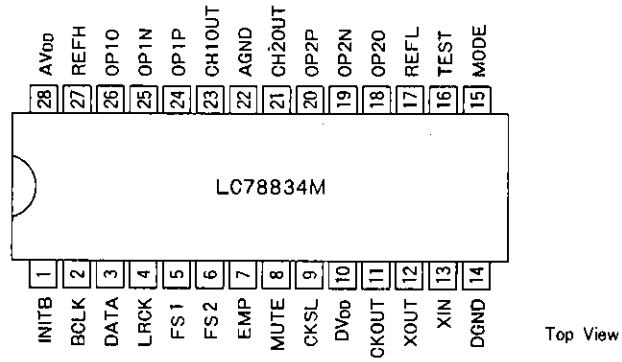
Operational Amplifier Block



Block Diagram



Pin Assignment



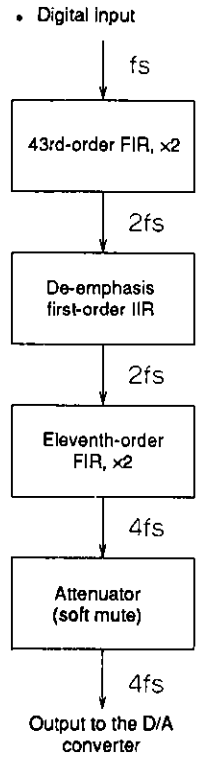
Top View

Pin Functions

Pin No.	Symbol	Function
1	INITB	Initialization signal input. The LC78834M is initialized on a low input.
2	BCLK	Bit clock input
3	DATA	Digital audio data input Data is input in a two's complement MSB first format.
4	LRCK	LR clock input High: CH1 input; Low: CH2 input
5	FS1	De-emphasis filter 32, 44.1, or 48 kHz mode selection FS1: L H H L FS2: L L H H fs: 44.1 kHz / 32 kHz / 48 kHz
6	FS2	
7	EMP	De-emphasis filter on/off switching High: on; Low: off.
8	MUTE	Mute signal input High: Soft muting on.
9	CKSL	System clock selection High: 512 fs; Low: 384 fs
10	DV_{DD}	Digital system power supply
11	CKOUT	Clock output
12	XOUT	Crystal oscillator output (system clock output)
13	XIN	Crystal oscillator input (system clock input)
14	DGND	Digital system ground
15	MODE	Digital audio data format selection High: 16-bit data input Low: 16-bit data input See section 4., "Digital Audio Data Input", page 8.
16	TEST	Test. Connect to DGND in normal operation.
17	REFL	Low-level reference voltage Normally connected to AGND through a capacitor.
18	OP2O	Op amp 2 output
19	OP2N	Op amp 2 inverting input
20	OP2P	Op amp 2 non-inverting input
21	CH2OUT	CH2 analog output
22	AGND	Analog system ground
23	CH1OUT	CH1 analog output
24	OP1P	Op amp 1 non-inverting input
25	OP1N	Op amp 1 inverting input
26	OP1O	Op amp 1 output
27	REFH	High-level reference voltage Normally connected to AGND through a capacitor.
28	AV_{DD}	Analog system ground

LC78834M Operation

1. Digital Filters
   The LC78834M performs the following processing.



- Oversampling
  Two 2× interpolation filters (constructed as FIR filters) are cascade connected.
  Two FIR filter stages, a 43rd order and an eleventh order, are cascade connected to perform 4× oversampling.
- De-emphasis
  A first-order IIR filter is used for digital de-emphasis.
  The filter coefficients are set up to correspond to the sampling frequency fs, which may be 32, 44.1, or 48 kHz.
  See page 11 for the filter characteristics when de-emphasis is on.
  — De-emphasis on/off
  De-emphasis on: EMP pin = high
  De-emphasis off: EMP pin = low
  — Filter coefficient selection

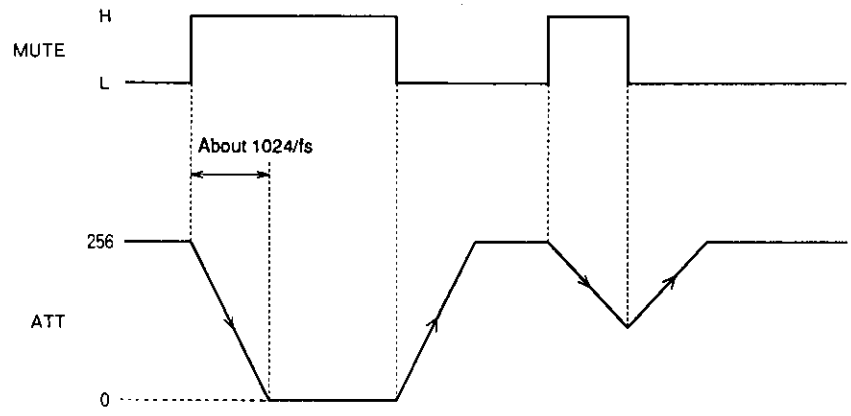
FS1	L	H	H	L
FS2	L	L	H	H
fs	44.1 kHz		32 kHz	48 kHz

- Soft mute

The soft muting function uses the built-in digital attenuator.
The following formula gives the attenuation.

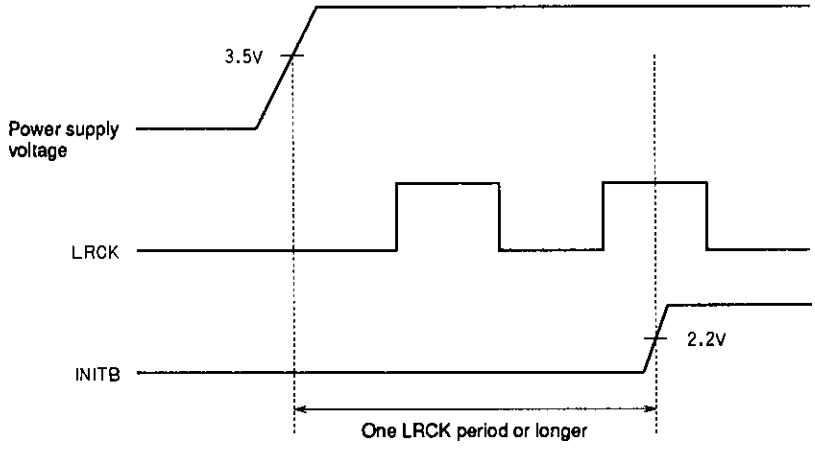
$20 \cdot \log (ATT/256)$ dB

The ATT parameter is an integer between 0 and 256. However, note that the attenuation will be $-\infty$ when ATT is zero.
When the MUTE pin is set to the high level, one is subtracted from the ATT parameter repeatedly moving it towards zero thus changing the attenuation towards $-\infty$. Inversely, when the MUTE pin is set to the high level, one is added to the ATT parameter repeatedly moving it towards 256 thus changing the attenuation towards unity. The time required for the soft mute function to operate is about 1024/fs.



2. Initialization

The LC78834M must be initialized when power is first applied and when the system clock is switched.
The LC78834M is initialized by setting the INITB pin to the low level. The required length of this initial low level period is defined as follows. Once the power supply has stabilized, input the XIN, BCLK and LRCK signals. The low level on the INITB pin must be held until at least one full cycle of the LRCK signal has completed, as shown in the figure.



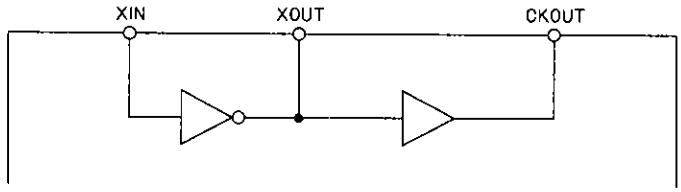
3. System Clock

The LC78834M can handle two system clocks types: either a 384 fs clock or a 512 fs clock.
The CKSL pin selects which clock type is used.

CKSL	System Clock
L	384 fs
H	512 fs

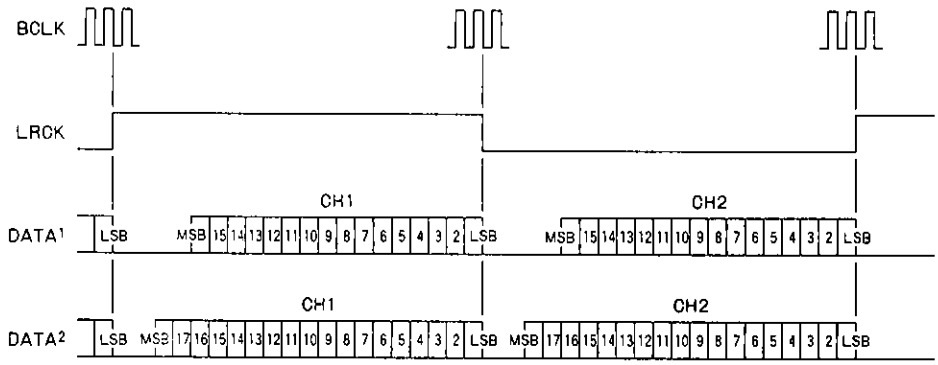
- CKOUT pin

The CKOUT pin is a system clock output pin.



4. Digital Audio Data Input

Digital audio data is a 16- or 18-bit serial signal in a two's complement MSB first format. The 16- or 18-bit serial data is input from the DATA pin to an internal register on the rising edge of the BCLK signal, and that register is read in on the rising and falling edges of the LRCK signal.



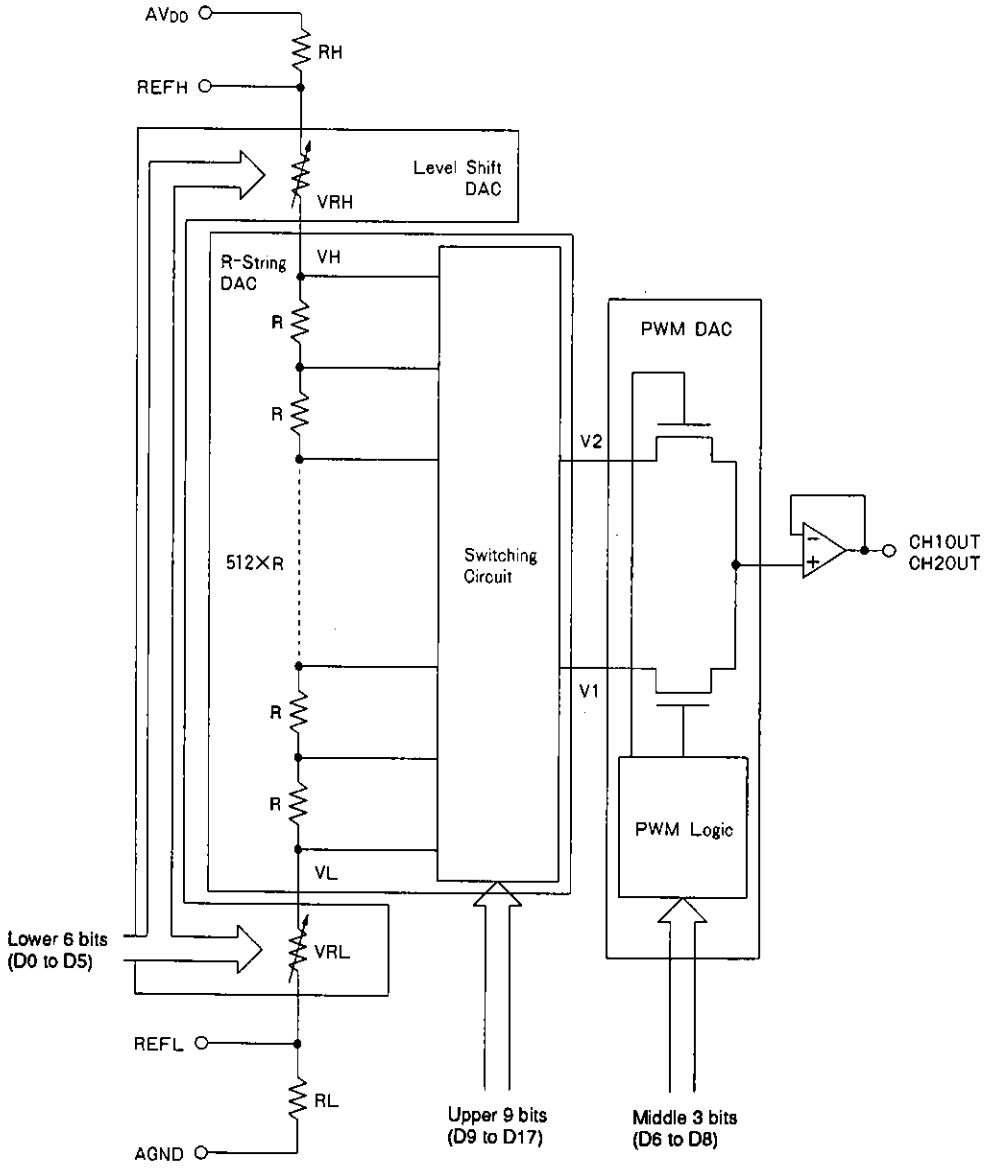
Digital Audio Data Input Timing

Note: When the MODE pin is low, DATA1 is read in, and when high, DATA2.

5. D/A Converter Block

The LC78834M incorporates two independent 18-bit D/A converters, one each for channel 1 and channel 2, as well as two output op amps.

These D/A converters are based on a dynamic level shifting conversion scheme which combines resistor string D/A conversion (R-string DAC), PWM (pulse width modulation) D/A conversion (PWM DAC), and level shifting D/A conversion (level shift DAC) as shown in the figure.



- R-string DAC

  The R-string DAC is a 9-bit D/A converter that consists of 512 (= 2^9) individual resistors (each with resistance R) connected in series that divide the voltage applied at the ends of that resistor string into 512 equal sections. Two adjacent potentials, V1 and V2, of the voltage divided potentials, are selected by a switching circuit according to the upper 9 bits of the data (D9 to D15). These two potentials are output to the PWM DAC. Note that V2 – V1 will be equal to (VH – VL)/512.

- PWM DAC

  The PWM DAC is a 3-bit D/A converter that divides the span of the two potentials V1 and V2 output from the R-string DAC by eight. This circuit outputs one or the other of the two potentials V1 and V2 from the CH1OUT (or CH2OUT) pin depending on the value of the middle three bits (D6 to D8) of the data.

- Level-shift DAC

  The level-shift DAC is a 6-bit D/A converter that consists of two variable resistors, VRH and VRL, inserted in series at the ends of the R-string DAC resistor string. The level-shift DAC controls the VRH and VRL variable resistors according to the lower six bits of the data (D0 to D5) as follows.

  — The sum of the resistances of VRH and VRL is held constant for all values of the data.

  — The values of VRH and VRL are set to be between 0 and 63 times R/512 according to the value of the data. (Here, R is the value of the resistance of the individual resistors in the R-string DAC.)

  This changes the values of the R-string DAC outputs V1 and V2 in the range 0 to 63 × ΔV/512 (where ΔV = (VH – VL)/512) in steps of ΔV/512.

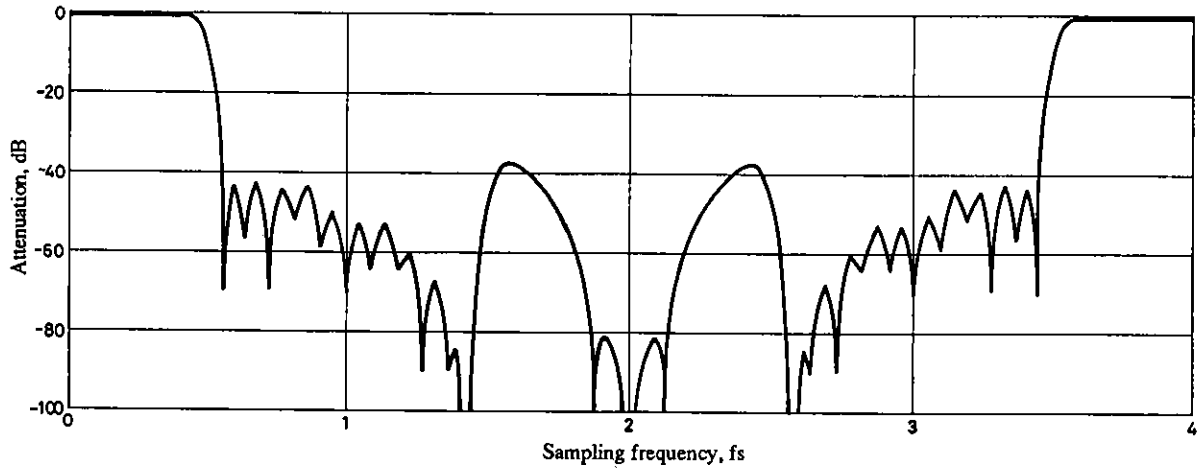
- Reference resistors RH and RL

  Capacitors (about 10 μF) must be connected between REFH and AGND and between REFL and AGND.
  When AV_{DD} = 5.0 V and AGND = 0 V, the LC78834M's maximum output amplitude should be set to be the range 1.3 to 3.7 V (2.4 Vp-p) for a 0 dB playback level by the resistors RH and RL.

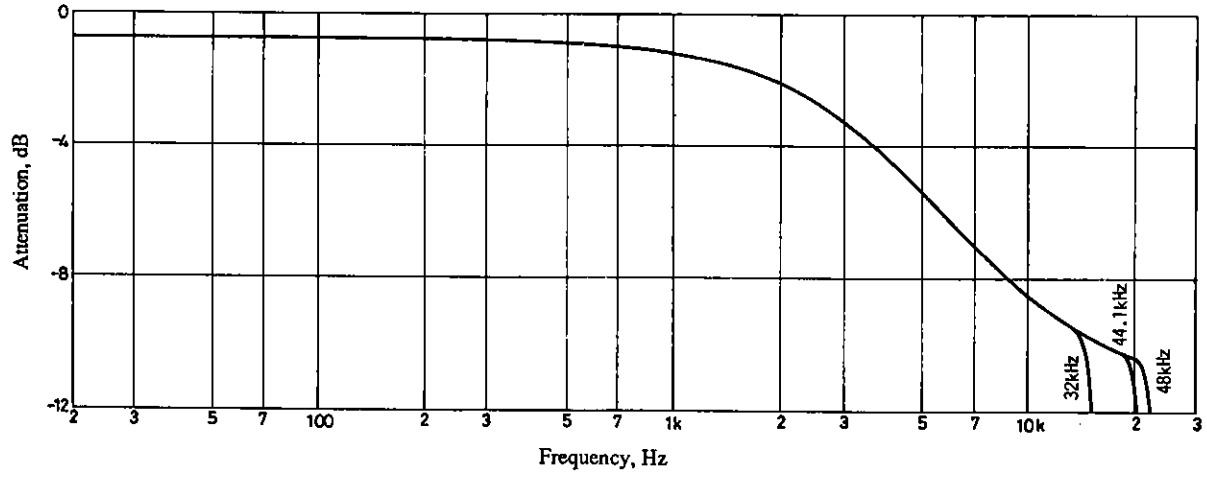
Filter Characteristics

4× oversampling
Ripple: Within ±0.05 dB
Attenuation: Not more than –35 dB

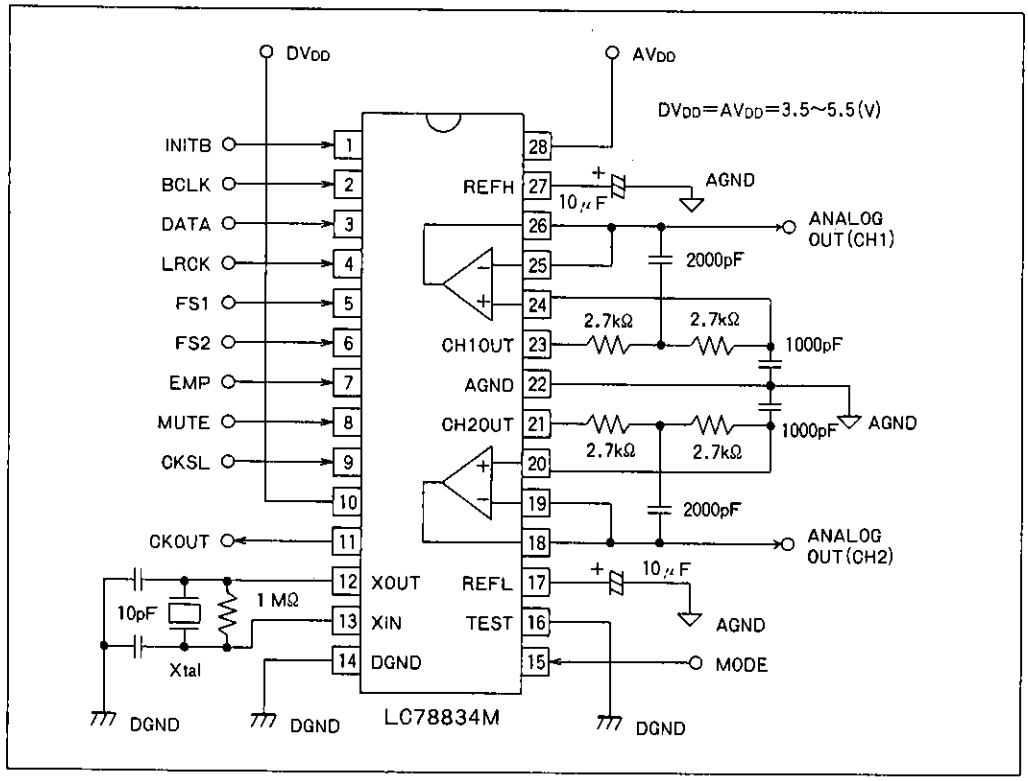
1. De-emphasis



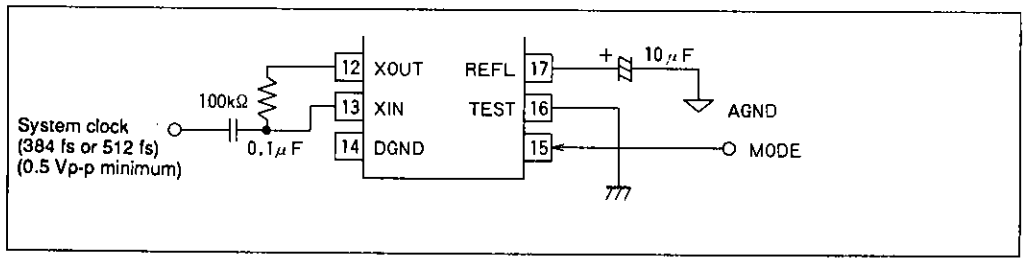
2. De-emphasis On Pass Band Characteristics



Application Circuit Example



External System Clock Supply Circuit



Notes:
1. The nodes marked DV_{DD} and DGND must be connected to the digital system power supply, and the nodes marked AV_{DD} and AGND must be connected to the analog system power supply.
2. TA low-impedance high-stability power supply (equivalent to a commercial three-terminal regulator) must be used for AV_{DD}.
3. Since it is possible for latchup to occur if the pin 10 (DV_{DD}) and the pin 28 (AV_{DD}) power supply rise timings differ, the pin 10 and pin 28 power supply application circuit must be designed so that no time differential occurs.
4. After power is applied, the XIN pin clock signal must be provided promptly. If the XIN pin is held fixed (at low or high) after power is supplied, the IC may be destroyed.

Power Application Timing

1. The analog power supply (AV_{DD}) and the digital power supply (DV_{DD}) must be brought up at the same time and must be turned off at the same time.
2. If a time difference occurs between the analog and digital power supplies, design the circuit to meet the following conditions.
   - The power supply rise and fall times must be less than 3 ms apart as shown in Figure 1.
   - If the time difference is over 3 ms, then allocate 5 ms or over as the rise or fall time of the power supply that rises or falls first respectively. Furthermore, the time difference must be under 50 ms.

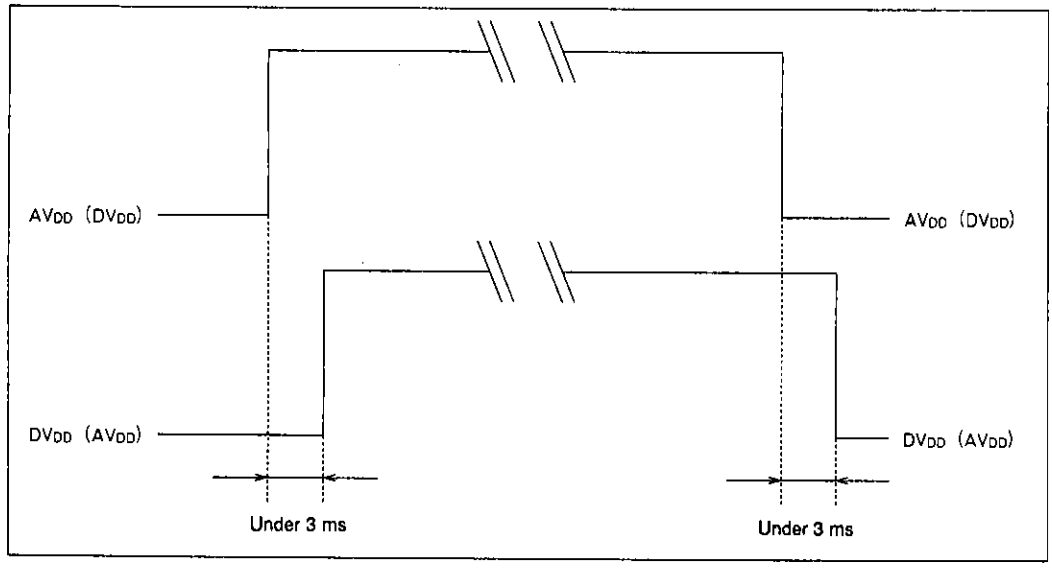


Figure 1

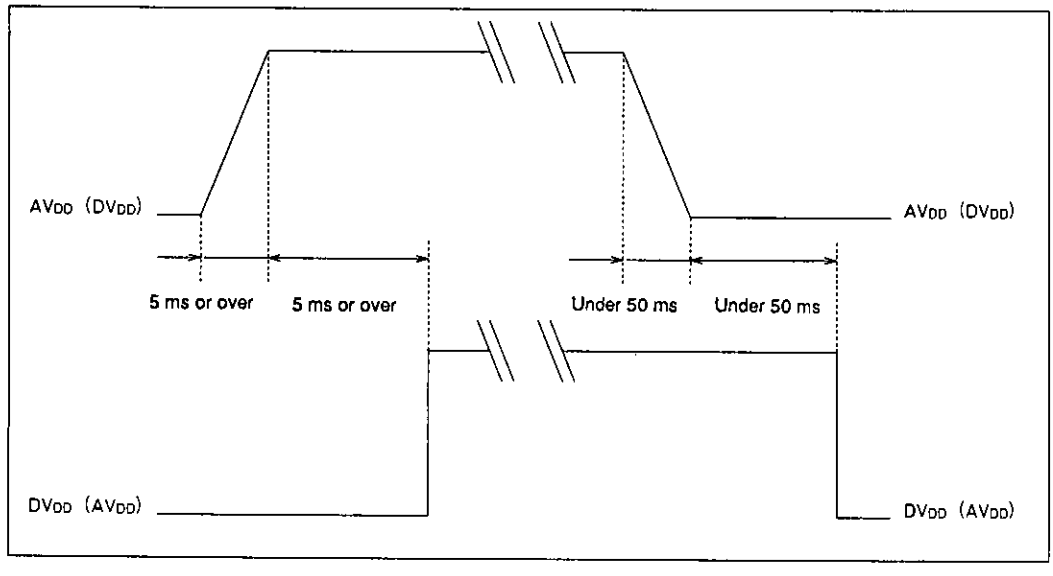


Figure 2