Integrated Circuit Systems, Inc.

ICS952802
Advance Information

Programmable Timing Control Hub™ for P4™ processor

Recommended Application:

SiS755/760 style chipset for AMD K8 Processor

Output Features:

- 2 - Pairs of differential push-pull K8CPU outputs
- 10 - PCICLK @ 3.3V
- 2 - AGPCLK @ 3.3V
- 3 - REF @ 3.3V
- 2 - ZCLK @ 3.3V
- 1 - 24_48MHz @ 3.3V
- 1 - 12_48MHz @ 3.3V
- 1 - PCI_12MHz @ 3.3V

Key Specifications:

- CPU Output Jitter <250ps
- AGP Output Jitter <250ps

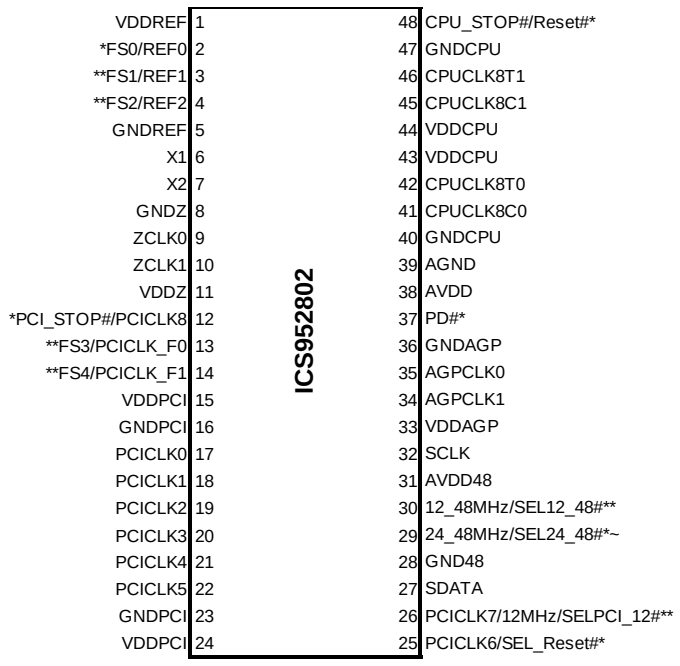
Features/Benefits:

- Selectable synchronous/asynchronous AGP/PCI/ZCLK frequency
- Linear Programmable output frequency.
- Programmable output divider ratios.
- Programmable output rise/fall time.
- Programmable output skew.
- Programmable spread percentage for EMI control.
- Watchdog timer technology and system reset function
- Programmable watch dog safe frequency.
- Support I2C Index read/write and block read/write operations.
- Uses external 14.318MHz reference input.

Functionality

Bit4	Bit3	Bit2	Bit1	Bit0	CPU	ZCLK	AGP	PCI
FS4	FS3	FS2	FS1	FS0	MHz	MHz	MHz	MHz
0	0	0	0	0	160.00	106.66	53.33	26.66
0	0	0	0	1	200.00	133.33	66.67	33.33
0	0	0	1	0	200.00	133.33	66.67	33.33
0	0	0	1	1	200.00	160.00	66.67	33.33
0	0	1	0	0	186.66	106.67	53.33	26.66
0	0	1	0	1	233.33	133.33	66.67	33.33
0	0	1	1	0	233.33	133.33	66.67	33.33
0	0	1	1	1	233.33	155.55	66.67	33.33
0	1	0	0	0	213.34	106.66	53.33	26.66
0	1	0	0	1	266.67	133.33	66.67	33.33
0	1	0	1	0	266.67	133.33	66.67	33.33
0	1	0	1	1	266.67	160.00	66.67	33.33
0	1	1	0	0	133.34	106.66	53.33	26.66
0	1	1	0	1	166.67	133.33	66.67	33.33
0	1	1	1	0	166.67	133.33	66.67	33.33
0	1	1	1	1	166.67	166.66	66.67	33.33
1	0	0	0	0	206.00	137.33	68.67	34.33
1	0	0	0	1	210.00	140.00	70.00	35.00
1	0	0	1	0	202.00	134.66	67.33	33.66
1	0	0	1	1	202.00	161.60	67.33	33.66
1	0	1	0	0	240.33	137.33	68.67	34.33
1	0	1	0	1	245.00	140.00	70.00	35.00
1	0	1	1	0	235.66	134.67	67.33	33.66
1	0	1	1	1	235.66	157.11	67.33	33.66
1	1	0	0	0	106.66	106.66	53.33	26.66
1	1	0	0	1	133.33	133.33	66.67	33.33
1	1	0	1	0	133.33	133.33	66.67	33.33
1	1	0	1	1	133.33	177.77	66.67	33.33
1	1	1	0	0	171.67	137.33	68.67	34.33
1	1	1	0	1	175.00	140.00	70.00	35.00
1	1	1	1	0	168.34	134.66	67.33	33.66
1	1	1	1	1	168.34	168.33	67.33	33.66

Pin Configuration



48-SSOP

* Internal Pull-Up Resistor

** Internal Pull-Down Resistor

~ This Output has 1.5X Drive Strength

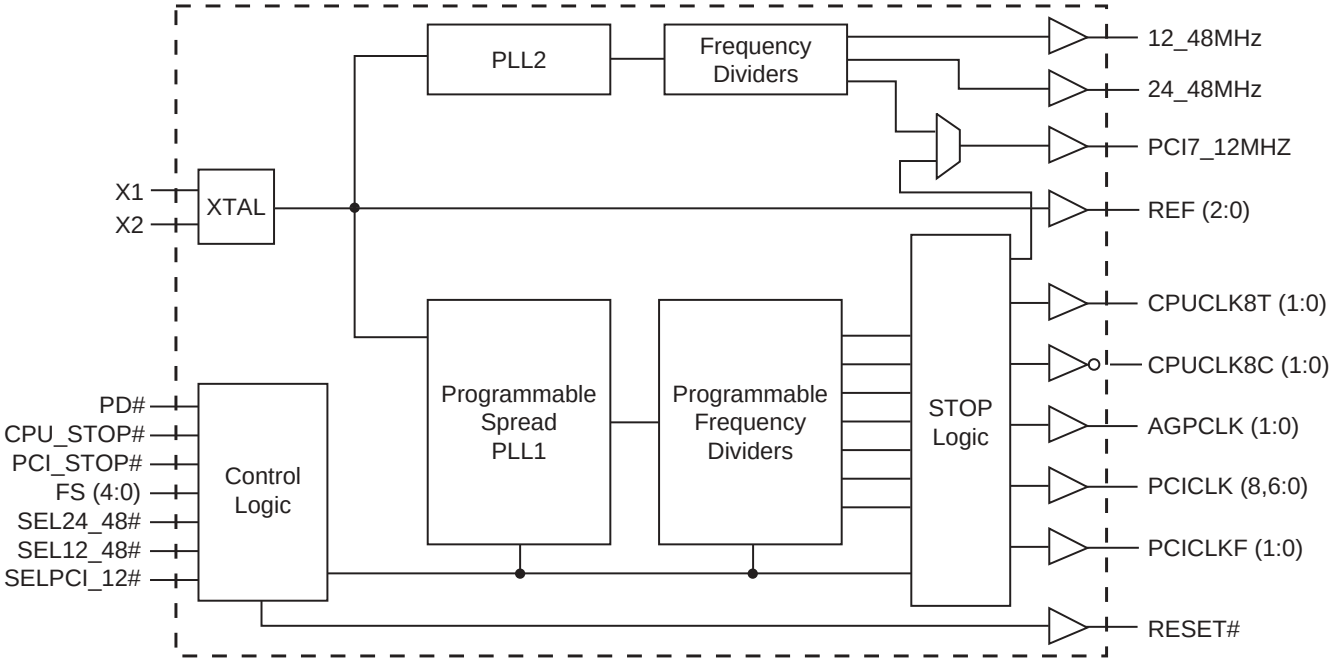
0731—09/18/02

General Description

The **ICS952802** is a two chip clock solution for desktop designs using SIS 755/760 style chipsets. When used with a zero delay buffer such as the ICS9179-16 for PC133 or the ICS93735 for DDR applications it provides all the necessary clocks signals for such a system.

The **ICS952802** is part of a whole new line of ICS clock generators and buffers called TCH™ (Timing Control Hub). ICS is the first to introduce a whole product line which offers full programmability and flexibility on a single clock device. Employing the use of a serially programmable I^2C interface, this device can adjust the output clocks by configuring the frequency setting, the output divider ratios, selecting the ideal spread percentage, the output skew, the output strength, and enabling/disabling each individual output clock. TCH also incorporates ICS's Watchdog Timer technology and a reset feature to provide a safe setting under unstable system conditions. M/N control can configure output frequency with resolution up to 0.1MHz increment.

Block Diagram



Pin Description

PIN #	PIN NAME	PIN TYPE	DESCRIPTION
1	VDDREF	PWR	Ref, XTAL power supply, nominal 3.3V
2	*FS0/REF0	I/O	Frequency select latch input pin / 14.318 MHz reference clock.
3	**FS1/REF1	I/O	Frequency select latch input pin / 14.318 MHz reference clock.
4	**FS2/REF2	I/O	Frequency select latch input pin / 14.318 MHz reference clock.
5	GNDREF	PWR	Ground pin for the REF outputs.
6	X1	IN	Crystal input,nominally 14.318MHz.
7	X2	OUT	Crystal output, nominally 14.318MHz.
8	GNDZ	PWR	Ground pin for the ZCLK outputs
9	ZCLK0	OUT	3.3V Hyperzip clock output.
10	ZCLK1	OUT	3.3V Hyperzip clock output.
11	VDDZ	PWR	Power supply for ZCLK clocks, nominal 3.3V
12	*PCI_STOP#/PCICLK8	I/O	Stops all PCICLKs besides the PCICLK_F clocks at logic 0 level, when input low. This input is selected by IIC.
13	**FS3/PCICLK_F0	I/O	Frequency select latch input pin / 3.3V PCI free running clock output.
14	**FS4/PCICLK_F1	I/O	Frequency select latch input pin / 3.3V PCI free running clock output.
15	VDDPCI	PWR	Power supply for PCI clocks, nominal 3.3V
16	GNDPCI	PWR	Ground pin for the PCI outputs
17	PCICLK0	OUT	PCI clock output.
18	PCICLK1	OUT	PCI clock output.
19	PCICLK2	OUT	PCI clock output.
20	PCICLK3	OUT	PCI clock output.
21	PCICLK4	OUT	PCI clock output.
22	PCICLK5	OUT	PCI clock output.
23	GNDPCI	PWR	Ground pin for the PCI outputs
24	VDDPCI	PWR	Power supply for PCI clocks, nominal 3.3V
25	PCICLK6/SEL_Reset#*	I/O	PCI clock output / Latch input pin to select pin 48 function; 0 = Reset#. 1 = CPU_Stop#
26	PCICLK7/12MHz/SELPCI_12#**	I/O	PCICLK/12MHz clock output / Latched select input for PCI/12MHz output. 0 = 12MHz, 1 = PCICLK.
27	SDATA	I/O	Data pin for I2C circuitry 5V tolerant
28	GND48	PWR	Ground pin for the 48MHz outputs
29	24_48MHz/SEL24_48#*~	I/O	24/48MHz clock output / Latched select input for 24/48MHz output. 0=48MHz, 1 = 24MHz.
30	12_48MHz/SEL12_48#**	I/O	12/48MHz clock output / Latched select input for 24/48MHz output. 0=48MHz, 1 = 12MHz.
31	AVDD48	PWR	Power for 24/48MHz outputs and fixed PLL core, nominal 3.3V
32	SCLK	IN	Clock pin of I2C circuitry 5V tolerant
33	VDDAGP	PWR	Power supply for AGP clocks, nominal 3.3V
34	AGPCLK1	OUT	AGP clock output
35	AGPCLK0	OUT	AGP clock output
36	GNDAGP	PWR	Ground pin for the AGP outputs
37	PD#*	IN	Asynchronous active low input pin used to power down the device into a low power state. The internal clocks are disabled and the VCO and the crystal are stopped. The latency of the power down will not be greater than 3ms.
38	AVDD	PWR	3.3V Analog Power pin for Core PLL
39	AGND	PWR	Analog Ground pin for Core PLL
40	GNDCPU	PWR	Ground pin for the CPU outputs
41	CPUCLK8C0	OUT	"Complementary" clocks of differential 3.3V push-pull K8 pair.
42	CPUCLK8T0	OUT	"True" clocks of differential 3.3V push-pull K8 pair.
43	VDDCPU	PWR	Supply for CPU clocks, 3.3V nominal
44	VDDCPU	PWR	Supply for CPU clocks, 3.3V nominal
45	CPUCLK8C1	OUT	"Complementary" clocks of differential 3.3V push-pull K8 pair.
46	CPUCLK8T1	OUT	"True" clocks of differential 3.3V push-pull K8 pair.
47	GNDCPU	PWR	Ground pin for the CPU outputs
48	CPU_STOP#/Reset#*	I/O	Slectable real time CPU_Stop# (Input) or Reset# (Output)

* Internal Pull-Up Resistor ** Internal Pull-Down Resistor ~ This Output has 1.5X Drive Strength

General I²C serial interface information for the ICS952802

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D2 (H)
- ICS clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- ICS clock will ***acknowledge***
- Controller (host) sends the data byte count = X
- ICS clock will ***acknowledge***
- Controller (host) starts sending ***Byte N through Byte N + X -1***
  (see Note 2)
- ICS clock will ***acknowledge*** each byte ***one at a time***
- Controller (host) sends a Stop bit

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the write address D2 (H)
- ICS clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- ICS clock will ***acknowledge***
- Controller (host) will send a separate start bit.
- Controller (host) sends the read address D3 (H)
- ICS clock will ***acknowledge***
- ICS clock will send the data byte count = X
- ICS clock sends ***Byte N + X -1***
- ICS clock sends ***Byte 0 through byte X (if $X_{(H)}$ was written to byte 8)***.
- Controller (host) will need to acknowledge each byte
- Controllor (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Write Operation

Controller (Host)			ICS (Slave/Receiver)
T	starT bit		
Slave Address $D2_{(H)}$			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
Data Byte Count = X			
			ACK
Beginning Byte N		X Byte	
			ACK
	O		
	O		O
	O		O
			O
Byte N + X - 1			
			ACK
P	stoP bit		

Index Block Read Operation

Controller (Host)		ICS (Slave/Receiver)	
T	starT bit		
Slave Address $D2_{(H)}$			
WR	WRite		
		ACK	
Beginning Byte = N			
		ACK	
RT	Repeat starT		
Slave Address $D3_{(H)}$			
RD	ReaD		
		ACK	
		Data Byte Count = X	
ACK			
		X Byte	Beginning Byte N
ACK			
			O
	O		O
	O		O
	O		
			Byte N + X - 1
N	Not acknowledge		
P	stoP bit		

Table1: Frequency Selection Table

Bit4	Bit3	Bit2	Bit1	Bit0	CPU	ZCLK	AGP	PCI	Spread
FS4	FS3	FS2	FS1	FS0	MHz	MHz	MHz	MHz	%
0	0	0	0	0	160.00	106.66	53.33	26.66	0.3% Center
0	0	0	0	1	200.00	133.33	66.67	33.33	0-0.5% Down
0	0	0	1	0	200.00	133.33	66.67	33.33	0.3% Center
0	0	0	1	1	200.00	160.00	66.67	33.33	0.3% Center
0	0	1	0	0	186.66	106.67	53.33	26.66	0.3% Center
0	0	1	0	1	233.33	133.33	66.67	33.33	0-0.5% Down
0	0	1	1	0	233.33	133.33	66.67	33.33	0.3% Center
0	0	1	1	1	233.33	155.55	66.67	33.33	0.3% Center
0	1	0	0	0	213.34	106.66	53.33	26.66	0.3% Center
0	1	0	0	1	266.67	133.33	66.67	33.33	0-0.5% Down
0	1	0	1	0	266.67	133.33	66.67	33.33	0.3% Center
0	1	0	1	1	266.67	160.00	66.67	33.33	0.3% Center
0	1	1	0	0	133.34	106.66	53.33	26.66	0.3% Center
0	1	1	0	1	166.67	133.33	66.67	33.33	0-0.5% Down
0	1	1	1	0	166.67	133.33	66.67	33.33	0.3% Center
0	1	1	1	1	166.67	166.66	66.67	33.33	0.3% Center
1	0	0	0	0	206.00	137.33	68.67	34.33	0.3% Center
1	0	0	0	1	210.00	140.00	70.00	35.00	0.3% Center
1	0	0	1	0	202.00	134.66	67.33	33.66	0.3% Center
1	0	0	1	1	202.00	161.60	67.33	33.66	0.3% Center
1	0	1	0	0	240.33	137.33	68.67	34.33	0.3% Center
1	0	1	0	1	245.00	140.00	70.00	35.00	0.3% Center
1	0	1	1	0	235.66	134.67	67.33	33.66	0.3% Center
1	0	1	1	1	235.66	157.11	67.33	33.66	0.3% Center
1	1	0	0	0	106.66	106.66	53.33	26.66	0.3% Center
1	1	0	0	1	133.33	133.33	66.67	33.33	0-0.5% Down
1	1	0	1	0	133.33	133.33	66.67	33.33	0.3% Center
1	1	0	1	1	133.33	177.77	66.67	33.33	0.3% Center
1	1	1	0	0	171.67	137.33	68.67	34.33	0.3% Center
1	1	1	0	1	175.00	140.00	70.00	35.00	0.3% Center
1	1	1	1	0	168.34	134.66	67.33	33.66	0.3% Center
1	1	1	1	1	168.34	168.33	67.33	33.66	0.3% Center

I²C Table: Reserved Register

Byte 0	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Reserved	Reserved	RW	-	-	1
Bit 6	-	Reserved	Reserved	RW	-	-	1
Bit 5		Reserved	Reserved	RW	-	-	1
Bit 4	-	Reserved	Reserved	RW	-	-	1
Bit 3	-	Reserved	Reserved	RW	-	-	1
Bit 2	-	Reserved	Reserved	RW	-	-	1
Bit 1	-	Reserved	Reserved	RW	-	-	1
Bit 0	-	Reserved	Reserved	RW	-	-	0

I²C Table: Revision & Vendor ID Register

Byte 1	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	RID3	REVISION ID	R	-	-	0
Bit 6	-	RID2		R	-	-	0
Bit 5	-	RID1		R	-	-	0
Bit 4	-	RID0		R	-	-	0
Bit 3	-	VID3	VENDOR ID	R	-	-	0
Bit 2	-	VID2		R	-	-	0
Bit 1	-	VID1		R	-	-	0
Bit 0	-	VID0		R	-	-	1

I²C Table: Output Control Register

Byte 2	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	GSR_EN	Gear Shift Reset Enable	RW	Disable	Enable	0
Bit 6	-	PCIFNSEL	PCI_Stop/PCI Select	RW	PCI_Stop#	PCICLK8	1
Bit 5	37	PD#_EN	PD# Pin Control	RW	Disable	Enable	1
Bit 4	30	12_48MHz	Output Control	RW	Disable	Enable	1
Bit 3	29	24_48MHz	Output Control	RW	Disable	Enable	1
Bit 2	4	REF2	Output Control	RW	Disable	Enable	1
Bit 1	3	REF1	Output Control	RW	Disable	Enable	1
Bit 0	2	REF0	Output Control	RW	Disable	Enable	1

I²C Table: Output Control Register

Byte 3	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	34	AGPCLK1	Output Control	RW	Disable	Enable	1
Bit 6	35	AGPCLK0	Output Control	RW	Disable	Enable	1
Bit 5	-	12_48MHz	Output Select	RW	48MHz	12MHz	Latch
Bit 4	-	24_48MHz	Output Select	RW	48MHz	24MHz	Latch
Bit 3	25	PCICLK6	Output Control	RW	Disable	Enable	1
Bit 2	26	PCICLK7/12MHz	Output Control	RW	Disable	Enable	1
Bit 1	12	PCICLK8	Output Control	RW	Disable	Enable	1
Bit 0	-	Reserved	Reserved	RW	-	-	1

I²C Table: Frequency Select Register

Byte 4	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	FS3	Freq Select Bit 3	RW	See Table1: Frequency Selection Table		0
Bit 6	-	FS2	Freq Select Bit 2	RW			0
Bit 5	-	FS1	Freq Select Bit 1	RW			0
Bit 4	-	FS0	Freq Select Bit 0	RW			0
Bit 3	-	FS Source	Frequency HW/IIC Select	RW	Latch Input	IIC	0
Bit 2	-	FS4	Freq Select Bit 4	RW	See Table1		0
Bit 1	-	SS_EN	Spread Enable	RW	OFF	ON	1
Bit 0	-	Outputs	Output Control	RW	Running	Tri-state	0

I²C Table: Read Back Register

Byte 5	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	SEL12_48#RB	SEL Read Back	R	48MHz	12MHz	X
Bit 6	-	SEL24_48#RB	SEL Read Back	R	48MHz	24MHz	X
Bit 5	-	WDHRB	WD Hard Alarm Status Read back	R	Normal	Alarm	X
Bit 4	-	FS4RB	FS4 Read back	R	-	-	X
Bit 3	-	FS3RB	FS3 Read back	R	-	-	X
Bit 2	-	FS2RB	FS2 Read back	R	-	-	X
Bit 1	-	FS1RB	FS1 Read back	R	-	-	X
Bit 0	-	FS0RB	FS0 Read back	R	-	-	X

I²C Table: Output Control Register

Byte 6	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	10	ZCLK_1	Output Control	RW	Disable	Enable	1
Bit 6	9	ZCLK_0	Output Control	RW	Disable	Enable	1
Bit 5	14	PCICLK_F1	PCI_STOP# Control	RW	Stop Disable	Stop Enable	0
Bit 4	13	PCICLK_F0	PCI_STOP# Control	RW	Stop Disable	Stop Enable	0
Bit 3	42/41	CPUCLK8T0/C0	CPU_STOP# Control	RW	Stop Disable	Stop Enable	1
Bit 2	46/45	CPUCLK8T1/C1	CPU_STOP# Control	RW	Stop Disable	Stop Enable	1
Bit 1	42/41	CPUCLK8T0/C0	Output Control	RW	Disable	Enable	1
Bit 0	46/45	CPUCLK8T1/C1	Output Control	RW	Disable	Enable	1

I²C Table: Output Control Register

Byte 7	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	14	PCICLK_F1	Output Control	RW	Disable	Enable	1
Bit 6	13	PCICLK_F0	Output Control	RW	Disable	Enable	1
Bit 5	22	PCICLK5	Output Control	RW	Disable	Enable	1
Bit 4	21	PCICLK4	Output Control	RW	Disable	Enable	1
Bit 3	20	PCICLK3	Output Control	RW	Disable	Enable	1
Bit 2	19	PCICLK2	Output Control	RW	Disable	Enable	1
Bit 1	18	PCICLK1	Output Control	RW	Disable	Enable	1
Bit 0	17	PCICLK0	Output Control	RW	Disable	Enable	1

I²C Table: Byte Count Register

Byte 8	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	BC7	Writing to this register will configure how many bytes will be read back, default is 0F = 15 bytes.	RW	-	-	0
Bit 6	-	BC6		RW	-	-	0
Bit 5	-	BC5		RW	-	-	0
Bit 4	-	BC4		RW	-	-	0
Bit 3	-	BC3		RW	-	-	1
Bit 2	-	BC2		RW	-	-	1
Bit 1	-	BC1		RW	-	-	1
Bit 0	-	BC0		RW	-	-	1

I²C Table: Watchdog Timer Register

Byte 9	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	WD7	These bits represent X*290ms the watchdog timer will wait before it goes to alarm mode. Default is 16 X 290ms =4.64 seconds	RW	-	-	0
Bit 6	-	WD6		RW	-	-	0
Bit 5	-	WD5		RW	-	-	0
Bit 4	-	WD4		RW	-	-	1
Bit 3	-	WD3		RW	-	-	0
Bit 2	-	WD2		RW	-	-	0
Bit 1	-	WD1		RW	-	-	0
Bit 0	-	WD0		RW	-	-	0

I²C Table: VCO Control Select Bit & WD Timer Control Register

Byte 10	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	M/NEN	M/N Programming Enable	RW	Disable	Enable	0
Bit 6	-	WDEN	Watchdog Enable	RW	Disable	Enable	0
Bit 5	-	Reserved	Reserved	RW	-	-	0
Bit 4	-	WD SF4	Writing to these bit will configure the safe frequency as Byte 4 bit 2, (7:4)	RW	-	-	0
Bit 3	-	WD SF3		RW	-	-	0
Bit 2	-	WD SF2		RW	-	-	0
Bit 1	-	WD SF1		RW	-	-	0
Bit 0	-	WD SF0		RW	-	-	1

I²C Table: VCO Frequency Control Register

Byte 11	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	N Div8	N Divider Bit 8	RW	-	-	X
Bit 6	-	M Div6	The decimal representation of M Div (6:0) + 2 is equal to reference divider value. Default at power up = latch-in or Byte 0 Rom table.	RW	-	-	X
Bit 5	-	M Div5		RW	-	-	X
Bit 4	-	M Div4		RW	-	-	X
Bit 3	-	M Div3		RW	-	-	X
Bit 2	-	M Div2		RW	-	-	X
Bit 1	-	M Div1		RW	-	-	X
Bit 0	-	M Div0		RW	-	-	X

I²C Table: VCO Frequency Control Register

Byte 12	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	N Div7	The decimal representation of N Div (8:0) + 8 is equal to VCO divider value. Default at power up = latch-in or Byte 0 Rom table.	RW	-	-	X
Bit 6	-	N Div6		RW	-	-	X
Bit 5	-	N Div5		RW	-	-	X
Bit 4	-	N Div4		RW	-	-	X
Bit 3	-	N Div3		RW	-	-	X
Bit 2	-	N Div2		RW	-	-	X
Bit 1	-	N Div1		RW	-	-	X
Bit 0	-	N Div0		RW	-	-	X

I²C Table: Spread Spectrum Control Register

Byte 13	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	SSP7	These Spread Spectrum bits will program the spread pecentage. It is recommended to use ICS Spread % table for spread programming.	RW	-	-	X
Bit 6	-	SSP6		RW	-	-	X
Bit 5	-	SSP5		RW	-	-	X
Bit 4	-	SSP4		RW	-	-	X
Bit 3	-	SSP3		RW	-	-	X
Bit 2	-	SSP2		RW	-	-	X
Bit 1	-	SSP1		RW	-	-	X
Bit 0	-	SSP0		RW	-	-	X

I²C Table: Spread Spectrum Control Register

Byte 14	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Reserved	Reserved	R	-	-	0
Bit 6	-	Reserved	Reserved	R	-	-	0
Bit 5	-	SSP13	It is recommended to use ICS Spread % Table for Spread Programming	R	-	-	X
Bit 4	-	SSP12		RW	-	-	X
Bit 3	-	SSP11		RW	-	-	X
Bit 2	-	SSP10		RW	-	-	X
Bit 1	-	SSP9		RW	-	-	X
Bit 0	-	SSP8		RW	-	-	X

I²C Table: Output Divider Control Register

Byte 15	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	PCI Div3	PCI divider ratio can be configured via these 4 bits individually.	RW	See Table 2: Divider Ratio Combination Table		X
Bit 6	-	PCI Div2		RW			X
Bit 5	-	PCI Div1		RW			X
Bit 4	-	PCI Div0		RW			X
Bit 3	-	CPU Div3	CPU divider ratio can be configured via these 4 bits individually.	RW	See Table 2: Divider Ratio Combination Table		X
Bit 2	-	CPU Div2		RW			X
Bit 1	-	CPU Div1		RW			X
Bit 0	-	CPU Div0		RW			X

Table2: Divider Ratio Combination Table

	Divider (3:2)								
Divider (1:0)	**Bit**	**00**		**01**		**10**		**11**	**MSB**
			1		**2**		**4**		**8**
	00	0000	**2**	0100	**4**	1000	**8**	1100	**16**
	01	0001	**3**	0101	**6**	1001	**12**	1101	**24**
	10	0010	**5**	0110	**10**	1010	**20**	1110	**40**
	11	0011	**7**	0111	**14**	1011	**28**	1111	**56**
	LSB	Address	Div	Address	Div	Address	Div	Address	Div

I²C Table: Output Divider Control Register

Byte 16	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	AGPDiv3	AGP divider ratio can be configured via these 4 bits individually.	RW	See Table 2: Divider Ratio Combination Table		X
Bit 6	-	AGPDiv2		RW			X
Bit 5	-	AGPDiv1		RW			X
Bit 4	-	AGPDiv0		RW			X
Bit 3	-	ZCLKDiv3	ZCLK divider ratio can be configured via these 4 bits individually.	RW	See Table 2: Divider Ratio Combination Table		X
Bit 2	-	ZCLKDiv2		RW			X
Bit 1	-	ZCLKDiv1		RW			X
Bit 0	-	ZCLKDiv0		RW			X

I²C Table: Output Divider Control Register

Byte 17	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	AGPINV	AGPPhase Invert	RW	Default	Inverse	X
Bit 6	-	ZCLKSDINV	ZCLK Phase Invert	RW	Default	Inverse	X
Bit 5	-	Reserved	Reserved	RW	-	-	X
Bit 4	-	CPUINV	CPU Phase Invert	RW	Default	Inverse	X
Bit 3	-	Reserved	Reserved	RW	-	-	X
Bit 2	-	Reserved	Reserved	RW	-	-	X
Bit 1	-	Reserved	Reserved	RW	-	-	X
Bit 0	-	Reserved	Reserved	RW	-	-	X

I²C Table: Group Skew Control Register

Byte 18	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	CPUSkw1	CPU-CPU Skew Control	RW	See Table 3: 4-Steps Skew Programming Table		1
Bit 6	-	CPUSkw0		RW			1
Bit 5	-	Reserved	Reserved	RW	-	-	0
Bit 4	-	Reserved	Reserved	RW	-	-	0
Bit 3	-	Reserved	Reserved	RW	-	-	0
Bit 2	-	ASYNC3	Async Freq Fix PLL	RW	See Table 4: Asynchronous Frequency Programming Table		0
Bit 1	-	ASYNC1		RW			0
Bit 0	-	ASYNC0		RW			0

Table 3: 4-Steps Skew Programming Table

4 Step	0	1	LSB
0	0ps	250ps	-
1	500ps	750ps	-
MSB	-	-	-

Table 4: Asynchronous Frequency Selection Table

B18 bit2	B18 bit1	B18 bit0	VCO	ZCLK	AGP	PCI
0	0	0	Main PLL	Main PLL	Main PLL	Main PLL
0	0	1	528	Main PLL	66	33
0	1	0	528	Main PLL	75.4	37.7
0	1	1	528	Main PLL	88	44
1	0	0	528	132	Main PLL	Main PLL
1	0	1	528	132	66	33
1	1	0	528	132	75.4	37.7
1	1	1	528	132	88	44

I^2C Table: Group Skew Control Register

Byte 19	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	ZCLKSkw3	CPU-ZCLK Skew Control	RW	16-Steps Skew Control. This byte will advance or delay the skew by 100ps per step		0
Bit 6	-	ZCLKSkw2		RW			0
Bit 5	-	ZCLKSkw1		RW			1
Bit 4	-	ZCLKSkw0		RW			1
Bit 3	-	AGPSkw3	CPU-AGP Skew Control	RW	16-Steps Skew Control. This byte will advance or delay the skew by 100ps per step		0
Bit 2	-	AGPSkw2		RW			0
Bit 1	-	AGPSkw1		RW			1
Bit 0	-	AGPSkw0		RW			1

I^2C Table: Group Skew Control Register

Byte 20	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	PCISkw3	CPU-PCI Skew Control	RW	16-Steps Skew Control. This byte will advance or delay the skew by 100ps per step		0
Bit 6	-	PCISkw2		RW			0
Bit 5	-	PCISkw1		RW			0
Bit 4	-	PCISkw0		RW			0
Bit 3	-	Reserved	Reserved	RW	-	-	0
Bit 2	-	Reserved	Reserved	RW	-	-	0
Bit 1	-	Reserved	Reserved	RW	-	-	0
Bit 0	-	Reserved	Reserved	RW	-	-	0

I²C Table: Slew Rate Control Register

Byte 21	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	24/48Slw1	24/48 Slew Rate Control	RW	-	-	0
Bit 6	-	24/48Slw0		RW	-	-	0
Bit 5	-	AGPSlw1	AGP Slew Rate Control	RW	-	-	0
Bit 4	-	AGPSlw0		RW	-	-	0
Bit 3	-	ZCLKSlw1	ZCLK Slew Rate Control	RW	-	-	0
Bit 2	-	ZCLKSlw0		RW	-	-	0
Bit 1	-	REFSlw1	REF Slew Rate Control	RW	-	-	0
Bit 0	-	REFSlw0		RW	-	-	0

I²C Table: Slew Rate Control Register

Byte 22	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Reserved	Reserved	RW	-	-	0
Bit 6	-	Reserved	Reserved	RW	-	-	0
Bit 5	-	Reserved	Reserved	RW	-	-	0
Bit 4	-	Reserved	Reserved	RW	-	-	0
Bit 3	-	PCI_FSlw1	PCI_F Slew Rate Control	RW	-	-	0
Bit 2	-	PCI_FSlw0		RW	-	-	0
Bit 1	-	PCISlw1	PCI Slew Rate Control	RW	-	-	0
Bit 0	-	PCISlw0		RW	-	-	0

I²C Table: Output Control Register

Byte 23	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Reserved	Reserved	RW	-	-	0
Bit 6	-	Reserved	Reserved	RW	-	-	0
Bit 5	-	Reserved	Reserved	RW	-	-	0
Bit 4	-	Reserved	Reserved	RW	-	-	0
Bit 3	-	Reserved	Reserved	RW	-	-	0
Bit 2	-	Reserved	Reserved	RW	-	-	0
Bit 1	-	Reserved	Reserved	RW	-	-	0
Bit 0	-	Reserved	Reserved	RW	-	-	0

I²C Table: Reserved Register

Byte 24	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Reserved	Reserved	RW	-	-	0
Bit 6	-	Reserved	Reserved	RW	-	-	0
Bit 5	-	Reserved	Reserved	RW	-	-	0
Bit 4	-	Reserved	Reserved	RW	-	-	0
Bit 3	-	Reserved	Reserved	RW	-	-	0
Bit 2	-	Reserved	Reserved	RW	-	-	0
Bit 1	-	Reserved	Reserved	RW	-	-	0
Bit 0	-	Reserved	Reserved	RW	-	-	0

Absolute Maximum Ratings

Core Supply Voltage . . . . . 4.6 V
I/O Supply Voltage 3.6V
Logic Inputs . . . . . GND –0.5 V to V_{DD} +0.5 V
Ambient Operating Temperature . . . . . 0°C to +70°C
Storage Temperature . . . . . –65°C to +150°C
Case Temperature . . . . . 115°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70°C; Supply Voltage V_{DD} = 3.3 V +/-5% (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH}		2		V_{DD} + 0.3	V
Input Low Voltage	V_{IL}		V_{SS} - 0.3		0.8	V
Input High Current	I_{IH}	V_{IN} = V_{DD}			5	mA
Input Low Current	I_{IL1}	V_{IN} = 0 V; Inputs with no pull-up resistors	-5			mA
Input Low Current	I_{IL2}	V_{IN} = 0 V; Inputs with pull-up resistors	-200			mA
Operating Supply Current	$I_{DD(op)}$	C_L = 0 pF; Select @ 100MHz			180	mA
Power Down Supply Current	I_{DDPD}	C_L = 0 pF; With input address to Vdd or GND			40	mA
Input frequency	F_i	V_{DD} = 3.3 V;	11		16	MHz
Input Capacitance[1]	C_{IN}	Logic Inputs			5	pF
	C_{INX}	X1 & X2 pins	27		45	pF
Transition Time[1]	T_{trans}	To 1st crossing of target Freq.			3	ms
Clk Stabilization[1]	T_{STAB}	From V_{DD} = 3.3 V to 1% target Freq.			3	ms
Skew[1]	$T_{CPU-PCI}$	V_T = 1.5 V	1.5		4	ns

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - ZCLK

T_A = 0 - 70°C; V_{DD} = 3.3 V +/-5%; C_L = 10-30 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Frequency	F_{O1}					MHz
Output Impedance	R_{DSP1}[1]	$V_O = V_{DD}*(0.5)$	12		55	Ω
Output High Voltage	V_{OH}[1]	I_{OH} = -1 mA	2.4			V
Output Low Voltage	V_{OL}[1]	I_{OL} = 1 mA			0.55	V
Output High Current	I_{OH}[1]	$V_{OH@MIN}$ = 1.0 V, $V_{OH@MAX}$ = 3.135 V	-33		-33	mA
Output Low Current	I_{OL}[1]	$V_{OL@MIN}$ = 1.95 V, $V_{OL@MAX}$ = 0.4 V	30		38	mA
Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.5		2	ns
Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.5		2	ns
Duty Cycle	d_{t1}[1]	V_T = 1.5 V	45		55	%
Skew	t_{sk1}[1]	V_T = 1.5 V			250	ps
Jitter	$t_{jcyc-cyc}$[1]	V_T = 1.5 V 3V66			250	ps

Electrical Characteristics - AGPCLK, ZCLK

T_A = 0 - 70°C; V_{DD} = 3.3 V +/-5%; C_L = 10-30 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Frequency	F_{O1}					MHz
Output Impedance	R_{DSP1}[1]	$V_O = V_{DD}*(0.5)$	12		55	Ω
Output High Voltage	V_{OH}[1]	I_{OH} = -1 mA	2.4			V
Output Low Voltage	V_{OL}[1]	I_{OL} = 1 mA			0.55	V
Output High Current	I_{OH}[1]	$V_{OH@MIN}$ = 1.0 V, $V_{OH@MAX}$ = 3.135 V	-33		-33	mA
Output Low Current	I_{OL}[1]	$V_{OL@MIN}$ = 1.95 V, $V_{OL@MAX}$ = 0.4 V	30		38	mA
Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.5		2	ns
Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.5		2	ns
Duty Cycle	d_{t1}[1]	V_T = 1.5 V	45		55	%
Skew	t_{sk1}[1]	V_T = 1.5 V			250	ps
Jitter	$t_{jcyc-cyc}$[1]	V_T = 1.5 V 3V66			250	ps

Electrical Characteristics - PCICLK

T_A = 0 - 70°C; V_{DD} = 3.3 V,+/-5%; C_L = 30 pF

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH1}	I_{OH} = -18 mA	2.1			V
Output Low Voltage	V_{OL1}	I_{OL} = 9.4 mA			0.4	V
Output High Current	I_{OH1}	V_{OH} = 2.0 V			-22	mA
Output Low Current	I_{OL1}	V_{OL} = 0.8 V	16		57	mA
Rise Time[1]	t_{r1}	V_{OL} = 0.4 V, V_{OH} = 2.4 V			2	ns
Fall Time[1]	t_{f1}	V_{OH} = 2.4 V, V_{OL} = 0.4 V			2	ns
Duty Cycle[1]	d_{t1}	V_T = 1.5 V	45		55	%
Skew[1]	t_{sk1}	V_T = 1.5 V			500	ps
Jitter	$t_{jcyc-cyc}$[1]	V_T = 1.5 V			500	ps
	t_{jabs1}	V_T = 1.5 V			500	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - 48MHz, 24_48MHz

T_A = 0 - 70°C; V_{DD} = 3.3 V +/-5%; C_L = 10-20 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP1}[1]	$V_O = V_{DD}*(0.5)$	20		60	Ω
Output High Voltage	V_{OH}[1]	I_{OH} = -1 mA	2.4			V
Output Low Voltage	V_{OL}[1]	I_{OL} = 1 mA			0.4	V
Output High Current	I_{OH}[1]	$V_{OH@MIN}$ = 1.0 V	-29			
		$V_{OH@MAX}$ = 3.135 V			-23	mA
Output Low Current	I_{OL}[1]	$V_{OL@MIN}$ = 1.95 V	29			
		$V_{OL@MAX}$ = 0.4 V			27	mA
Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.5		1	ns
Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.5		1	ns
Duty Cycle	d_{t1}[1]	V_T = 1.5 V	45		55	%
Jitter	$t_{jcyc-cyc}$[1]	V_T = 1.5 V			350	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - REF

T_A = 0 - 70°C; V_{DD} = 3.3 V , +/-5%; C_L = 10 - 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH5}	I_{OH} = -12 mA	2.6			V
Output Low Voltage	V_{OL5}	I_{OL} = 9 mA			0.4	V
Output High Current	I_{OH5}	V_{OH} = 2.0 V			-22	mA
Output Low Current	I_{OL5}	V_{OL} = 0.8 V	16			mA
Rise Time[1]	t_{r5}	V_{OL} = 0.4 V, V_{OH} = 2.4 V			4	ns
Fall Time[1]	t_{f5}	V_{OH} = 2.4 V, V_{OL} = 0.4 V			4	ns
Duty Cycle[1]	d_{t5}	V_T = 1.5 V	45		55	%
Jitter[1]	$t_{jcyc-cyc5}$	V_T = 1.5 V			1000	ps
	t_{jabs5}	V_T = 1.5 V			800	ps

Electrical Characteristics - CPUCLK

T_A = 0 - 70º C; V_{DD} = 3.3 V +/-5%; C_L = 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	Z_O	$V_O = V_X$	15		55	Ω
Output High Voltage	V_{OH2B}		1		1.2	V
Output Low Voltage	V_{OL2B}				0.4	V
Output Low Current	I_{OL2B}	V_{OL} = 0.3 V	18			mA
Rise Edge Rate[1]		Measured from 20-80%	2		7	V/ns
Fall Edge Rate[1]		Measured from 80-20%	2		7	V/ns
V_{DIFF}		Differential Voltage, Measured @ the Hammer test load (single-ended measurement)	0.4		2.3	V
DV_{DIFF}		Change in V_{DIFF_DC} magnitude, Measured @ the Hammer test load (single-ended measurement)	-150		150	mV
V_{CM}		Common Mode Voltage, Measured @ the Hammer test load (single-ended measurement)	1.05		1.45	V
DV_{CM}		Change in Common Mode Voltage, Measured @ the Hammer test load (single-ended measurement)	-200		200	mV
Duty Cycle[1]	d_{t2B}	V_T = 50%	45		53	%
Jitter, Cycle-to-cycle[1]	$t_{jcyc-cyc2B}$	$V_T = V_X$	0		200	ps

Notes:

1 - Guaranteed by design, not 100% tested in production.

2 - V_{DIF} specifies the minimum input differential voltages (V_{TR}-V_{CP}) required for switching, where V_{TR} is the "true" input level and V_{CP} is the "complement" input level.

3 - $Vpullup_{(external)}$ = 1.5V, Min = $Vpullup_{(external)}$/2-150mV; Max=($Vpullup_{(external)}$/2)+150mV

Shared Pin Operation - Input/Output Pins

The I/O pins designated by (input/output) serve as dual signal functions to the device. During initial power-up, they act as input pins. The logic level (voltage) that is present on these pins at this time is read and stored into a 5-bit internal data latch. At the end of Power-On reset, (see AC characteristics for timing values), the device changes the mode of operations for these pins to an output function. In this mode the pins produce the specified buffered clocks to external loads.

To program (load) the internal configuration register for these pins, a resistor is connected to either the VDD (logic 1) power supply or the GND (logic 0) voltage potential. A 10 Kilohm (10K) resistor is used to provide both the solid CMOS programming voltage needed during the power-up programming period and to provide an insignificant load on the output clock during the subsequent operating period.

Figure 1 shows a means of implementing this function when a switch or 2 pin header is used. With no jumper is installed the pin will be pulled high. With the jumper in place the pin will be pulled low. If programmability is not necessary, than only a single resistor is necessary. The programming resistors should be located close to the series termination resistor to minimize the current loop area. It is more important to locate the series termination resistor close to the driver than the programming resistor.

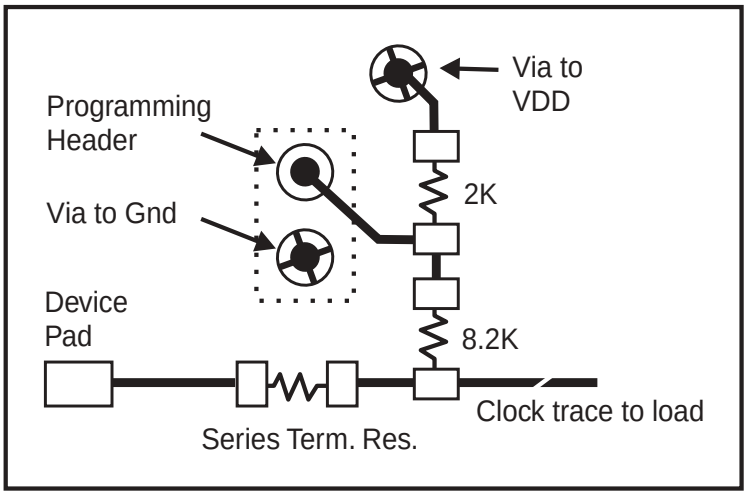
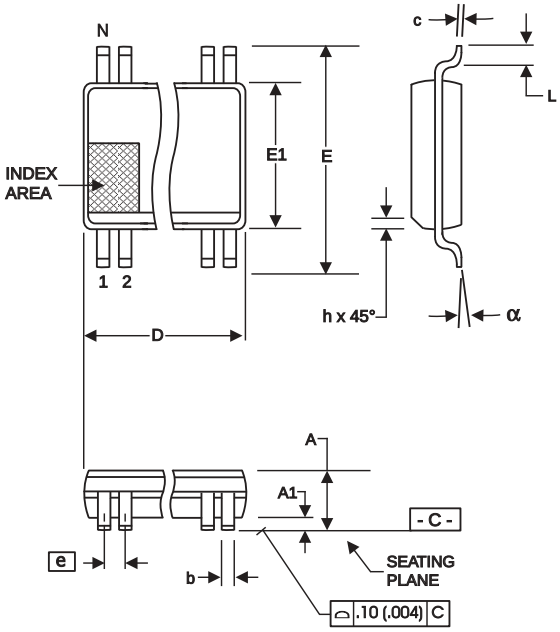


Fig. 1



SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	2.41	2.80	.095	.110
A1	0.20	0.40	.008	.016
b	0.20	0.34	.008	.0135
c	0.13	0.25	.005	.010
D	SEE VARIATIONS		SEE VARIATIONS	
E	10.03	10.68	.395	.420
E1	7.40	7.60	.291	.299
e	0.635 BASIC		0.025 BASIC	
h	0.38	0.64	.015	.025
L	0.50	1.02	.020	.040
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
48	15.75	16.00	.620	.630

Reference Doc.: JEDEC Publication 95, MO-118

10-0034

Ordering Information

ICS952802yFT

Example:

ICS XXXX y **F - T**

- **Designation for tape and reel packaging**
- **Package Type**
  F=SSOP
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type**
- **Prefix**
  ICS = Standard Device

0731—09/18/02