Integrated
Circuit
Systems, Inc.

ICS9158-03

Frequency Generator and Integrated Buffer

General Description

The **ICS9158-03** is a low-cost frequency generator designed specifically for desktop and notebook PC applications. Eight copies of the CPU clock are available.

Each high drive (40mA) output is capable for driving a 30pF load and has a typical duty cycle of 50/50. The clock outputs are skew-controlled to within ±250ps.

The **ICS9158-03** makes a gradual transition between frequencies, so that it meets the Intel cycle-to-cycle timing specification for 486 and Pentium™ systems.

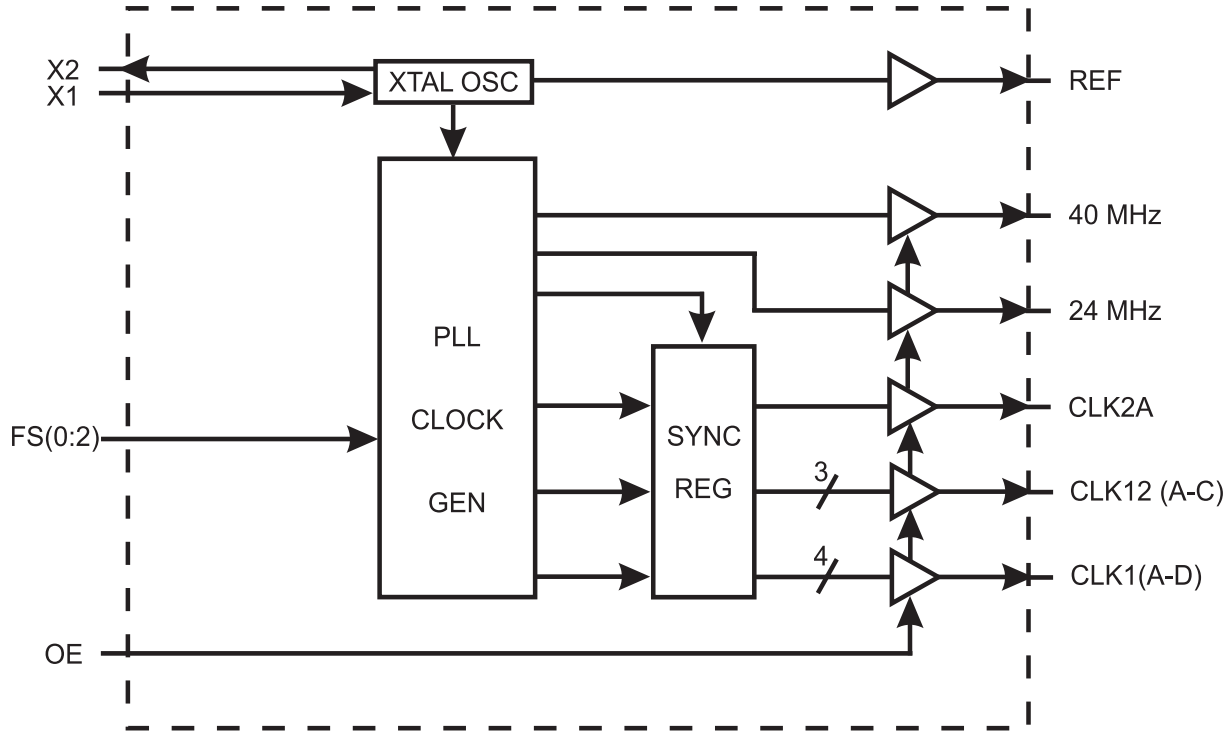
Features

- 8 skew-free, high drive CPU/BUS clocks
- Up to 100 MHz output
- ±250ps skew between all outputs
- Outputs can drive up to 30pF load and 40mA
- 50±10% duty cycle
- Compatible with 486 and Pentium CPUs
- On-chip loop filter components
- 4.5V - 5.5V supply range
- 24-pin SOIC package

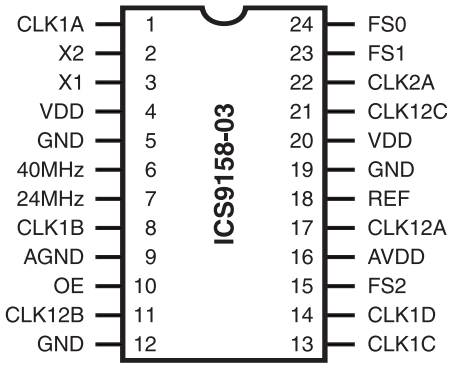
Applications

- Ideal for RISC or CISC systems such as 486, Pentium, PowerPC™, etc. requiring multiple CPU and BUS clocks.

Block Diagram



Pin Configuration



24-Pin SOIC

Functionality

(Assuming 14.318 MHz input.)
VDD=5V±10% or 3.3V±10%, TEMP=0-70°C

FS2	FS1	FS0	CLK2A (MHz)	CLK12(A-C) (MHZ)	CLK1(A-D) (MHz)
0	0	0	32	16	16
0	0	1	32	32	16
0	1	0	32	16	16
0	1	1	32	32	16
1	0	0	50	25	25
1	0	1	50	50	25
1	1	0	66.67	33.33	33.33
1	1	1	60	60	30

Peripheral Clocks

OE	CLK2A	CLK12(A-C)	CLK12(A-D)	40MHz (Pin 6)	24MHz (Pin 7)	REF (Pin 18)
1	Runs	Runs	Runs	39.92	23.95	14.31818
0	Tristate	Tristate	Tristate	Tristate	Tristate	Tristate

Pin Descriptions for ICS9158-03

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	CLK1A	OUT	CLK1A clock output
2	X2	OUT	Crystal connection
3	X1	IN	Crystal connection
4	VDD	PWR	Digital POWER SUPPLY (+5V)
5	GND	PWR	Digital GROUND
6	40 MHz	OUT	40 MHz clock output
7	24 MHz	OUT	24 MHz floppy disk/combination I/O clock output
8	CLK1B	OUT	CLK1B clock output
9	AGND	PWR	ANALOG GROUND
10	OE	IN	OUTPUT ENABLE. Tristates all outputs when low.
11	CLK12B	OUT	CLK12B clock output
12	GND	PWR	Digital GROUND
13	CLK1C	OUT	CLK1C clock output
14	CLK1D	OUT	CLK1D clock output
15	FS2	IN	CPU clock frequency select 2
16	AVDD	PWR	ANALOG power supply (+5V)
17	CLK12A	OUT	CLK12A clock output
18	REF	OUT	14.31818 MHz clock output
19	GND	PWR	Digital GROUND
20	VDD	PWR	Digital POWER SUPPLY (+5V)
21	CLK12C	OUT	2X CPU clock output
22	CLK2A	OUT	CPU clock output
23	FS1	IN	CPU clock frequency select 1
24	FS0	IN	CPU clock frequency select 0

Absolute Maximum Ratings

AVDD, VDD referenced to GND 7V
Operating temperature under bias. . . . . 0°C to +70°C
Storage temperature . . . . . -40°C to +150°C
Voltage on I/O pins referenced to GND. . . . . GND -0.5V to VDD +0.5V
Power dissipation . . . . . 0.5 Watts

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics at 5V

V_{DD} = +5V±10%, T_A=0°C to 70°C unless otherwise stated

DC Characteristics						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage	V_{IL}				0.8	V
Input High Voltage	V_{IH}		2.0			V
Input Low Current	I_{IL}	V_{IN}=0V (Pull-up)	-20			µA
Input High Current	I_{IH}	V_{IN}=V_{DD}	-5		5	µA
Output Low Voltage	V_{OL}	I_{OL}=20.0mA		0.25	0.4	V
Output High Voltage[1]	V_{OH}	I_{OH}=-30mA	2.4	3.5		V
Output Low Current[1]	I_{OL}	V_{OL}=0.8V	45	65		mA
Output High Current[1]	I_{OH}	V_{OH}=2.0V		-55	-35	mA
Supply Current	I_{DD}	No load, 66 MHz		67	100	mA
Output Frequency Change over Supply and Temperature[1]	F_D	With respect to typical frequency		0.002	0.01	%
Short circuit current[1]	I_{SC}	Each output clock	25	56		mA
Pull-up resistor value[1]	R_{PU}	Input pin		680		kΩ
Input Capacitance[1]	C_i	Except X1, X2			8	pf
Load Capacitance[1]	C_L	Pins X1, X2		20		pf

Note 1: Parameter is guaranteed by design and characterization. Not 100% tested in production.

Electrical Characteristics (*continued*)

V_{DD} = +5V±10%, T_A=0°C to 70°C unless otherwise stated

AC Characteristics						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Output Rise time, 0.8 to 2.0V (Note 1)	tr	30pf load	-	1	2.0	ns
Rise time, 20% to 80% VDD (Note 1)	tr	30pf load	-	2.5	3	ns
Output Fall time, 2.0 to 0.8V[1]	tf	30pf load	-	0.5	2.0	ns
Fall time, 80% to 20% VDD[1]	tf	30pf load	-	1.5	3.0	ns
Duty cycle[1]	dt	30pf load	45/55	48/52	55/45	%
Jitter, one sigma[1]	tj1s	As compared with clock period		0.5	2.0	%
Jitter, absolute	tjab		-5	2	5	%
Jitter, absolute	tjab	25-66MHz clocks	-250		250	ps
Input Frequency	fi			14.318		MHz
Clock skew between CLK2A, CLK1(A-D) and CLK12(A-C) outputs	Tsk		-250	100	250	ps
Frequency Transition Time[1]	tft	From 4 to 50 MHz		13	20	ms

Note 1: Parameter is guaranteed by design and characterization. Not 100% tested in production.

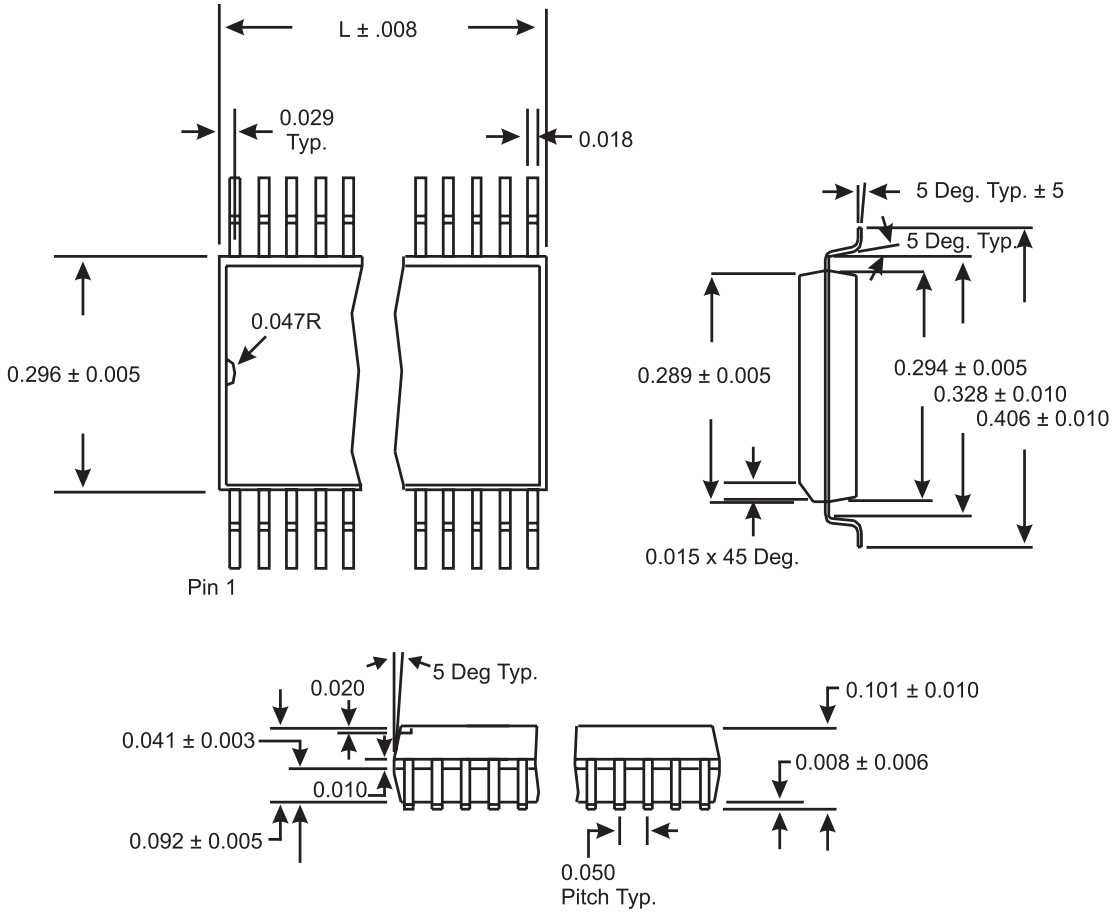
Electrical Characteristics at 3.3V

V_{DD} = +3.3V±10%, T_A=0°C to 70°C unless otherwise stated

DC Characteristics						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage	V_{IL}				0.2 VDD	V
Input High Voltage	V_{IH}		0.7 VDD			V
Input Low Current	I_{IL}	V_{IN}=0V(Pull-up)	-10			µA
Input High Current	I_{IH}	V_{IN}=V_{DD}	-5			µA
Output Low Voltage	V_{OL}	I_{OL}=10mA			0.1V_{DD}	V
Output High Voltage[1]	V_{OH}	I_{OH}=-5mA	0.85V_{DD}			V
Output Low Current[1]	I_{OL}	V_{OL}=0.2V_{DD}	20	30		mA
Output High Current[1]	I_{OH}	V_{OH}=0.7V_{DD}		-15	-10	mA
Supply Current	I_{DD}	No load, 66 MHz		43	70	mA
Output Frequency Change over Supply and Temperature[1]	F_D	With respect to typical frequency		0.002	0.01	%
Short Circuit Current[1]	I_{SC}	Each output clock	25	56		mA
Pull-up Resistor Value[1]	R_{PU}	Input pin		900		kW
Input Capacitance[1]	C_i	Except X1, X2			8	pF
Load Capacitance[1]	C_L	Pins X1, X2		20		pF

AC Characteristics						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Output Rise time, 0.8 to 2.0V[1]	t_r	30pF load	-	1	2.5	ns
Rise time, 20% to 80% V_{DD}[1]	t_r	30pF load	-	2.5	4.0	ns
Output Fall time, 2.0 to 0.8V[1]	t_f	30pF load	-	0.5	2.5	ns
Fall time, 80% to 20% V_{DD}[1]	t_f	30pF load	-	1.5	4.0	ns
Duty cycle[1]	d_t	30pF load	40/50	44/46	50/40	%
Jitter, one sigma[1]	t_{j1s}	As compared with clock period		0.5	2.0	%
Jitter, absolute[1]	t_{jab}			2	5	%
Jitter, absolute[1]	t_{jab}	25-66 MHz clocks			300	ps
Input Frequency	f_i			14.318		MHz
Clock skew window between CLK2A, CLK1(A-D) CPU and CLK12(A-C) outputs[1]	T_{sk}			100	250	ps
Frequency Transition time[1]	t_{ft}	From 4 to 50 MHz		13	20	ms

Note 1: Parameter is guaranteed by design and characterization. Not 100% tested in production.



LEAD COUNT	24L
DIMENSION L	0.604

24 Lead SOIC

Ordering Information

ICS9158-03CW24

Example:

ICS XXXX-PPP W

Package Type
W=(SOIC) 300mil

Pattern Number (2 or 3 digit number for parts with ROM code patterns)
Device Type (consists of 3 or 4 digit numbers)
Prefix
ICS, AV=Standard Device; GSP=Genlock Device