

High Speed, Monolithic Pin Driver

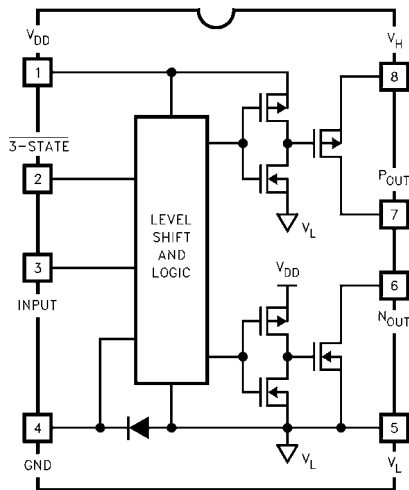


The EL7154 3-state pin driver is particularly well suited for ATE and level shifting applications. The 4A peak drive capability, makes the EL7154 an excellent choice when driving high speed capacitive lines.

The p-channel MOSFET is completely isolated from the power supply, providing a high degree of flexibility. Pin (7) can be grounded, and the output can be taken from pin (8) when a "source follower" output is desired. Then n-channel MOSFET has an isolated drain, but shares a common bus with pre-drivers and level shifter circuits. This is necessary to ensure that the nchannel device can turn off effectively when V_L goes below GND. In some power-FET and IGBT applications, negative drive is desirable to insure effective turn-off. The EL7154 can be used in these applications by returning V_L to a moderate negative potential.

Pinout

EL7154
(8-PIN PDIP, SOIC)
TOP VIEW



Truth Table

3-STATE	INPUT	P _{OUT}	N _{OUT}
0	0	Open	Open
0	1	Open	Open
1	0	HIGH	Open
1	1	Open	LOW

Features

- Comparatively low cost
- 3-State output
- 3V and 5V Input compatible
- Clocking speeds up to 10MHz
- 20ns Switching/delay time
- 4A Peak drive
- Isolated drains
- Low output impedance—2.5Ω
- Low quiescent current—5mA
- Wide operating voltage—4.5V–16V
- Isolated P-channel device
- Separate ground and V_L pins

Applications

- Loaded circuit board testers
- Digital testers
- Level shifting below GND
- IGBT drivers
- CCD drivers

Ordering Information

PART NUMBER	TEMP. RANGE	PACKAGE	PKG. NO.
EL7154CN	-40°C to +85°C	8-Pin PDIP	MDP0031
EL7154CS	-40°C to +85°C	8-Pin SOIC	MDP0027

Nominal Operating Voltage Range

PIN	MIN	MAX
V_L	-3	0
$V_{DD}-V_L$	5	15
V_H-V_L	2	15
$V_{DD}-V_H$	-0.5	15
V_{DD}	5	15

Manufactured under U.S. Patent Nos. 5,334,883, #5,341,047, #5,352,578, #5,352,389, #5,351,012, #5,374,898

EL7154

Absolute Maximum Ratings (T_A = 25°C)

Supply (V _{DD} to V _L ; V _H -V _L , V _H to GND), V ₊ to V _H	16.5V
V _L to GND	-5V
Input Pins	-0.3V below V _L to +0.3V above V _{DD}
Peak Output Current4A

Storage Temperature Range	-65°C to +150°C
Ambient Operating Temperature	-40°C to +85°C
Operating Junction Temperature	125°C
Power Dissipation	
SOIC570mW
PDIP1050mW

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: T_J = T_C = T_A

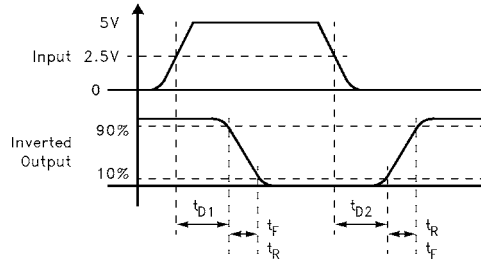
DC Electrical Specifications T_A = 25°C, V_{DD} = +12V, V_H = +12V, V_L = -3V, unless otherwise specified

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN	TYP	MAX	UNITS
INPUT						
V _{IH}	Logic "1" Input Voltage		2.4			V
I _{IH}	Logic "1" Input Current	V _{IH} = V _{DD}		0.1	10	μA
V _{IL}	Logic "0" Input Voltage				0.6	V
I _{IL}	Logic "0" Input Current	V _{IL} = 0V		0.1	10	μA
V _{HVS}	Input Hysteresis			0.3		V
OUTPUT						
R _{OH}	Pull-Up Resistance	I _{OUT} = -100mA		1.5	4	Ω
R _{OL}	Pull-Down Resistance	I _{OUT} = +100mA		2	4	Ω
I _{OUT}	Output Leakage Current	V _{DD} /GND		0.2	10	μA
I _{PK}	Peak Output Current	Source Sink		4.0 4.0		A
I _{DC}	Continuous Output Current	Source/Sink	200			mA
POWER SUPPLY						
I _S	Power Supply Current	Inputs = V _{DD}		1	2.5	mA
V _S	Operating Voltage		4.5		16	V
I _G	Current to GND (Pin 4)			1	10	μA
I _H	Off Leakage at V _H	Pin 8 = 0V		1	10	μA

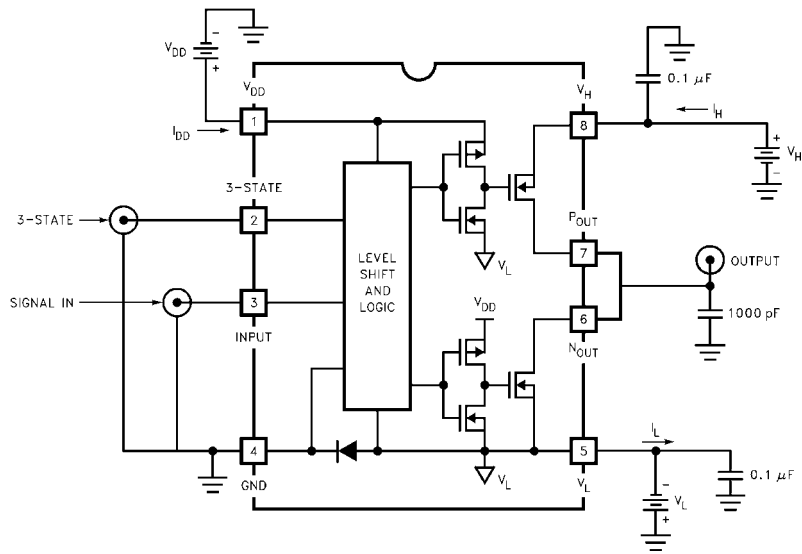
AC Electrical Specifications T_A = 25°C unless otherwise specified

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN	TYP	MAX	UNITS
SWITCHING CHARACTERISTICS (V_{DD} = V_H = 12V; V_L = -3V)						
t _R	Rise Time	C _L = 100pF		4	25	ns
		C _L = 2000pF		20		
t _F	Fall Time	C _L = 100pF		4	25	ns
		C _L = 2000pF		20		
t _{D-1}	Turn-Off Delay Time	C _L = 2000pF		20	25	ns
t _{D-2}	Turn-On Delay Time	C _L = 2000pF		10	25	ns
t _{D-1}	3-State Delay				25	ns
t _{D-2}	3-State Delay				25	ns

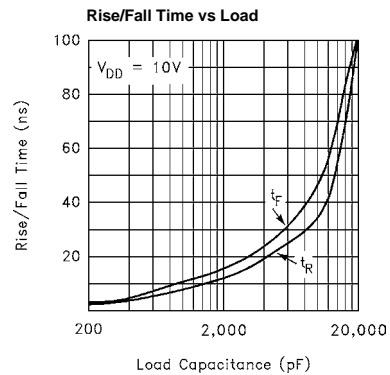
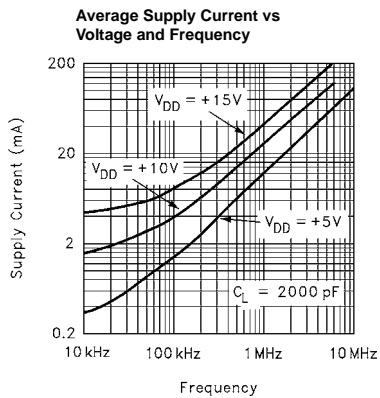
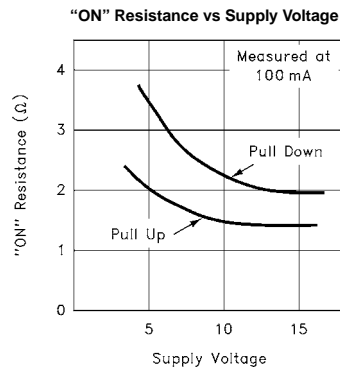
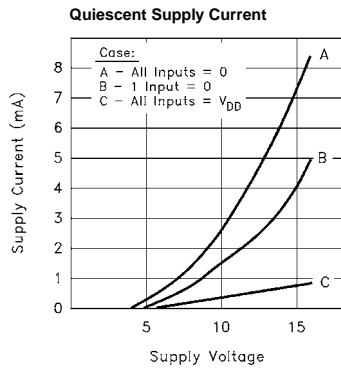
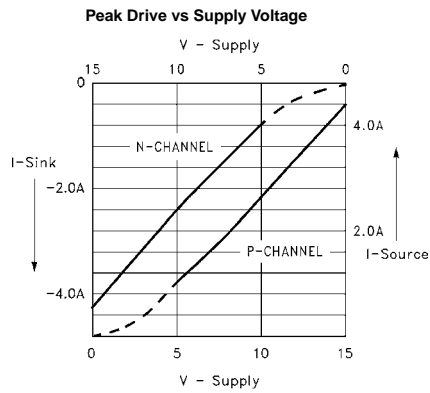
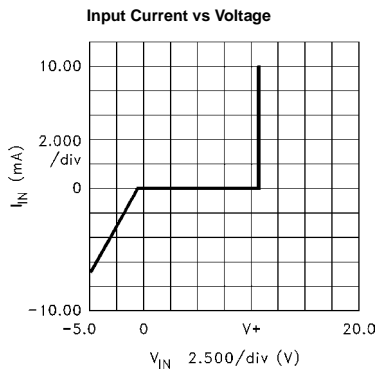
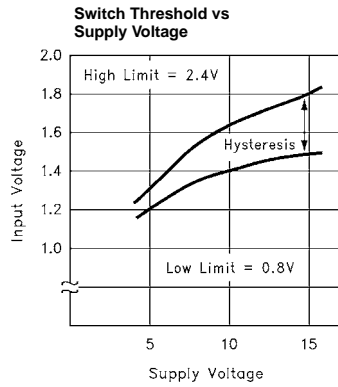
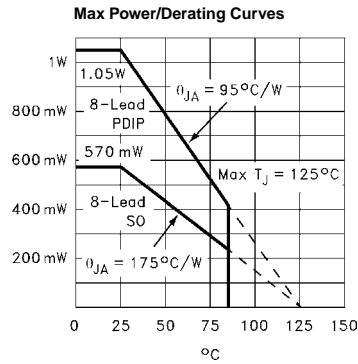
Timing Table



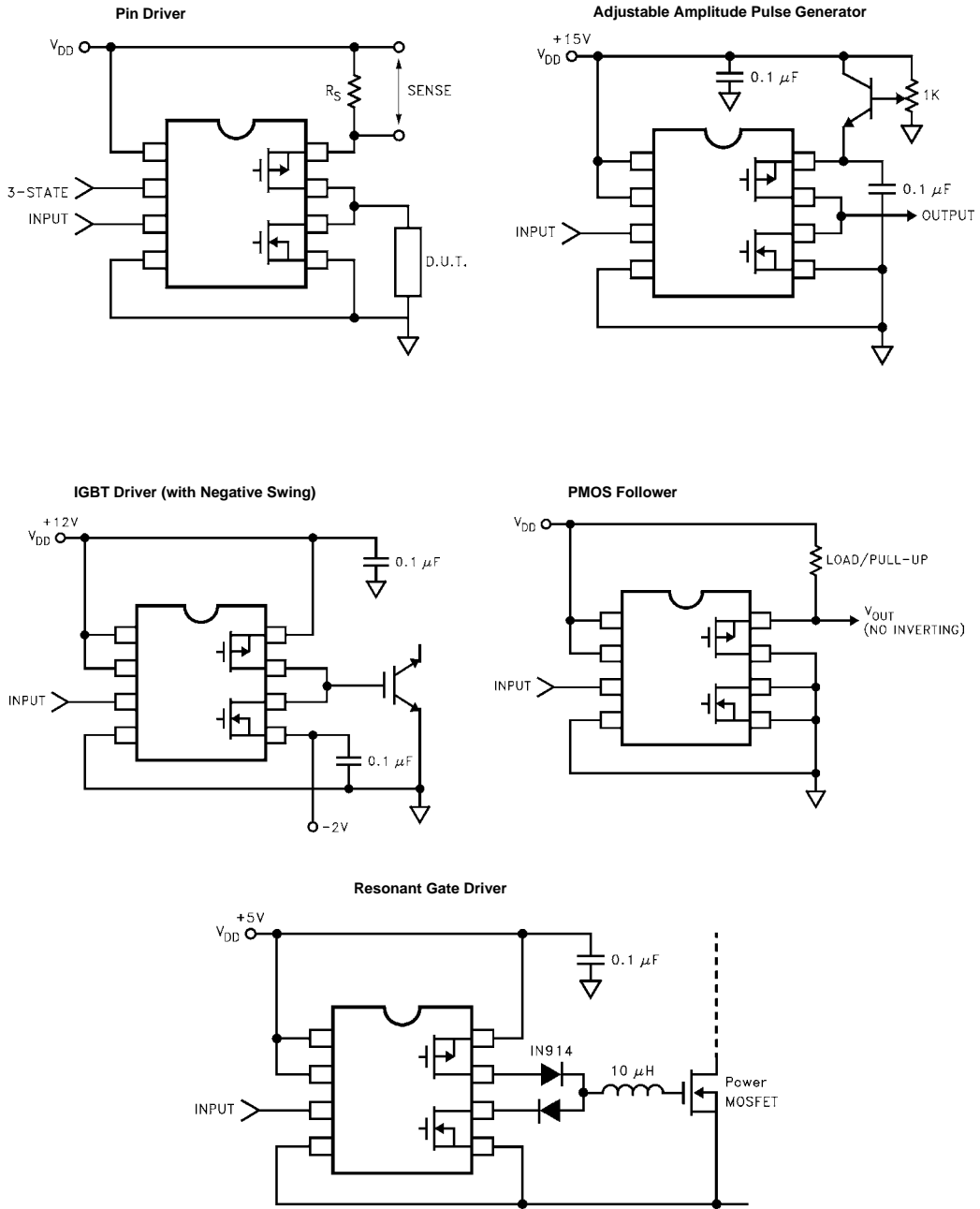
Standard Test Configuration



Typical Performance Curves



Typical Applications



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