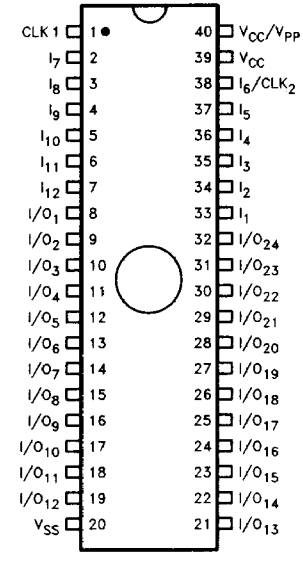
5C121
1200 GATE CHMOS
H-SERIES ERASABLE PROGRAMMABLE LOGIC DEVICE

- **High Performance LSI Semi-Custom Logic Replacement for Gate Arrays and Conventional Fixed Logic**
- **EPROM Technology Based. UV Erasable**
- **Programmable Macrocell and I/O Architecture; up to 36 Inputs or 24 Outputs, 28 Macrocells Including 4 Buried Registers**
- **All Inputs are Latchable with a Programmable Latch Feature**
- **High Speed t_{PD} (Max) 50 ns Operating Frequency (Max) 20 MHz**
- **Low Power; 15 mW Typical Standby Dissipation**
- **Typical Usable Gate Count of 1200 2-Input NAND Gates**
- **Advanced Architecture Features Including Programmable Output Polarity (Active High/Low), Register By-Pass and Reset Controls**
- **Programmable Clock System for Input Latches and Output Registers**
- **Product-Term Sharing and Local Bus Architecture for Optimized Array Performance**
- **Compatible with LS TTL and 74HC CMOS Logic**
- **Register Pre-Load and Erasable Array for 100% Generic Testability**
- **Programmable "Security Bit" allows total protection of proprietary designs**
- **Available in a 40-Lead Window Cerdip Package** (See Packaging Spec Order # 231369)
- **Fully Compatible with EP1210**

The Intel 5C121 H-EPLD (H-series Erasable Programmable Logic Device) is an LSI logic circuit that is user customizable through programming. This device can be used to replace gate arrays, multiple programmable logic arrays and LS TTL and 74HC CMOS SSI and MSI logic devices. The logic capacity of the 5C121 is typically equal to 1200 two-input NAND gates.

Pin Configuration



290098-1

ILLUSTRATIONS COURTESY OF ALTERA CORPORATION.

October 1988
Order Number: 290098-005

The 5C121 H-EPLD uses CHMOS* EPROM (floating gate) cells as logic control elements instead of fuses. Use of Intel's advanced CHMOS II-E EPROM process technology enables greater logic densities to be achieved with superior speed and power performance. The EPROM technology also enables these devices to be 100% factory tested by the programming and the erasure of all the EPROM logic control elements in the device.

The architecture of the 5C121 is based on the 'Sum of Products' PLA (Programmable Logic Array) structure with a programmable AND array feeding into a fixed OR array. Flexibility in accommodating logical functions without the overhead of unnecessary product terms or speed penalties of programmable OR structures is achieved through the provision of a range of OR gate widths as well as through product term sharing. The use of a segmented PLA structure with local and global connectivity allows for further improvements in performance. The 5C121 also contains innovative architectural features that provide extensive Input/Output flexibility.

ARCHITECTURE DESCRIPTION

The 5C121 H-EPLD has 12 dedicated inputs as well as 24 Input/Output pins. All inputs to the circuit (both dedicated and I/O inputs) may be latched using transparent 7475 type latches. In addition to these 36 input latches, 28 D type registers are also provided.

The internal architecture of the 5C121 H-EPLD is based on 28 macrocells. Each macrocell (see Figure 1) contains a PLA structure (programmable AND array product terms connected to an OR gate) and an I/O architecture control block (with a D Flip-Flop) that can be programmed to create many different output logic structures. This powerful I/O architecture can be configured to support both active-high, active-low, 3-state, open drain and bi-directional data ports all on a 4-bit wide basis. They can also act as inputs on a nibble wide basis with optional input latching.

Macrocells in each half of the circuit are grouped together for I/O architecture programming. Each bank of four macrocells can be further programmed on an individual macrocell basis to generate active high or active low outputs of the logic function from the PLA.

The primary logic array of the 5C121 is segmented into two symmetrical halves that communicate via global bus signals. The main array contains some 15104 programmable elements representing 236 product terms (AND gates) each containing 64 input signals.

The macrocells share a common programmable clock system (described in a later section) that controls clocking of all registers and input latches. The device contains 8 modes of clock operation that allow logic transition to take place on either rising or falling edges of the clock signals.

The device also contains four macrocells whose outputs are not tied to any I/O pin but feed back into the array to create buried state-functions. The feedback path may be either the registered or combinational result of the PLA output. The use of the buried state macrocells provides maximum equivalent logic density without demanding higher pin-count packages that consume valuable board space.

MACROCELL I/O ARCHITECTURE

The Input/Output architecture of the 5C121 macrocell (see Figure 1) can be programmed using both static and dynamic controls. The static controls remain fixed after the device is programmed whereas the dynamic controls may change state as a result of the signals applied to the device.

The static controls set the inversion logic (i), register by-pass (ii) and input feedback multiplexers (iii). In the latter two cases these controls operate on four macrocells as a bank.

The buried-state registers have simpler controls that determine if the feedback is to be registered or combinational.

The inversion control logic, marked (i) in Figure 1, is achieved by programming the EPROM control bit connected to the same XOR gate as the output from the PLA structure. Programming or erasure of this EPROM element toggles the OR gate output of the PLA between active-high and active-low. The inversion control operates on an individual macrocell basis.

The register by-pass control, marked (ii) in Figure 1 allows the PLA output to either flow through the D Flip-Flop as a registered output or by-pass the Flip-Flop and be a combinational output.

The dynamic controls consist of a programmable input latch-enable as well as reset and output enable product terms. The latch-enable function is common throughout the 5C121 and once chosen, will latch all the inputs. This function is programmed by the clock control block but may also be driven by input signals applied to pin 1 (see clock modes—Table 1).

*CHMOS is a patented process of Intel Corporation.

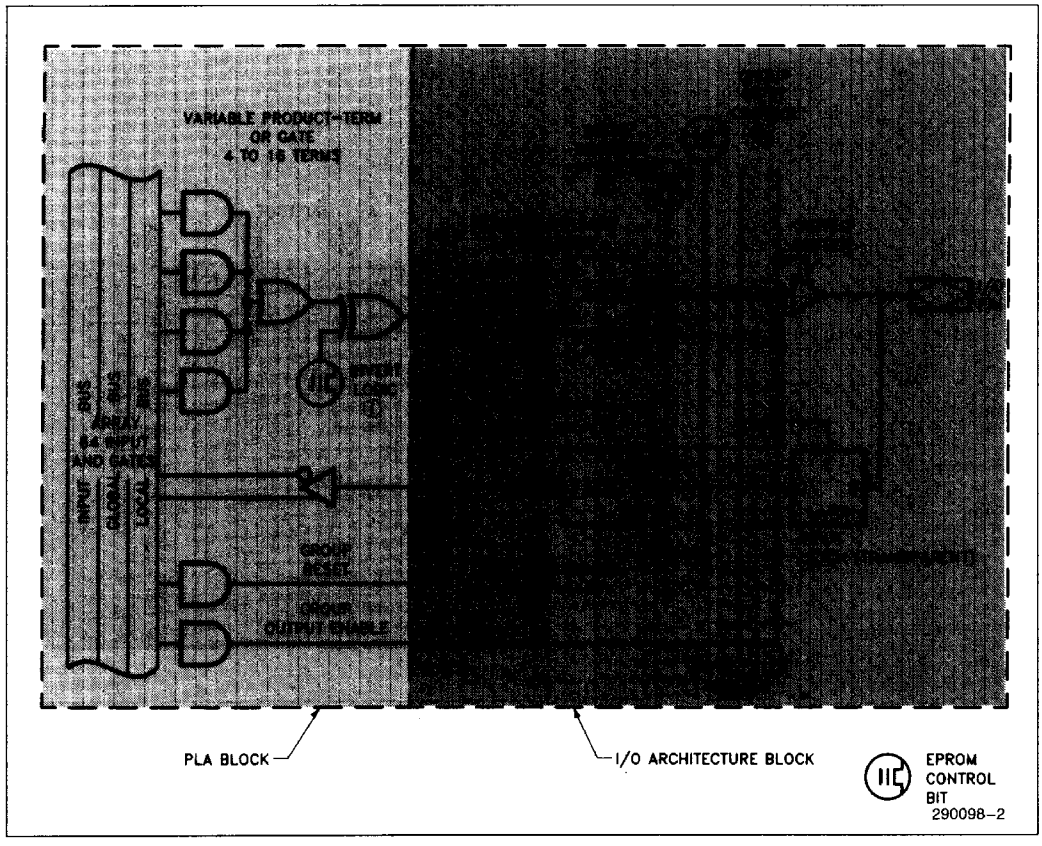


Figure 1. 5C121 Macrocell I/O Architecture

The reset and output-enable controls are logically controlled by single product terms (the logic AND of programmed variables in the array). These terms have control over banks of four macrocells.

The output-enable control may be used to generate architecture types that include bi-directional, 3-state, open drain, or input only structures.

INTERNAL BUS STRUCTURE

The two identical halves of the 5C121 communicate via a series of busses. The local bus structure used for communication within each half of the chip contains 16 conductors that carry the TRUE and COMPLEMENT of 8 local macrocells. In the block diagram (Figure 2) of the 5C121 the local macrocells are B-1 and B-2 on one half and A-1 and A-2 on the other half.

The global busses (Input bus & Global feedback from A-3 & B-3 macrocells & buried registers) are made up of 48 conductors that span the entire chip. These 48 conductors carry the TRUE and COMPLEMENT of the twelve primary inputs (pins 2 through 7 and 33 through 38), signals from 4 Buried Registers as well as the global outputs of 8 macrocells in groups A-3 and B-3.

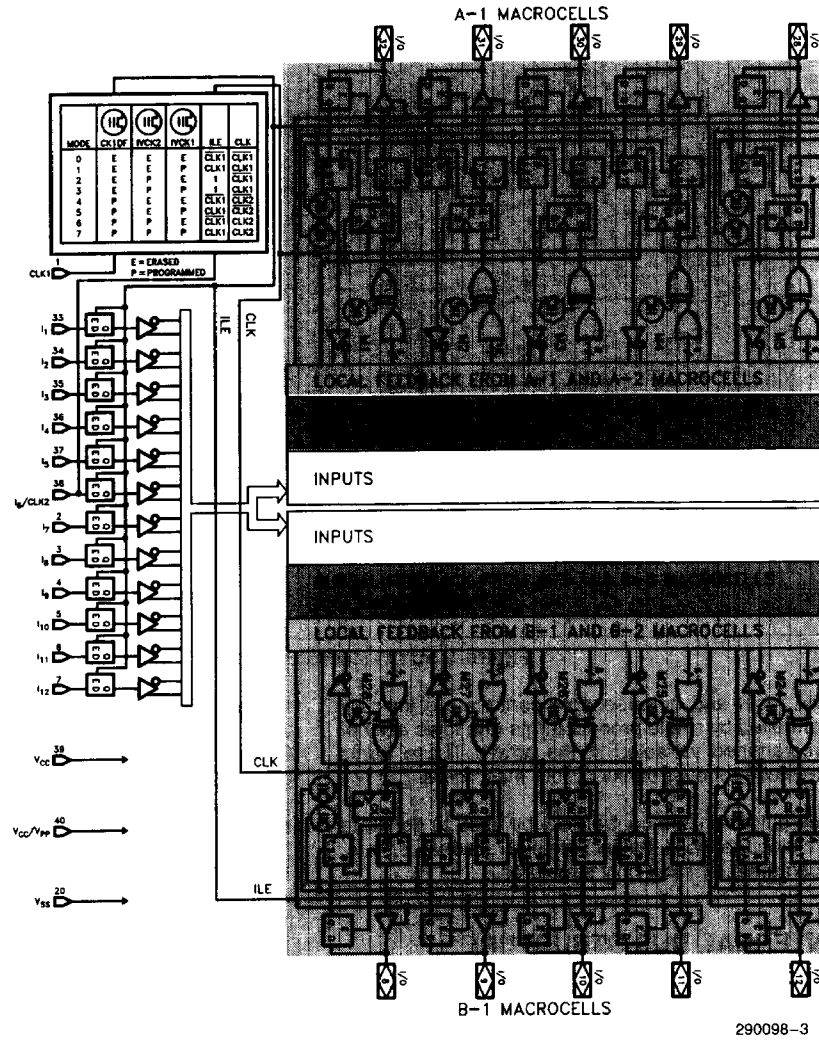


Figure 2. 5C121 Block Diagram

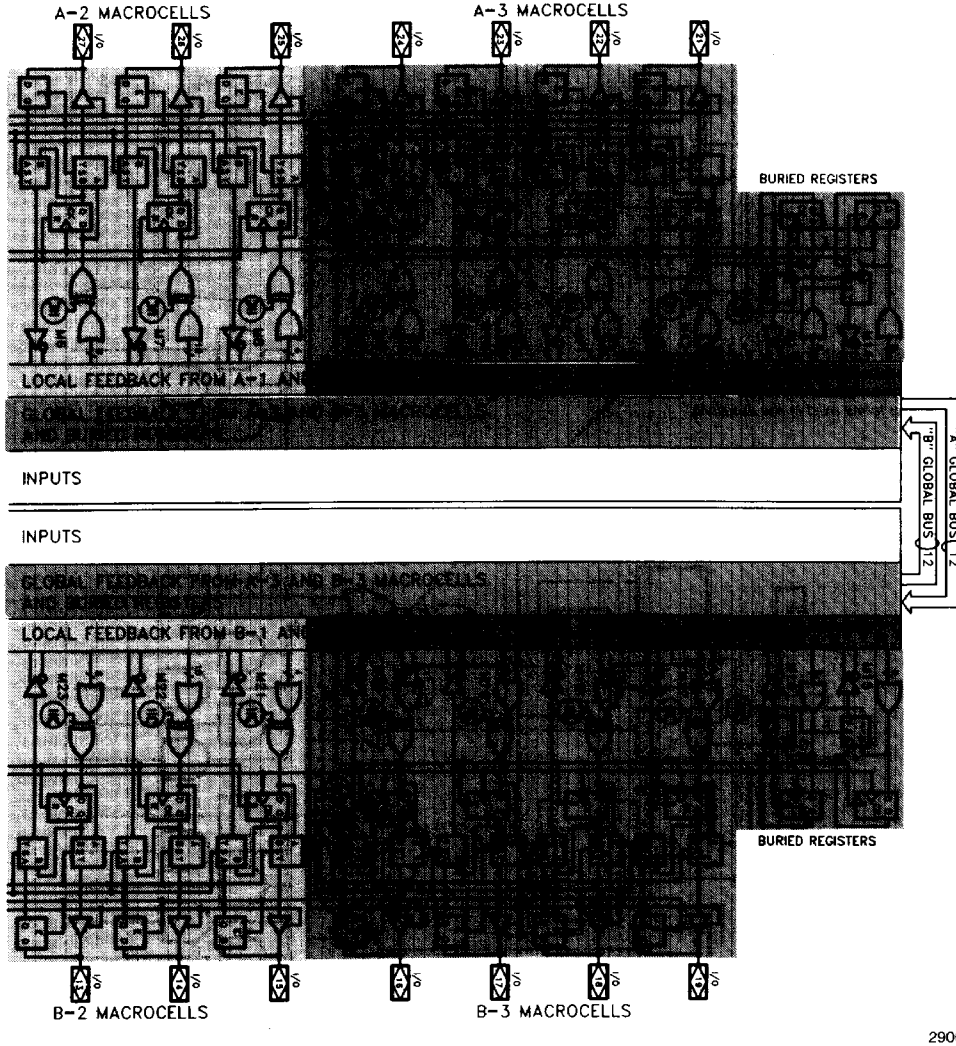


Figure 2. 5C121 Block Diagram (Continued)

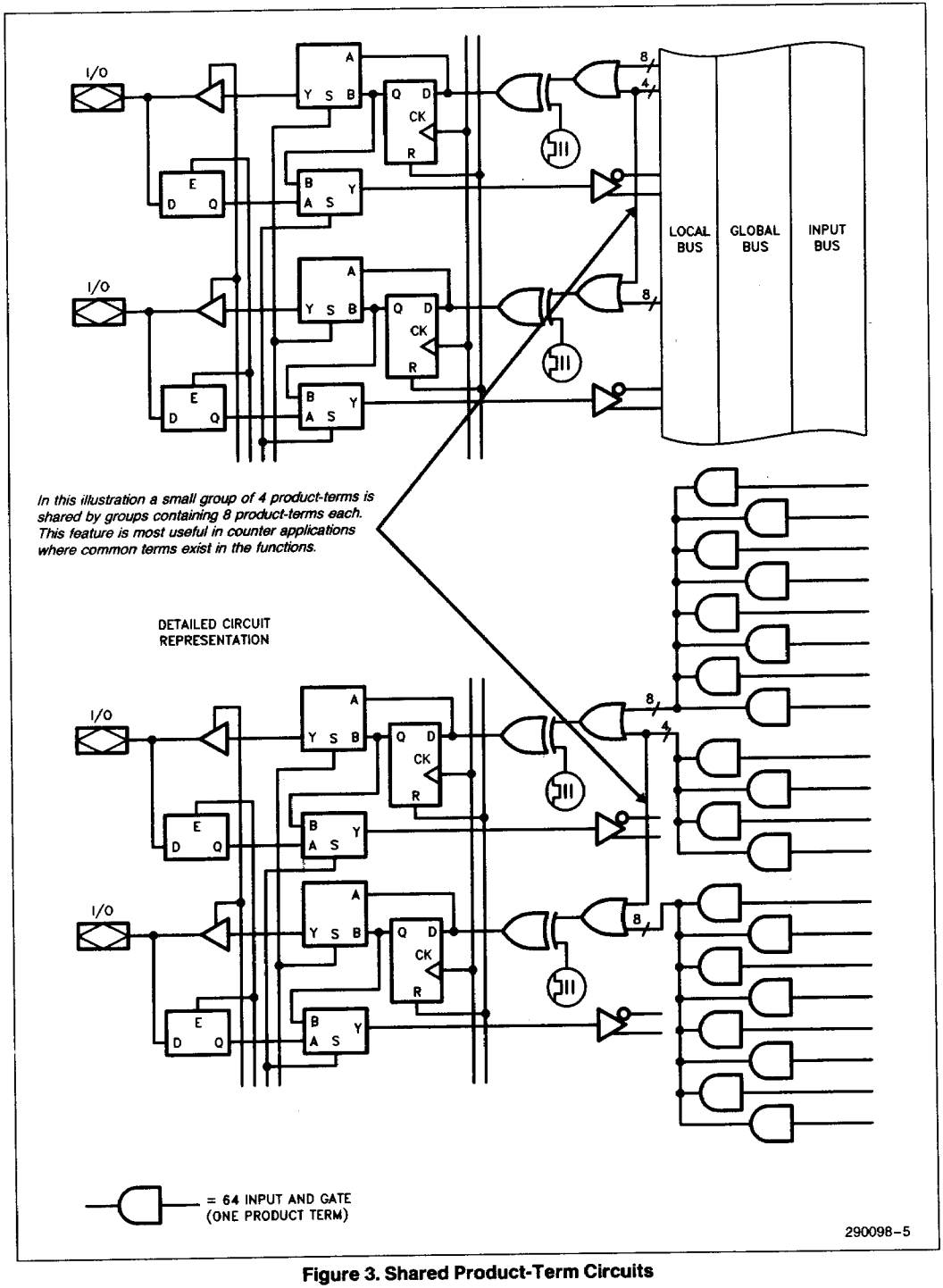


Figure 3. Shared Product-Term Circuits

SHARED PRODUCT TERMS

Macrocells 9 & 10, 11 & 12, 17 & 18 and 19 & 20 (in groups A-3 and B-3—the macrocells with global feedback) have the facility to share a total of 16 additional product terms. This sharing takes place between pairs of adjacent macrocells. This capability enables, for example, macrocells 9 and 10 to expand to 16 and 8 effective product terms respectively, and for macrocells 11 and 12 both to expand to 12 effective product terms. Figure 3 shows this sharing technique in detail. This facility is primarily of use in state machine and counter applications where common product terms are frequently required among output functions.

MACROCELL-BUS INTERFACE

As discussed earlier, the macrocells within the 5C121 are interconnected to other macrocells and inputs to the device via three internal data busses.

The product terms span the entire bus structure (local feedback, global feedback and input buses) that is adjacent to their macrocell (see Figure 4) so that they may produce a logical AND of any of the variables (or their complements) that are present on the busses.

All macrocells have the ability to return data to the local or the global bus. Feedback data may originate from the output of the macrocell or from the I/O pin. Feedback to the global bus communicates throughout the part. Macrocells that feedback to the local bus communicate only to their half of the 5C121. Connections to and from the signal busses are made with EPROM switches that provide the reprogrammable logic capability of the circuit.

Macrocells in groups A-3 and B-3 and the buried registers all have global bus connections while macrocells in groups A-1, A-2 and B-1, B-2 have only local bus connections (see Block Diagram, Figure 2). Advanced features of the Intel Programmable Logic Development System II will, if desired, automatically select an appropriate macrocell to meet both the logic requirements and the connection to an appropriate signal bus to achieve the interconnection to other macrocells.

At each intersecting point in the logic array there exists an EPROM-type programmable connection. Initially, all connections are complete. This means that both the true and complement of all inputs are connected to each product-term. Connections are opened during the programming process. Therefore any product term can be connected to the true or complement of any input. When both the true and complement connections of any input are left intact, a logical false results on the output of the AND gate. If both the true and complement connections of any input are programmed open, then a logical "don't care" results for that input. If all inputs for a product term are programmed open, then a logical true results on the output of the AND gate.

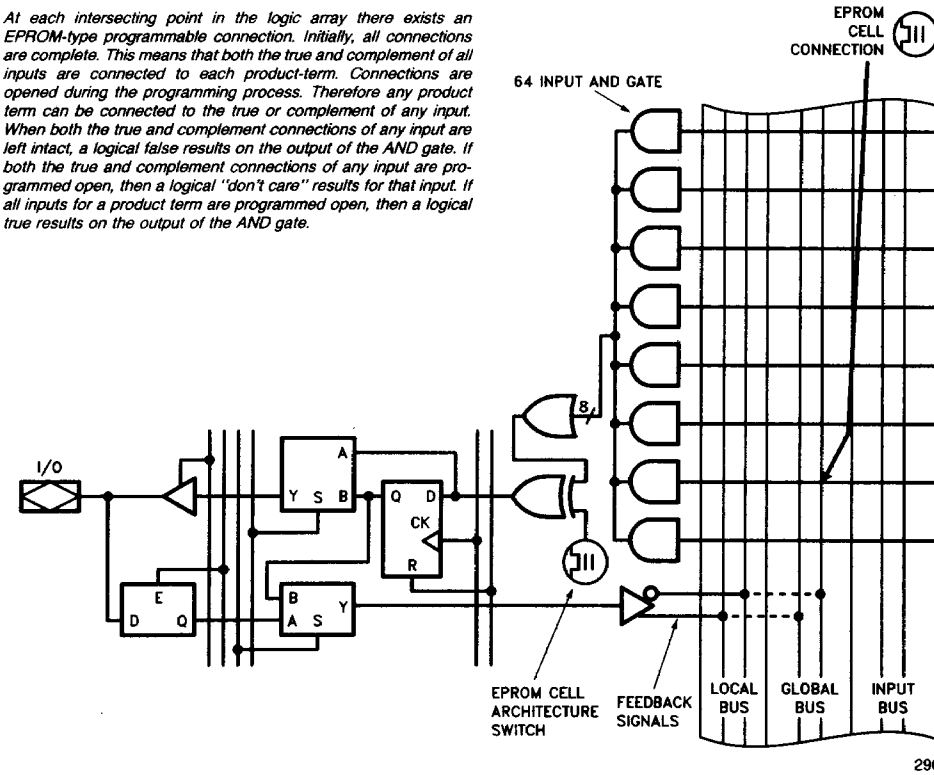


Figure 4. Macrocell-Bus Interface

CLOCK MODE CONTROL

The 5C121 contains two internal clock data paths that drive the input latches (transparent 7475 type) and the output registers. These clocks may be programmed into one of 8 operating modes (see clock mode Table 1). Figure 1 shows a typical macrocell which is driven by the master clock signal CLK and the input latch-enable signal ILE.

The master clock signal is input via pin 1. If programmed modes 4, 5, 6 & 7 are chosen, a second clock signal is required which is input via pin 38 (see Figure 5). Table 1 shows the operation of each clock programming mode.

If modes 0, 1, 4, 5, 6 or 7 are chosen (i.e. latching of the inputs is required), all inputs, both dedicated and I/O, are latched with the same ILE signal. Data applied to the inputs when CLK1 is low (high) is latched when CLK1 goes high (low) and will stay latched as long as CLK1 stays high (low). Levels shown in parenthesis are for modes 1, 5 & 7 and levels shown outside parenthesis are for modes 0, 4 & 6.

Care is required when using any of the clock modes 4, 5, 6 or 7, that require two input clock signals to ensure that timing hazards are not created.

ERASURE CHARACTERISTICS

Erasure characteristics of the 5C121 are such that erasure begins to occur upon exposure to light with wavelengths shorter than approximately 4000Å. It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000–4000Å. Data shows that constant exposure to room level fluorescent lighting could erase the typical 5C121 in approximately three years, while it would take approximately one week to cause erasure when exposed to direct sunlight. If the 5C121 is to be exposed to these types of lighting conditions for extended periods of time, conductive opaque labels should be placed over the window to prevent unintentional erasure.

The recommended erasure procedure for the 5C121 is exposure to shortwave ultraviolet light which has the wavelength of 2537Å. The integrated dose (i.e., UV intensity × exposure time) for erasure should be a minimum of fifteen (15) Wsec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12,000 μW/cm^2 power rating. The 5C121 should be placed within one inch of the lamp tubes during erasure. The maximum integrated dose the 5C121 can be exposed to without damage is 7258 Wsec/cm^2 (1 week @ 12,000 μW/cm^2). Exposure to high intensity UV light for longer periods may cause permanent damage.

PROGRAMMING CHARACTERISTICS

Initially, and after erasure, all the EPROM control bits of the 5C121 are connected (in the "1" state). Each of the connected control bits are selectively disconnected by programming the EPROM cell into their "0" state. Programming voltage and waveform specifications are available by request from Intel to support programming of the 5C121.

int$_e$ligent Programming™ Algorithm

The 5C121 supports the int$_e$ligent Programming Algorithm which rapidly programs Intel H-ELPDs (and EPROMs) using an efficient and reliable method. The int$_e$ligent Programming Algorithm is particularly suited to the production programming environment. This method greatly decreases the overall programming time while programming reliability is ensured as the incremental program margin of each bit is continually monitored to determine when the bit has been successfully programmed.

FUNCTIONAL TESTING

Since the logical operation of the 5C121 is controlled by EPROM elements, the device is completely factory tested. Each programmable EPROM bit controlling the internal logic including the buried state registers are tested using application-independent test program patterns. After testing, the devices are erased before shipment to customers. No post-programming tests of the EPROM array are necessary.

DESIGN RECOMMENDATIONS

For proper operation it is recommended that input and output pins be constrained to the range GND < (V_{IN} or V_{OUT}) < V_{CC}. Unused inputs should be tied to an appropriate logic level (e.g. either V_{CC} or GND) to minimize device power consumption.

When utilizing a macrocell with an I/O pin connection as a buried macrocell (i.e. just using the macrocell for feedback purposes to other macrocells), its I/O pin is a 'reserved pin'. (The Intel Programmable Logic Development System II will label the pin 'RESERVED' in the utilization report that it generates.) Such an I/O pin will actually be an output pin and should not be grounded. It should be left unconnected such that it can go high or low depending on the state of the macrocell's output.

In normal operation V_{CC}/V_{PP} (pin 40) should be connected directly to V_{CC} (pin 39).

Table 1. Clock Programming (Key: L = Latched; T = Transparent)

Programmed Mode	Input Signals Are Latched When:	Output Registers Change State When:	Clock Configuration
0	CLK1 (Pin 1)  L T	CLK1 (Pin 1) 	1 Clock
1	CLK1 (Pin 1)  T L	CLK1 (Pin 1) 	1 Clock
2	Inputs Not Latched	CLK1 (Pin 1) 	1 Clock
3	Inputs Not Latched	CLK1 (Pin 1) 	1 Clock
4	CLK1 (Pin 1)  L T	CLK2 (Pin 38) 	2 Clocks
5	CLK1 (Pin 1)  T L	CLK2 (Pin 38) 	2 Clock
6	CLK1 (Pin 1)  L T	CLK2 (Pin 38) 	2 Clocks
7	CLK1 (Pin 1)  T L	CLK2 (Pin 38) 	2 Clocks

As with all CMOS devices, ESD handling procedures should be used with the 5C121 to prevent damage to the device during programming, assembly, and test.

DESIGN SECURITY

A single EPROM bit provides a programmable design secruity feature that controls the access to the data programmed into the device. If this bit is set, a proprietary design within the device cannot be copied. This EPROM security bit enables a higher degree of design security than fused-based devices since programmed data within EPROM cells is invisible even to microscopic evaluation. The EPROM security bit, along with all the other EPROM control bits, will be reset by erasing the device.

AUTOMATIC STAND-BY MODE

The 5C121 contains a programmable bit, the Turbo Bit, that optimizes operation for speed or for power savings. When the Turbo Bit is programmed (TURBO = ON), the device is optimized for maximum speed. When the Turbo Bit is not programmed (TURBO = OFF), the device is optimized for power savings by entering standby mode during periods of inactivity.

Figure 6 shows the device entering standby mode approximately 100 ns after the last input transition. When the next input transition is detected, the device returns to active mode. Wakeup time adds an additional 10 ns to the propagation delay through the device as measured from the first input. No delay will occur if an output is dependent on more than one input and the last of the inputs changes after the device has returned to active mode.

After erasure, the Turbo Bit is unprogrammed (OFF); automatic standby mode is enabled. When the Turbo Bit is programmed (ON), the device never enters standby mode.

LATCH-UP IMMUNITY

All of the input, I/O, and clock pins of the 5C121 have been designed to resist latch-up which is inherent in inferior CMOS structures. The 5C121 is designed with Intel's proprietary CHMOS II-E EPROM process. Thus, each of the 5C121 pins will not experience latch-up with currents up to 100 mA and voltages ranging from $-1V$ to $V_{CC} + 1V$. Furthermore, the programming pin is designed to resist latch-up to the 13.5V maximum device limit.

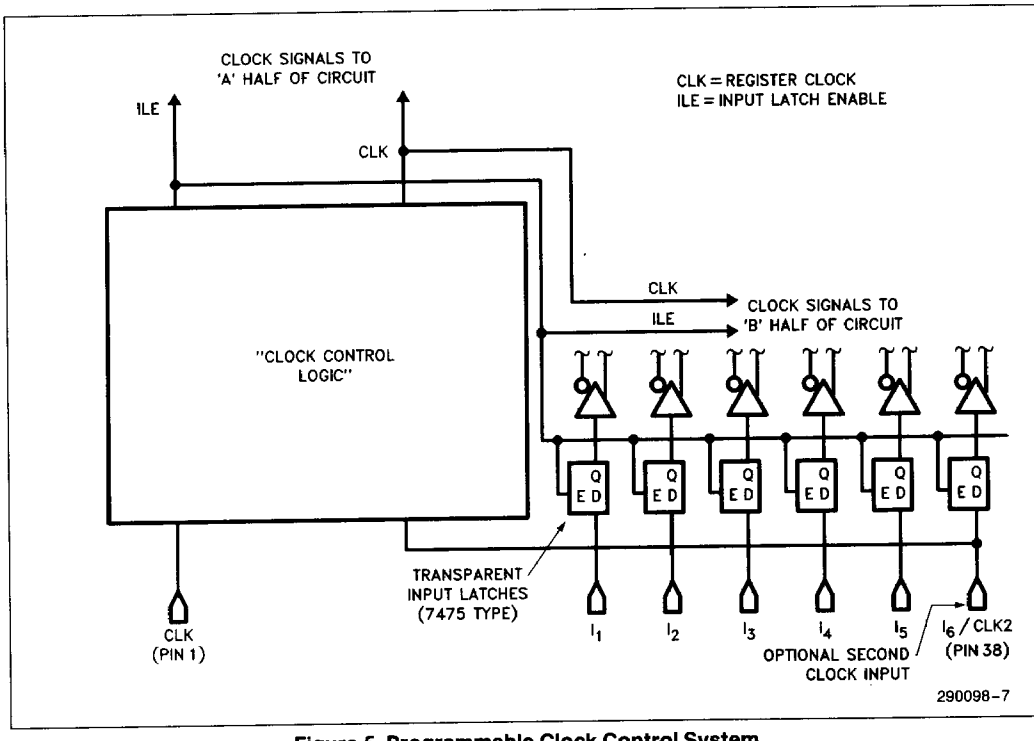


Figure 5. Programmable Clock Control System

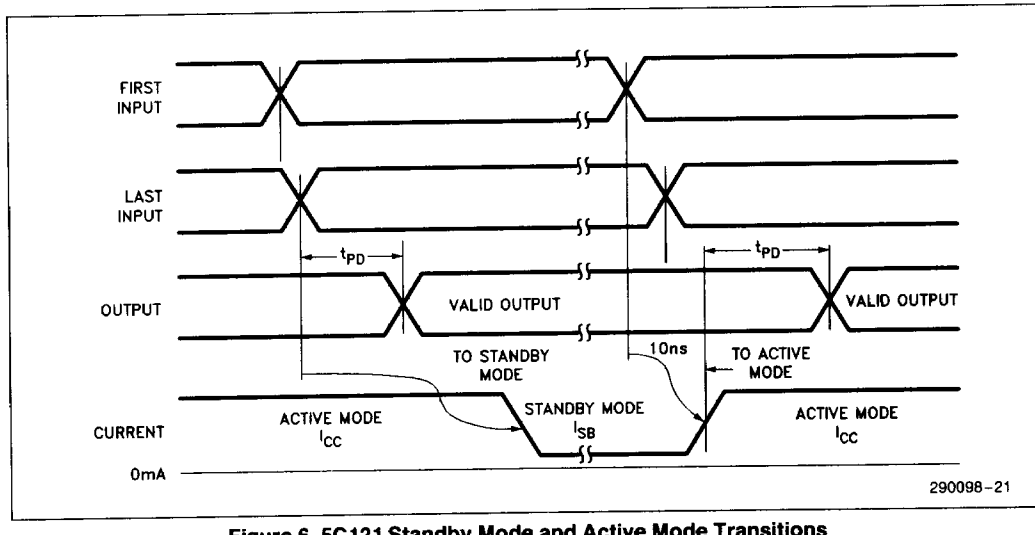


Figure 6. 5C121 Standby Mode and Active Mode Transitions

Intel Programmable Logic Development System II (iPLDS II)

iPLDS II provides all the tools needed to design with Intel H-Series EPLDs or compatible devices. It contains comprehensive third generation software that supports four different design entry methods, minimizes logic, does automatic pin assignments and produces the best design fit for the selected EPLD. It is user friendly with guided menus, on-line Help messages and soft key inputs.

In addition, the iPLDS II contains programmer hardware in the form of an expansion card for the PC with programming software to enable the user to program EPLDs, read and verify programmed devices and also to graphically edit programming files. The software generates industry standard JEDEC object code output files which can be downloaded to other programmers as well.

The iPLDS II has interfaces to popular schematic capture packages to enable designs to be entered using schematics. An integrated schematic entry method is provided by SCHEMA II-PLD, a low-cost schematic capture package that supports EPLD primitives and user-defined macro symbols. SCHEMA II-PLD contains the EPLD Design Manager, which provides a single user interface to both SCHEMA II-PLD and iPLS II software. The other design entry formats supported are Boolean equation entry and State Machine design entry.

The iPLDS II runs on the IBM† PC, PC/XT or PC/AT and other compatible machines with the following configuration:

(1) At least one floppy disk drive and hard disk drive

(2) MS-DOS†† Operating System Version 2.0 or later release

(3) 512K Memory (640K recommended)

(4) Intel iUP-PC Universal Programmer-Personal Computer and GUPI Adaptor (supplied with iPLDS II).

Detailed information on the Intel Programmable Logic Development System II is contained in a separate Intel data sheet (Order Number: 280168).

†IBM Personal Computer is a registered trademark of International Business Machine Corporation.

††MS-DOS is a registered trademark of Microsoft Corporation.

ADF PRIMITIVES SUPPORTED

The following ADF primitives are supported by this device:

INP	RONF
LINP	RORF
CONF	ROIF
CORF	ROLF
COIF	NOCF
COLF	NORF

ORDERING INFORMATION

t_{PD} (ns)	t_{CO} (ns)	f_{MAX} (MHz)	Order Code	Package	Operating Range
55	32	25	D5C121-55	CERDIP	Commercial
65	33	20	D5C121-65	CERDIP	Commercial
90	38	16	D5C121-90	CERDIP	Commercial

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage(1)	−2.0	7.0	V
V_{PP}	Programming Supply Voltage(1)	−2.0	13.5	V
V_I	DC Input Voltage(1)(2)	−0.5	V_{CC}+0.5	V
I_{CC}	DC V_{CC} Current(4)		100	mA
T_{stg}	Storage Temperature	−65	+150	°C
T_{amb}	Ambient Temperature(3)	−10	+85	°C

Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

NOTES:
1. Voltages with respect to ground.
2. Minimum DC input is −0.5V. During transitions, the inputs may undershoot to −2.0V or overshoot to 7.0V for periods less than 20 ns under no load conditions.
3. Under bias.
4. With outputs tristated.

RECOMMENDED OPERATING CONDITIONS

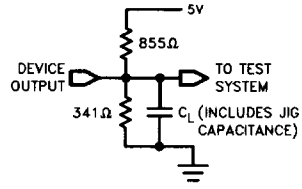
Symbol	Parameter	Min	Max	Units
V_{CC}	Supply Voltage	4.75	5.25	V
V_I	Input Voltage	0	V_{CC}	V
V_O	Output Voltage	0	V_{CC}	V
T_A	Operating Temperature	0	70	°C
t_R	Input Rise Time		500	ns
t_F	Input Fall Time		500	ns

D.C. CHARACTERISTICS T_A = 0° to 70°C, V_{CC} = 5.0V ±5%

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IH}	HIGH Level Input Voltage			2.0		V_{CC}+0.3	V
V_{IL}	LOW Level Input Voltage			−0.3		0.8	V
V_{OH}	HIGH Level Output Voltage	I_O = −4.0 mA DC		2.4			V
V_{OL}	LOW Level Output Voltage	I_O = 4.0 mA DC				0.45	V
I_I	Input Leakage Current	V_I = V_{CC} or GND				±10.0	µA
I_{OZ}	3-State Output Off-State Current	V_O = V_{CC} or GND				±10.0	µA
I_{OS}	Output Short Circuit Current	(Note 5)				130	mA
I_{SB}	V_{CC} Supply Current (Standby) (Note 6)	V_I = V_{CC} or GND, I_O = 0	CMOS Inputs			3	mA
			TTL Inputs			30	
I_{CC}	V_{CC} Supply Current (Active)	No Load, f = 10 MHz	CMOS Inputs			50	mA
			TTL Inputs			100	

NOTES:
5. Output shorted for no more than 1 sec. and no more than one output shorted at a time. I_{OS} is sampled but not 100% tested.
6. Chip automatically goes into standby mode if logic transitions do not occur. (Approximately 100 ns after last transition.)

A.C. TESTING LOAD CIRCUIT



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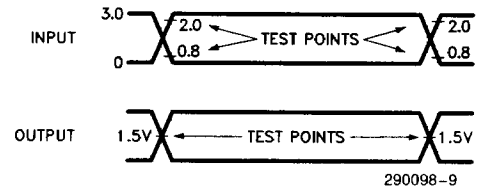
C_L = 50 pF

A.C. TESTING INPUT, OUTPUT WAVEFORM



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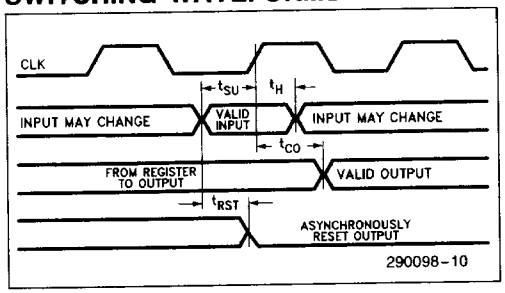
A.C. Testing: Inputs are Driven at 3.0V for a Logic "1" and 0V for a Logic "0". Timing Measurements are made at 2.0V for a Logic "1" and 0.8V for a Logic "0" on inputs. Outputs are measured at a 1.5V point. Device input rise and fall times < 6 ns.

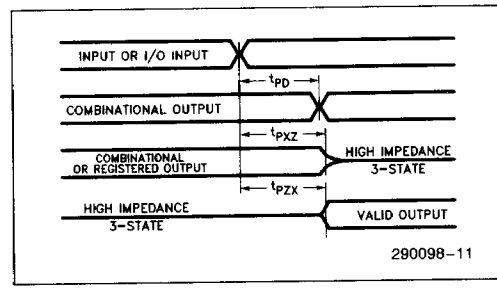
A.C. CHARACTERISTICS T_A = 0° to 70°C, V_{CC} = 5.0V ±5%

Symbol	Parameter	Device	5C121-55 EP1210-1		5C121-65 EP1210-2		5C121-90 EP1210		Unit
		Conditions	Min	Max	Min	Max	Min	Max	
t_{PD}	Non-Registered Input or I/O Input to Non-Registered Output			55		65		90	ns
t_{PZX}[7]	Non-Registered Input or I/O Input to Output Enable	C_L = 30 pF		50		65		90	ns
t_{PXZ}[7]	Non-Registered Input or I/O Input to Output Disable			50		65		90	ns
t_{SU}	Non-Registered Input or I/O Input to Output Register Setup		40		47		62		ns
t_H	Non-Registered Input or I/O Input to Output Register Hold		0		0		0		ns
t_{CH}	Clock High Time		20		25		30		ns
t_{CL}	Clock Low Time	C_L = 30 pF	20		25		30		ns
t_{CO}	Clock to Output Delay			32		33		38	ns
t_{CNT}	Minimum Clock Period (Register Output Feedback to Register Input—Internal Path)		50		55		75		ns
f_{CNT}	Maximum Frequency ($1/t_{CNT}$)			20.0		18.0		13.0	MHz
f_{MAX}	Maximum Frequency ($1/t_{SU}$)—Pipelined			25.0		21.2		16.1	MHz
t_{RST}	Asynchronous Reset Time			50		65		90	ns
t_{ILS}	Set Up Time for Latching Inputs		0		0		0		ns
t_{ILH}	Hold Time for Latching Inputs		15		20		25		ns
t_{C1C2}	Minimum Clock 1 to Clock 2 Delay		40		50		65		ns
t_{ILDFS}	Input Latch to D-FF Setup Time	Mode 0, 1	40		50		65		ns
t_{DFILS}	D-FF to Input Latch Setup Time		25		30		35		ns
t_{P3}	Minimum Period for a 2-Clock System (T_{C1C2} + t_{CO1})		72		83		103		ns
f_3	Maximum Frequency ($1/t_{P3}$)			13.8		12.0		9.7	MHz

NOTE:
7. t_{PZX} and t_{PXZ} are measured at ±0.5V from steady state voltage as driven by spec. output load. t_{PXZ} is measured with C_L = 5 pF.

SWITCHING WAVEFORMS

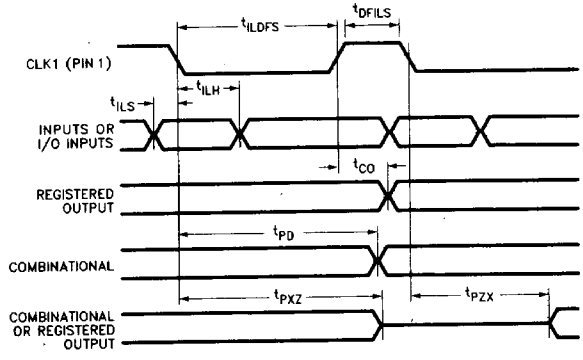




NOTE:
Above waveforms shown for clock modes 2 or 3 (t_{SU} & t_H are as in modes 2 & 3; no ILE signal is used).

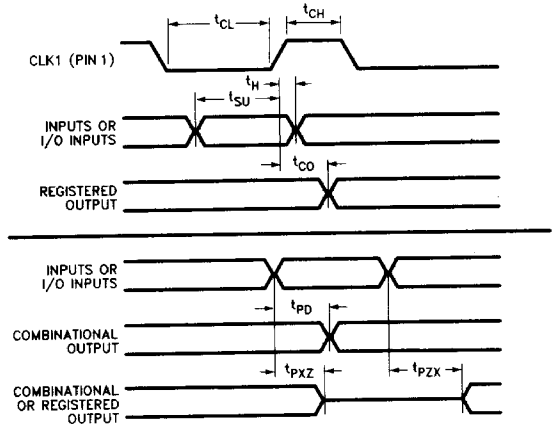
CLOCK MODES SWITCHING WAVEFORMS

1-CLOCK SYSTEM: MODES 0 AND 1



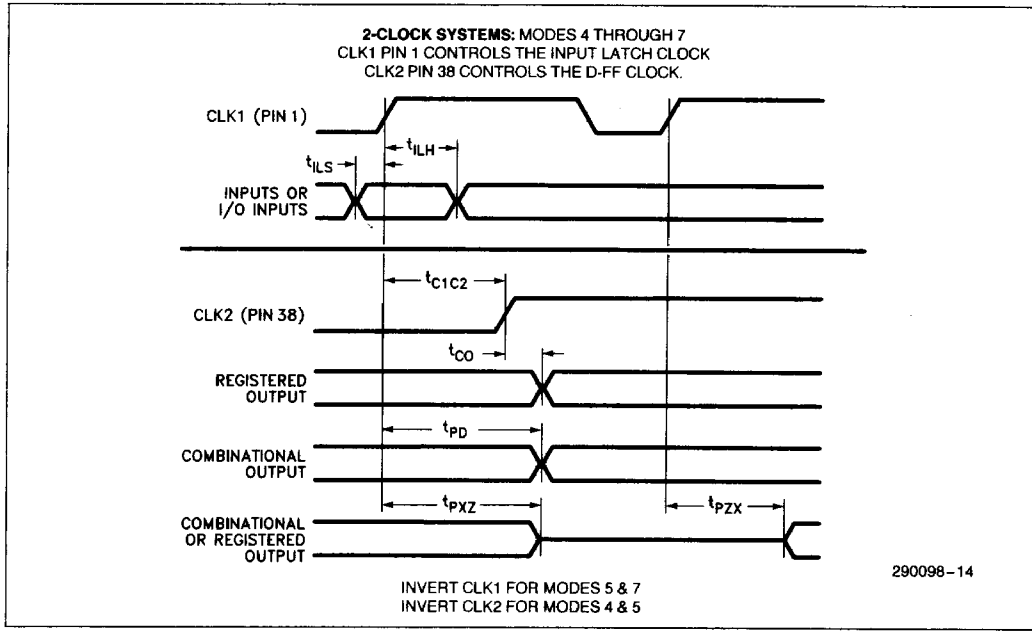
INVERT CLK1 FOR MODE 0

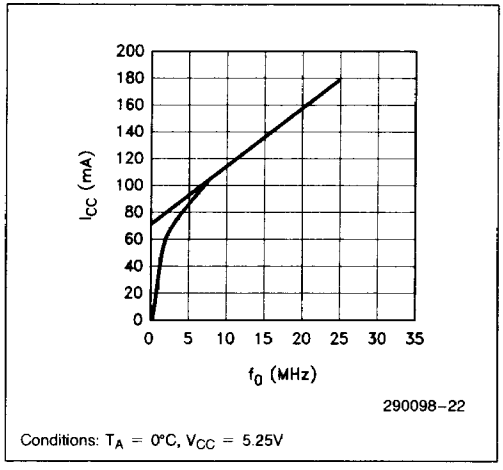
1-CLOCK SYSTEM: MODES 2 AND 3



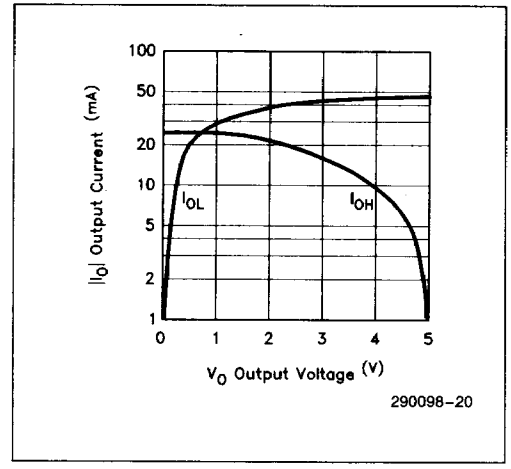
INVERT CLK1 FOR MODE 2

CLOCK MODES
SWITCHING WAVEFORMS (Continued)





5C121 Current in Relation to Frequency



Output Drive Current in Relation to Voltage