RoboClockII™ CY7B994V

PRELIMINARY **CY7B993V**

High-Speed Multi-Phase PLL Clock Buffer

Features

- **12/100-MHz (CY7B993V), or 24/185-MHz (CY7B994V) output operation**
- **Matched pair outputs skew <200 ps**
- **Zero input-to-output delay**
- **18 LVTTL 50% duty-cycle outputs capable of driving 50Ω terminated lines**
- **Commercial Temp. Range with 16 outputs at 185 MHz**
- **Industrial Temp. Range with 6 outputs at 185 MHz**
- **3.3V LVTTL/LV Differential (LVPECL), Fault Tolerant and Hot Insertable reference inputs**
- **Phase adjustments in 625/1300 ps steps up to ±10.4 ns**
- **Multiply/Divide ratios of (1–6, 8, 10, 12):(1–6, 8, 10, 12)**
- **Operation up to 12x input frequency**
- **Individual Output Bank disable for aggressive power management and EMI reduction**
- **Output high-impedance option for testing purposes**
- **Fully integrated PLL with Lock Indicator**
- **Low Cycle-to-Cycle Jitter (<100 ps peak-peak)**
- **Single 3.3V ± 10% supply**
- **100-Pin TQFP package**

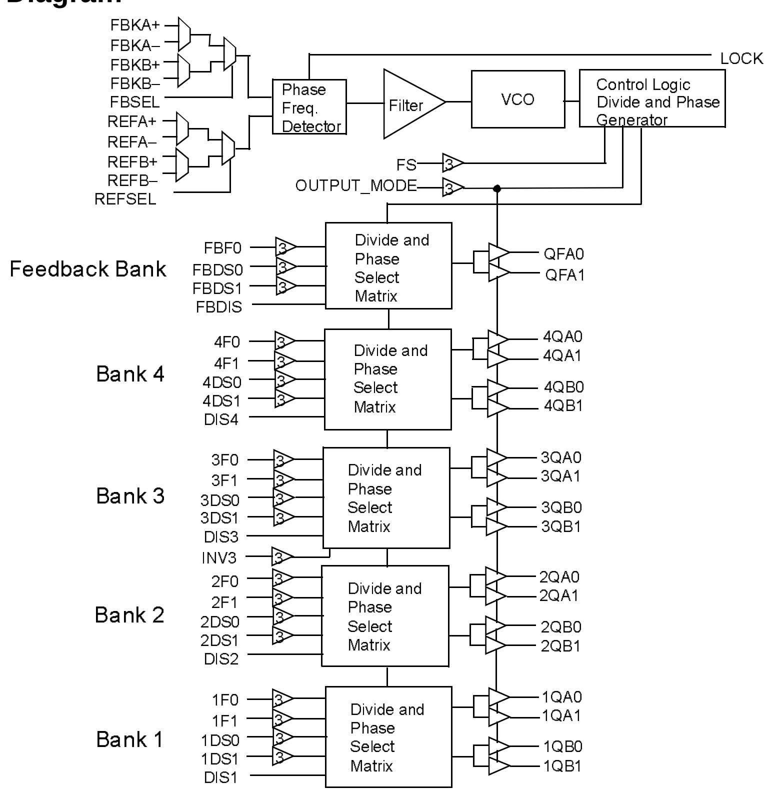
Functional Description

The CY7B993V and CY7B994V High-Speed Multi-Phase PLL Clock Buffers offer user-selectable control over system clock functions. This multiple-output clock driver provides the system integrator with functions necessary to optimize the timing of high-performance computer and communication systems.

Eighteen configurable outputs can each drive terminated transmission lines with impedances as low as 50Ω while delivering minimal and specified output skews at LVTTL levels. The outputs are arranged in five banks. Banks 1 to 4 of four outputs allow a divide function of 1 to 12, while simultaneously allowing phase adjustments in 625 ps–1300 ps increments up to 10.4 ns. One of the output banks also includes an independent clock invert function. The feedback bank consists of two outputs, which allows divide-by functionality from 1 to 12 and limited phase adjustments. Any one of these eighteen outputs can be connected to the feedback input as well as driving other inputs.

Selectable reference input is a fault tolerance feature which allows smooth change over to secondary clock source, when the primary clock source is not in operation. The reference inputs and feedback inputs are configurable to accommodate both LVTTL or Differential (LVPECL) inputs. The completely integrated PLL reduces jitter and simplifies board layout.

Functional Block Diagram



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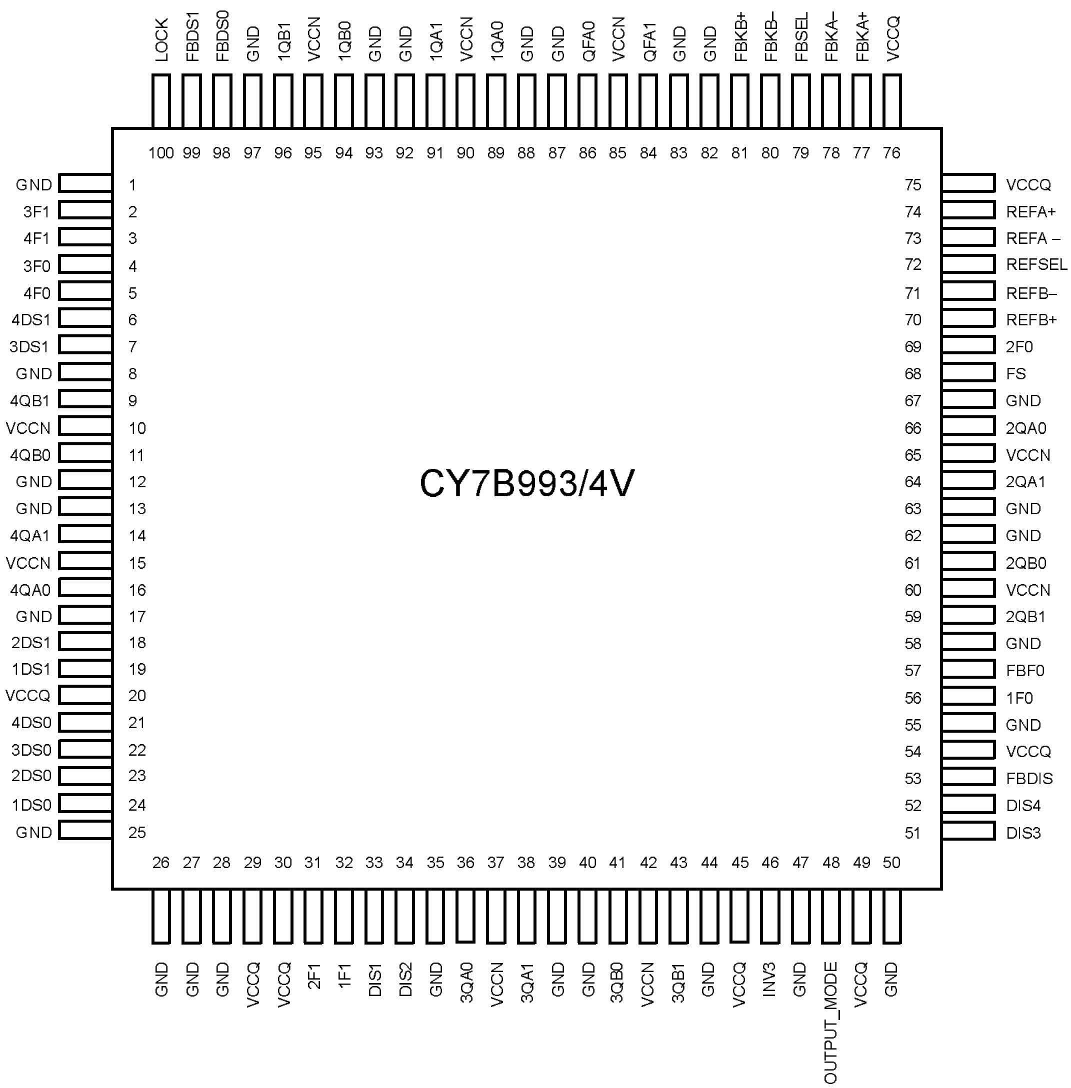
Pin Configurations

100-Pin TQFP



Pin Configurations (continued)

100-Lead BGA

	1	2	3	4	5	6	7	8	9	10
A	1QB1	1QB0	1QA1	1QA0	QFA0	QFA1	FBKB+	VCCQ	FBKA–	FBKA+
B	VCCN	VCCN	VCCN	VCCN	VCCN	VCCN	VCCQ	FBKB–	FBSEL	REFA+
C	GND	GND	GND	GND	GND	GND	VCCQ	GND	GND	REFA–
D	LOCK	4F0 (3_level)	3F1 (3_level)	GND	FBDS1 (3_level)	FBDS0 (3_level)	2F0 (3_level)	VCCQ	REFSEL	REFB–
E	4QB1	VCCN	4DS1 (3_level)	GND	3F0 (3_level)	4F1 (3_level)	GND	FS (3_level)	VCCN	REFB+
F	4QB0	VCCN	3DS1 (3_level)	GND	GND	GND	GND	FBF0 (3_level)	VCCN	2QA0
G	4QA1	2DS1 (3_level)	VCCQ	GND	GND	GND	GND	VCCQ	1F0 (3_level)	2QA1
H	4QA0	1DS1 (3_level)	1DS0 (3_level)	VCCQ	GND	GND	VCCQ	OUTPUT MODE (3_level)	FBDIS	2QB0
J	4DS0 (3_level)	3DS0 (3_level)	2DS0 (3_level)	DIS1	VCCN	VCCN	GND	INV3 (3_level)	DIS3	2QB1
K	2F1 (3_level)	1F1 (3_level)	DIS2	VCCN	3QA0	3QA1	GND	3QB0	3QB1	DIS4

Pin Definitions[1]

Name	I/O	Type	Description
FBSEL	Input	LVTTL	Feedback Input Select: When LOW, FBKA inputs are selected. When HIGH, the FBKB inputs are selected. This input has an internal pull-down.
FBKA+, FBKA– FBKB+, FBKB–	Input	LVTTL/ LVDIFF	Feedback Inputs: One pair of inputs selected by the FBSEL is used to feedback the clock output xQn to the phase detector. The PLL will operate such that the rising edges of the reference and feedback signals are aligned in both phase and frequency. These inputs can operate as differential PECL or single-ended TTL inputs. When operating as a single-ended LVTTL input, the complementary input must be left open.
REFA+, REFA– REFB+, REFB–	Input	LVTTL/ LVDIFF	Reference Inputs: These inputs can operate as differential PECL or single-ended TTL reference inputs to the PLL. When operating as a single-ended LVTTL input, the complementary input must be left open.
REFSEL	Input	LVTTL	Reference Select Input: The REFSEL input controls how the reference input is configured. When LOW, it will use the REFA pair as the reference input. When HIGH, it will use the REFB pair as the reference input. This input has an internal pull-down.
FS	Input	3-level Input	Frequency Select: This input must be set according to the nominal frequency (f_{NOM}). See *Table 1*.
FBF0	Input	3-level Input	Feedback Output Phase Function Select: This input determines the phase function of the Feedback Bank's QFA[0:1] outputs. See *Table 3*.
FBDS[0:1]	Input	3-level Input	Feedback Divider Function Select: These inputs determine the function of the QFA0 and QFA1 outputs. See *Table 4*.
FBDIS	Input	LVTTL	Feedback Disable: This input controls the state of QFA[0:1]. When HIGH, the QFA[0:1] is disabled to the "HOLD-OFF" or "HI-Z" state; the disable state is determined by OUTPUT_MODE. When LOW, the QFA[0:1] is enabled. See *Table 5*. This input has an internal pull-down.
[1:4]F[0:1]	Input	3-level Input	Output Phase Function Select: Each pair controls the phase function of the respective bank of outputs. See *Table 3*.
[1:4]DS[0:1]	Input	3-level Input	Output Divider Function Select: Each pair controls the divider function of the respective bank of outputs. See *Table 4*.
DIS[1:4]	Input	LVTTL	Output Disable: Each input controls the state of the respective output bank. When HIGH, the output bank is disabled to the "HOLD-OFF" or "HI-Z" state; the disable state is determined by OUTPUT_MODE. When LOW, the [1:4]Q[A:B][0:1] is enabled. See *Table 5*. These inputs each have an internal pull-down.
INV3	Input	3-level Input	Invert Mode: This input only affects Bank 3. When this input is LOW, each matched output pair will become complementary (3QA0+, 3QA1–, 3QB0+, 3QB1–). When this input is HIGH, all four outputs in the same bank will be inverted. When this input is MID all four outputs will be non-inverting.
LOCK	Output	LVTTL	PLL Lock Indicator: When HIGH, this output indicates the internal PLL is locked to the reference signal. When LOW, the PLL is attempting to acquire lock.
OUTPUT_MODE	Input	3-Level Input	Output Mode: This pin determines the clock outputs' disable state. When this input is HIGH, the clock outputs will disable to high-impedance (HI-Z). When this input is LOW, the clock outputs will disable to "HOLD-OFF" mode. When in MID, the device will enter factory test mode.
QFA[0:1]	Output	LVTTL	Clock Feedback Output: This pair of clock outputs is intended to be connected to the FB input. These outputs have numerous divide options and three choices of phase adjustments. The function is determined by the setting of the FBDS[0:1] pins and FBF0.
[1:4]Q[A:B][0:1]	Output	LVTTL	Clock Output: These outputs provide numerous divide and phase select functions determined by the [1:4]DS[0:1] and [1:4]F[0:1] inputs.
VCCN		PWR	Output Buffer Power: Power supply for each output pair.
VCCQ		PWR	Internal Power: Power supply for the internal circuitry.
GND		PWR	Device Ground.

Note:

1. For all three-state inputs, HIGH indicates a connection to V_{CC}, LOW indicates a connection to GND, and MID indicates an open connection. Internal termination circuitry holds an unconnected input to $V_{CC}/2$.

Block Diagram Description

Phase Frequency Detector and Filter

These two blocks accept signals from the REF inputs (REFA+, REFA–, REFB+ or REFB–) and the FB inputs (FBKA+, FBKA–, FBKB+ or FBKB–). Correction information is then generated to control the frequency of the Voltage Controlled Oscillator (VCO). These two blocks, along with the VCO, form a Phase-Locked Loop (PLL) that tracks the incoming REF signal.

The RoboClockII™ has a flexible REF and FB input scheme. These inputs allow the use of either differential LVPECL or single-ended LVTTL inputs. To configure as single-ended LVTTL inputs, the complementary pin must be left open (internally pulled to 1.5V), then the other input pin can be used as a LVTTL input. The REF inputs are also tolerant to hot insertion.

The REF inputs can be changed dynamically. When changing from one reference input to the other reference input of the same frequency, the PLL is optimized to ensure that the clock outputs period will not be less than the calculated system budget ($t_{MIN} = t_{REF}$ (nominal reference clock period) – t_{CCJ} (cycle-to-cycle jitter) – t_{PDEV} (max. period deviation)) while re-acquiring lock.

VCO, Control Logic, Divider, and Phase Generator

The VCO accepts analog control inputs from the PLL filter block. The FS control pin setting determines the nominal operational frequency range of the divide by one output (f_{NOM}) of the device. f_{NOM} is directly related to the VCO frequency. There are two versions of the RoboClockII, a low-speed device (CY7B993V) where f_{NOM} ranges from 12 MHz to 100 MHz, and a high-speed device (CY7B994V) which ranges from 24 MHz to 200 MHz. The FS setting for each device is shown in *Table 1*.

The f_{NOM} frequency is seen on "divide-by-one" outputs. For the CY7B994V, the upper f_{NOM} range extends from 96 MHz to 200 MHz, but the maximum output frequency is limited to185 MHz.

Table 1. Frequency Range Select

FS[2]	CY7B993V f_{NOM} (MHz) Min.	CY7B993V f_{NOM} (MHz) Max.	CY7B994V f_{NOM} (MHz) Min.	CY7B994V f_{NOM} (MHz) Max.
LOW	12	26	24	52
MID	24	52	48	100
HIGH	48	100	96	200[3]

Time Unit Definition

Selectable skew is in discrete increments of time unit (t_U). The value of a t_U is determined by the FS setting and the maximum nominal output frequency. The equation to be used to determine the t_U value is as follows:

$t_U = 1/(f_{NOM}*N)$

N is a multiplication factor which is determined by the FS setting. f_{NOM} is nominal frequency of the device. N is defined in *Table 2*.

Table 2. N Factor Determination

FS	CY7B993V N	CY7B993V f_{NOM} (MHz) at which t_U =1.0 ns	CY7B994V N	CY7B994V f_{NOM} (MHz) at which t_U =1.0 ns
LOW	64	15.625	32	31.25
MID	32	31.25	16	62.5
HIGH	16	62.5	8	125

Divide and Phase Select Matrix

The Divide and Phase Select Matrix is comprised of five independent banks: four banks of clock outputs and one bank for feedback. Each clock output bank has two pairs of low-skew, high-fanout output buffers ([1:4]Q[A:B][0:1]), two phase function select inputs ([1:4]F[0:1]), two divider function selects ([1:4]DS[0:1]), and one output disable (DIS[1:4]).

The feedback bank has one pair of low-skew, high-fanout output buffers (QFA[0:1]). One of these outputs may connect to the selected feedback input (FBK[A:B]±). This feedback bank also has one phase function select input (FBF0), two divider function selects FSDS[0:1], and one output disable (FBDIS).

The phase capabilities that are chosen by the phase function select pins are shown in *Table 3.* The divide capabilities for each bank are shown in *Table 4.*

Table 3. Output Skew Select Function

Function Selects [1:4]F1	Function Selects [1:4]F0 and FBF0	Output Skew Function Bank1	Bank2	Bank3	Bank4	Feed-back Bank
LOW	LOW	$-4t_U$	$-4t_U$	$-8t_U$	$-8t_U$	$-4t_U$
LOW	MID	$-3t_U$	–3tu	$-7t_U$	$-7t_U$	NA
LOW	HIGH	$-2t_U$	$-2t_U$	$-6t_U$	$-6t_U$	NA
MID	LOW	$-1t_U$	$-1t_U$	BK1[4]	BK1[4]	NA
MID	MID	$0t_U$	$0t_U$	$0t_U$	$0t_U$	0tu
MID	HIGH	$+1t_U$	$+1t_U$	BK2[4]	BK2[4]	NA
HIGH	LOW	$+2t_U$	$+2t_U$	$+6t_U$	$+6t_U$	NA
HIGH	MID	$+3t_U$	$+3t_U$	$+7t_U$	$+7t_U$	NA
HIGH	HIGH	$+4t_U$	$+4t_U$	$+8t_U$	$+8t_U$	$+4t_U$

Notes:

2. The level to be set on FS is determined by the "nominal" operating frequency (f_{NOM}) of the V_{CO} and Phase Generator. f_{NOM} always appears on an output when the output is operating in the undivided mode. The REF and FB are at f_{NOM} when the output connected to FB is undivided.
3. The maximum output frequency is 185 MHz.
4. BK1, BK2 denotes following the skew setting of Bank1 and Bank2 respectively.

Table 4. Output Divider Function

Function Selects		Output Divider Function				
[1:4]DS1 and FBDS1	**[1:4]DS0 and FBDS0**	**Bank 1**	**Bank 2**	**Bank 3**	**Bank 4**	**Feed-back Bank**
LOW	LOW	/1	/1	/1	/1	/1
LOW	MID	/2	/2	/2	/2	/2
LOW	HIGH	/3	/3	/3	/3	/3
MID	LOW	/4	/4	/4	/4	/4
MID	MID	/5	/5	/5	/5	/5
MID	HIGH	/6	/6	/6	/6	/6
HIGH	LOW	/8	/8	/8	/8	/8
HIGH	MID	/10	/10	/10	/10	/10
HIGH	HIGH	/12	/12	/12	/12	/12

Figure 1 illustrates the timing relationship of programmable skew outputs. All times are measured with respect to REF with the output used for feedback programmed with $0t_U$ skew. The PLL naturally aligns the rising edge of the FB input and REF input. If the output used for feedback is programmed to another skew position, then the whole t_U matrix will shift with respect to REF. For example, if the output used for feedback is programmed to shift $-8t_U$, then the whole matrix is shifted forward in time by $8t_U$. Thus an output programmed with $8t_U$ of skew will effectively be skewed $16t_U$ with respect to REF.

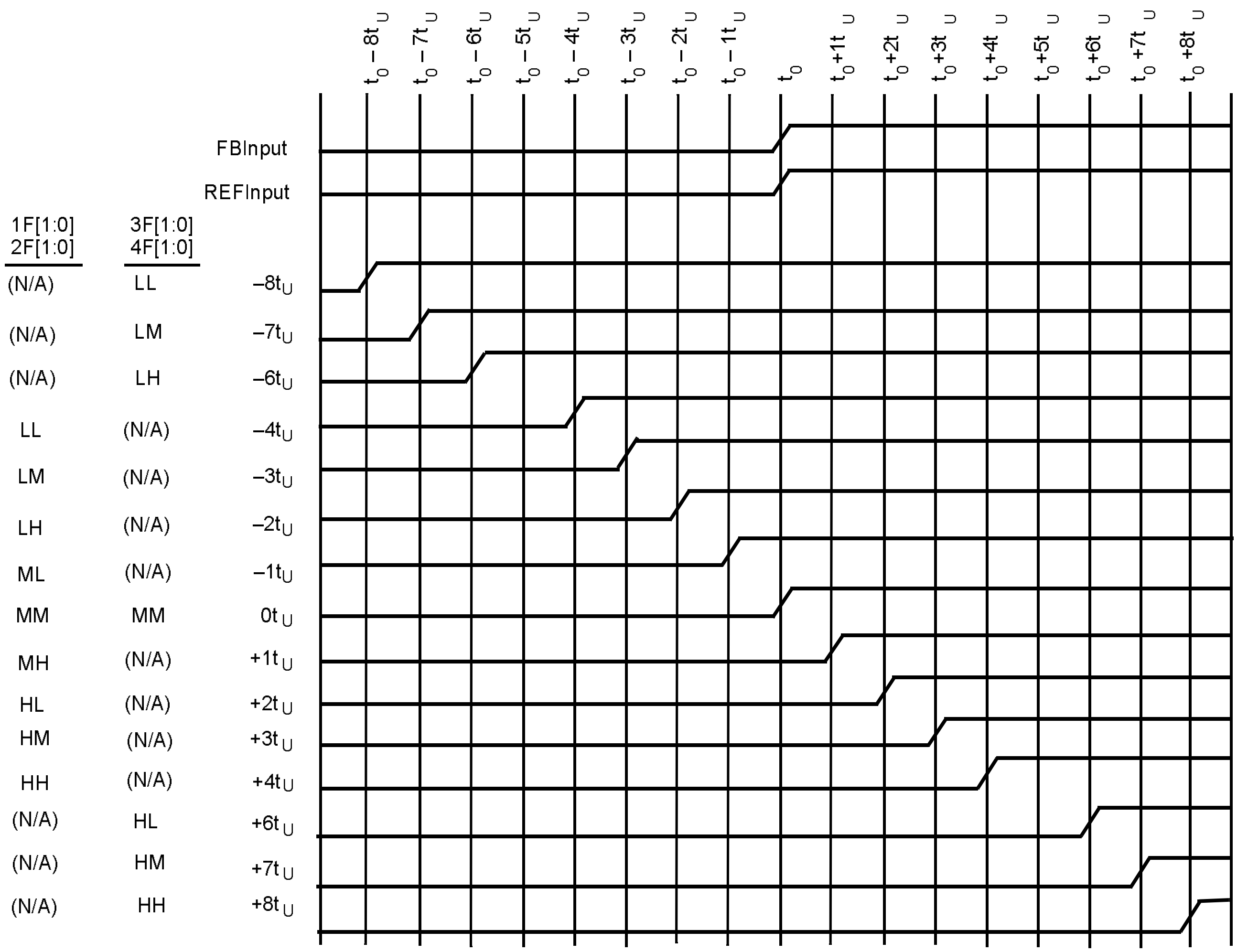


Figure 1. Typical Outputs with FB Connected to a Zero-Skew Output[5]

Note:
5. FB connected to an output selected for "zero" skew (i.e., FBF0=MID or XF[1:0]=MID).

Output Disable Description

The feedback Divide and Phase Select Matrix Bank has two outputs, and each of the four Divide and Phase Select Matrix Banks have four outputs. The outputs of each bank can be independently put into a HOLD-OFF or high-impedance state. The combination of the OUTPUT_MODE and DIS[1:4]/FBDIS inputs determines the clock outputs' state for each bank. When the DIS[1:4]/FBDIS is LOW, the outputs of the corresponding bank will be enabled. When the DIS[1:4]/FBDIS is HIGH, the outputs for that bank will be disabled to a high-impedance (HI-Z) or HOLD-OFF state depending on the OUTPUT_MODE input. *Table 5* defines the disabled output functions.

The HOLD-OFF state is intended to be a power saving feature. An output bank is disabled to the HOLD-OFF state in a maximum of six output clock cycles from the time when the disable input (DIS[1:4]/FBDIS) is HIGH. When disabled to the HOLD-OFF state, non-inverting outputs are driven to a logic LOW state on its falling edge. Inverting outputs are driven to a logic HIGH state on its rising edge. This ensures the output clocks are stopped without glitch. When a bank of outputs is disabled to HI-Z state, the respective bank of outputs will go HI-Z immediately.

Table 5. DIS[1:4]/FBDIS Pin Functionality

OUTPUT_MODE	DIS[1:4]/FBDIS	Output Mode
HIGH/LOW	LOW	ENABLED
HIGH	HIGH	HI-Z
LOW	HIGH	HOLD-OFF
MID	X	FACTORY TEST

INV3 Pin Function

Bank3 has signal invert capability. The four outputs of Bank3 will act as two pairs of complementary outputs when the INV3 pin is driven LOW. In complementary output mode, 3QA0 and 3QB0 are non-inverting; 3QA1and 3QB1 are inverting outputs. All four outputs will be inverted when the INV3 pin is driven HIGH. When the INV3 pin is left in MID, the outputs will not invert. Inversion of the outputs are independent of the skew and divide functions. Therefore, clock outputs of Bank3 can be inverted, divided, and skewed at the same time.

Lock Detect Output Description

The LOCK detect output indicates the lock condition of the integrated PLL. Lock detection is accomplished by comparing the phase difference between the reference and feedback inputs. Phase error is declared when the phase difference between the two inputs is greater than the specified device propagation delay limit ($t_{PDFSL,\ M,\ H}$).

When in the locked state, after four or more consecutive feedback clock cycles with phase-errors, the LOCK output will be forced LOW to indicate out-of-lock state.

When in the out-of-lock state, 32 consecutive phase-errorless feedback clock cycles are required to allow the LOCK output to indicate lock condition (LOCK = HIGH).

If the feedback clock is removed after LOCK has gone HIGH, a "watchdog" circuit is implemented to indicate the out-of-lock condition after a time-out period by deasserting LOCK LOW. This time out period is based upon a divided down reference clock.

This assumes that there is activity on the selected REF input. If there is no activity on the selected REF input then the LOCK detect pin may not accurately reflect the state of the internal PLL.

Factory Test Mode Description

The device will enter factory test mode when the OUTPUT_MODE is driven to MID. In factory test mode, the device will operate with its internal PLL disconnected; input level supplied to the reference input will be used in place of the PLL output. In TEST mode the selected FB input(s) must be tied LOW. All functions of the device are still operational in factory test mode except the internal PLL and output bank disables. The OUTPUT_MODE input is designed to be a static input. Dynamically toggling this input from LOW to HIGH may temporarily cause the device to go into factory test mode (when passing through the MID state).

Factory Test Reset

When in factory test mode (OUTPUT_MODE=MID), the device can be reset to a deterministic state by driving the DIS4 input HIGH. When the DIS4 input is driven HIGH in factory test mode, all clock outputs will go to HI-Z; after the selected reference clock pin has 5 positive transitions, all the internal finite state machines (FSM) will be set to a deterministic state. The deterministic state of the state machines will depend on the configurations of the divide selects, skew selects, and frequency select input. All clock outputs will stay in high-impedance mode and all FSMs will stay in the deterministic state until DIS4 is deasserted. When DIS4 is deasserted (with OUTPUT_MODE still at MID), the device will re-enter factory test mode.

Safe Operating Zone

The following figure illustrates the operating condition at which the device does not exceed its allowable maximum junction temperature of 150°C. *Figure 2* shows the maximum number of outputs that can operate at 185 MHz (with 25-pF load and no air flow) at various ambient temperatures. At the limit line, all other outputs are configured to divide-by-two (i.e., operating at 92.5 MHz) or lower frequencies. The device will operate below maximum allowable junction temperature of 150°C when its configuration (with the specified constraints) falls within the shaded region (safe operating zone). *Figure 2* shows that at 85°C, the maximum number of outputs that can operate at 185 MHz is 6; and at 70°C, the maximum number of outputs that can operate at 185 MHz is 16 (with 25-pF load and 0-m/s air flow).

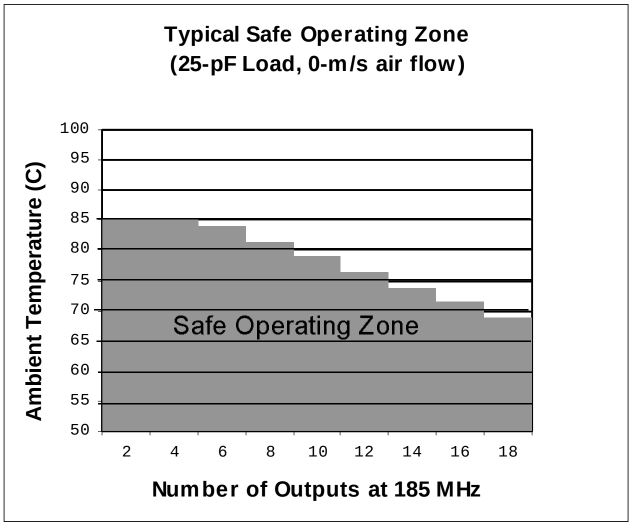


Figure 2. Typical Safe Operating Zone

Maximum Ratings

(Above which the useful life may be impaired. For user guide-lines, not tested.)

Storage Temperature ....–40°C to +125°C

Ambient Temperature with Power Applied ..–40°C to +125°C

Supply Voltage to Ground Potential ....–0.5V to +4.6V

DC Input Voltage ....–0.3V to V_{CC}+0.5V

Output Current into Outputs (LOW)......................... TBD mA

Static Discharge Voltage ....>1100V
(per MIL-STD-883, Method 3015)

Latch-Up Current.. TBD

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	3.3V ±10%
Industrial	–40°C to +85°C	3.3V ±10%

Electrical Characteristics Over the Operating Range

Parameter	Description		Test Conditions	Min.	Max.	Unit
LVTTL Compatible Output Pins (QFA[0:1], [1:4]Q[A:B][0:1], LOCK)						
V_{OH}	LVTTL HIGH Voltage	QFA[0:1], [1:4]Q[A:B][0:1]	V_{CC} = Min., I_{OH} = –30 mA	2.4		V
		LOCK	I_{OH} = –2 mA, V_{CC} = Min.	2.4		V
V_{OL}	LVTTL LOW Voltage	QFA[0:1], [1:4]Q[A:B][0:1]	V_{CC} = Min., I_{OL}= 30 mA		0.5	V
		LOCK	I_{OL}= 2 mA, V_{CC} = Min.		0.5	V
I_{OZ}	High-Impedance State Leakage Current			TBD	TBD	µA
LVTTL Compatible Input Pins (FBKA±, FBKB±, REFA±, REFB±, FBSEL, REFSEL, FBDIS, DIS[1:4])						
V_{IH}	LVTTL Input HIGH	FBK[A:B]±, REF[A:B]±	Min. ≤ V_{CC} ≤ Max.	2.0	V_{CC}+0.3	V
		REFSEL, FBSEL, FBDIS, DIS[1:4]		2.0	V_{CC}+0.3	V
V_{IL}	LVTTL Input LOW	FBK[A:B]±, REF[A:B]±	Min. ≤ V_{CC} ≤ Max.	–0.3	0.8	V
		REFSEL, FBSEL, FBDIS, DIS[1:4]		–0.3	0.8	V
I_I	LVTTL V_{IN} >V_{CC}	FBK[A:B]±, REF[A:B]±	V_{CC} = GND, V_{IN} = 3.63V		100	µA
I_{IH}	LVTTL Input HIGH Current	FBK[A:B]±, REF[A:B]±	V_{CC} = Max., V_{IN} = V_{CC}		500	µA
		REFSEL, FBSEL, FBDIS, DIS[1:4]	V_{IN} = V_{CC}	TBD	TBD	µA
I_{IL}	LVTTL Input LOW Current	FBK[A:B]±, REF[A:B]±	V_{CC} = Max., V_{IN} = GND	–500		µA
		REFSEL, FBSEL, FBDIS, DIS[1:4]		TBD	TBD	µA
3-Level Input Pins (FBF0, FBDS[0:1], [1:4]F[0:1], [1:4]DS[0:1], FS, OUTPUT_MODE(TEST))						
V_{IHH}	Three Level Input HIGH[6]		Min. ≤ V_{CC} ≤ Max.	0.87*V_{CC}		V
V_{IMM}	Three Level Input MID[6]		Min. ≤ V_{CC} ≤ Max.	0.47*V_{CC}	0.53*V_{CC}	V
V_{ILL}	Three Level Input LOW[6]		Min. ≤ V_{CC} ≤ Max.		0.13*V_{CC}	V
I_{IHH}	Three Level Input HIGH Current	3-level input pins excl. FBF0	V_{IN} = V_{CC}		200	µA
		FBF0			400	µA

Electrical Characteristics Over the Operating Range (continued)

Parameter	Description		Test Conditions	Min.	Max.	Unit
I_{IMM}	Three Level Input MID Current	3-level input pins excl. FBF0	$V_{IN} = V_{CC}/2$	–50	50	µA
		FBF0		–100	100	µA
I_{ILL}	Three Level Input LOW Current	3-level input pins excl. FBF0	V_{IN} = GND	–200		µA
		FBF0		–400		µA
LVDIFF Input Pins (FBK[A:B]±, REF[A:B]±)						
V_{DIFF}	Input Differential Voltage			400	V_{CC}	mV
V_{IHHP}	Highest Input HIGH Voltage			1.0	V_{CC}	V
V_{ILLP}	Lowest Input LOW Voltage			GND	$V_{CC} – 0.4$	V
V_{COM}	Common Mode Range (crossing voltage)			0.8	V_{CC}	V
Operating Current						
I_{CCI}	Internal Operating Current	CY7B993V	V_{CC} = Max., f_{MAX}[8]		TBD	mA
		CY7B994V			TBD	mA
I_{CCN}	Output Current Dissipation / Bank[7]	CY7B993V	V_{CC} = Max., C_{LOAD} = 25 pF, R_{LOAD} = 50Ω at $V_{CC}/2$, f_{MAX}		TBD	mA
		CY7B994V			TBD	mA

Capacitance

Parameter	Description	Test Conditions	Min.	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 3.3V	TBD	TBD	pF

Notes:

6. These inputs are normally wired to V_{CC}, GND, or left unconnected (actual threshold voltages vary as a percentage of V_{CC}). Internal termination resistors hold the unconnected inputs at $V_{CC}/2$. If these inputs are switched, the function and timing of the outputs may glitch and the PLL may require an additional t_{LOCK} time before all data sheet limits are achieved.
7. This is dependent upon frequency and number of outputs of a bank being loaded. The value indicates maximum I_{CCN} at maximum frequency and maximum load of 25 pF terminated to 50Ω at $V_{CC}/2$. For any other frequencies and load conditions the following equation can be used to calculate the maximum output current: TBD.
8. I_{CCI} measurement is performed with Bank1 and FB Bank configured to run at maximum frequency (f_{NOM} = 100 MHz for CY7B993V, f_{NOM} = 185 MHz for CY7B994V), and all other clock output banks to run at half the maximum frequency. FS and OUTPUT_MODE are asserted to the HIGH state.

Switching Characteristics Over the Operating Range[9, 10, 11, 12, 13]

Parameter	Description		CY7B993/4V-5 Min.	CY7B993/4V-5 Max.	CY7B993/4V-7 Min.	CY7B993/4V-7 Max.	Unit
f_{out}	Clock Output Frequency	CY7B993V		100		100	MHz
		CY7B994V		185		185	MHz
t_{SKEWPR}	Matched-Pair Skew[14, 15]			185		185	ps
$t_{SKEWBNK}$	Intrabank Skew[14, 15]			250		350	ps
t_{SKEW0}	Output-Output Skew (same frequency and phase, rise to rise, fall to fall)[14, 15]			550		750	ps
t_{SKEW1}	Output-Output Skew (same frequency and phase, other banks at different frequency, rise to rise, fall to fall)[14, 15]			650		850	ps
t_{SKEW2}	Output-Output Skew (invert to nominal of different banks, compared banks at same frequency, rising edge to falling edge aligned, other banks at same frequency)[14, 15]			700		1000	ps
t_{SKEW3}	Output-Output Skew (all output configurations outside of t_{SKEW1} and t_{SKEW2}.)[14, 15]			800		1100	ps
$t_{SKEWCPR}$	Complementary Outputs Skew (crossing to crossing, complementary outputs of the same bank)[14, 15, 16]			600		600	ps
t_{CCJ1-3}	Cycle-to-Cycle Jitter (divide by 1 output frequency, FB = divide by 1, 2, 3)			150		150	ps Peak-Peak
$t_{CCJ4-12}$	Cycle-to-Cycle Jitter (divide by 1 output frequency, FB = divide by 4, 5, 6, 8, 10, 12)			100		100	ps Peak-Peak
t_{PD}	Propagation Delay, REF to FB Rise		–500	500	–700	700	ps
$t_{PDDELTA}$	Propagation Delay difference between two devices.[17]			200		300	ps
t_{REFpwh}	REF input (Pulse Width HIGH)[18]		2.0		2.0		ns
t_{REFpwl}	REF input (Pulse Width LOW)[18]		2.0		2.0		ns
t_r/t_f	Output Rise/Fall Time[19]		0.15	2.0	0.15	2.0	ns
t_{LOCK}	PLL Lock TIme From Power-Up			10		10	ms
$t_{RELOCK1}$	PLL Re-Lock Time (from same frequency, different phase) with Stable Power Supply			500		500	µs
$t_{RELOCK2}$	PLL Re-Lock Time (from different frequency, different phase) with Stable Power Supply[20]			1000		1000	µs
t_{ODCV}	Output duty cycle deviation from 50%[13]		–1.0	1.0	–1.0	1.0	ns
t_{PWH}	Output HIGH time deviation from 50%[21]			1.5		1.5	ns
t_{PWL}	Output LOW time deviation from 50%[21]			2.0		2.0	ns
t_{PDEV}	Period deviation when changing from reference to reference[22]			TBD		TBD	UI

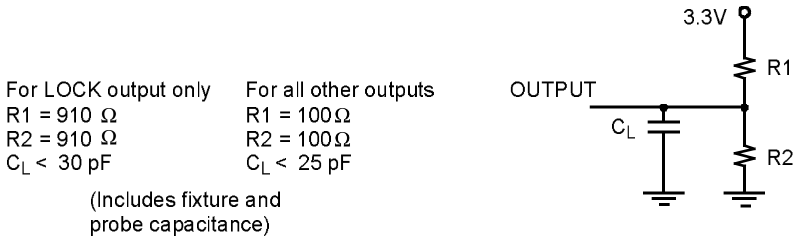
Notes:

9. This is for non-three level inputs.
10. Assumes 25 pF Max. Load Capacitance.
11. Both outputs of pair must be terminated, even if only one is being used.
12. Each package must be properly decoupled.
13. AC parameters are measured at 1.5V, unless otherwise indicated.
14. Test Load C_L = 25 pF, terminated to $V_{CC}/2$ with 50Ω.
15. SKEW is defined as the time between the earliest and the latest output transition among all outputs for which the same phase delay has been selected when all outputs are loaded with 25 pF and properly terminated.
16. Complementary output skews are measured at complementary signal pair intersections.
17. Guaranteed by statistical correlation. Tested initially and after any design or process changes that may affect these parameters.
18. Tested initially and after any design or process changes that may affect these parameters.
19. Rise and fall times are measured between 2.0V and 0.8V.
20. f_{NOM} must be within the frequency range defined by the same FS state.
21. t_{PWH} is measured at 2.0V. t_{PWL} is measured at 0.8V.
22. UI = Unit Interval. Examples: 1 UI is a full period. 0.1UI is 10% of period.

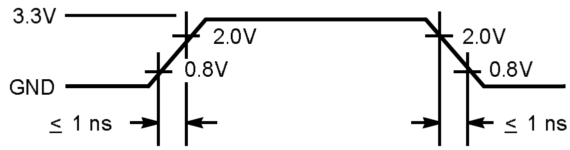
Switching Characteristics Over the Operating Range[9, 10, 11, 12, 13] (continued)

Parameter	Description	CY7B993/4V-5		CY7B993/4V-7		Unit
		Min.	Max.	Min.	Max.	
t_{OHZ}	DIS[1:4]/FBDIS HIGH to output high-impedance from HIGH[14, 23]	1.0	10	1.0	10	ns
t_{OLZ}	DIS[1:4]/FBDIS HIGH to output high-impedance from LOW[14, 23]	1.0	10	1.0	10	ns
t_{OZH}	DIS[1:4]/FBDIS LOW to output HIGH from output is high-impedance[24]	0.5[23]	14[25]	0.5[23]	14[25]	ns
t_{OZL}	DIS[1:4]/FBDIS LOW to output LOW from high-impedance[24]	0.5[23]	14[25]	0.5[23]	14[25]	ns

AC Test Loads and Waveform[26]



(a) LVTTL AC Test Load

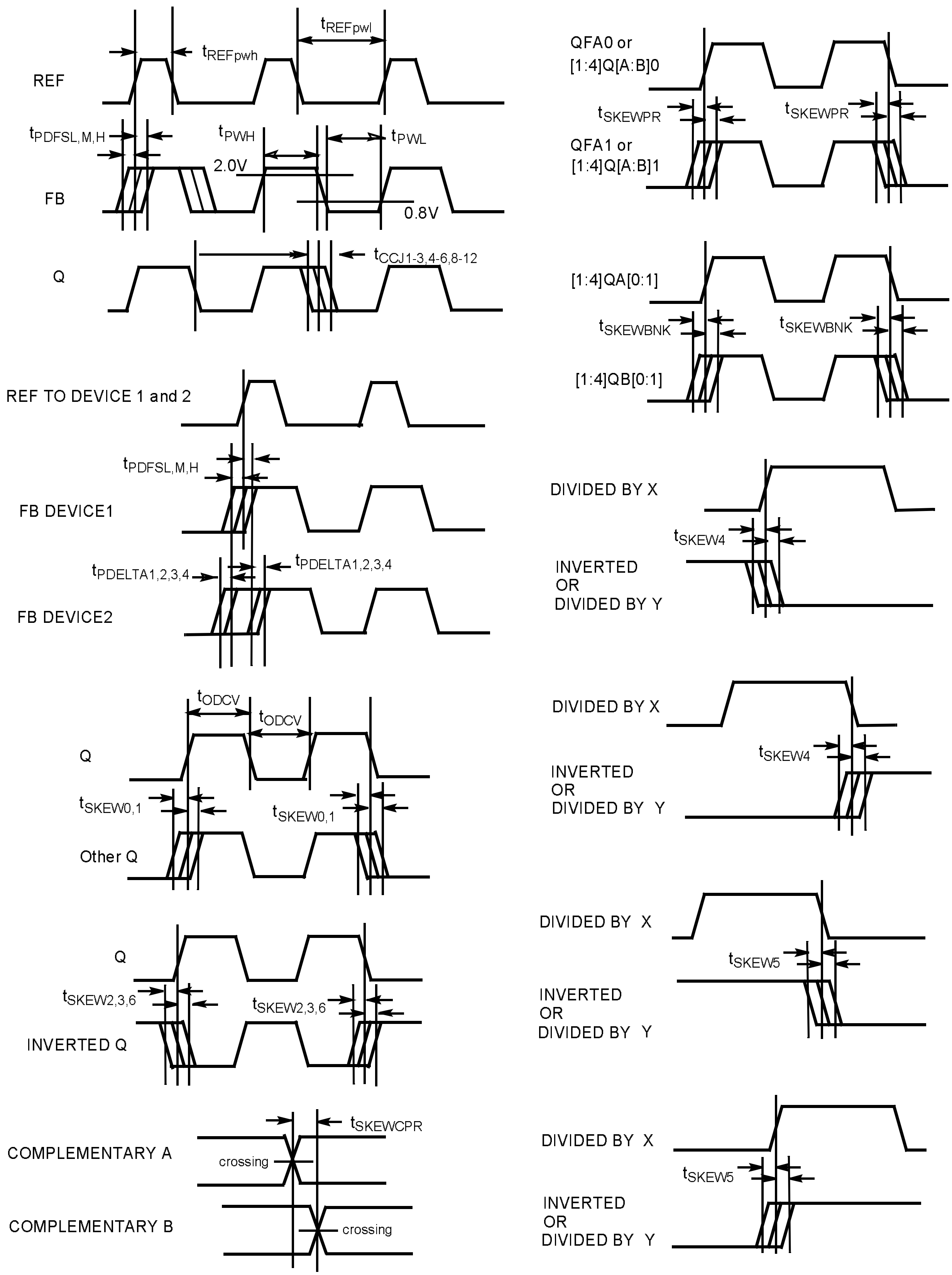


(b) TTL Input Test Waveform

Notes:

23. Measured at 0.5V deviation from starting voltage.
24. For t_{OZL} and t_{OZH} minimum, C_L = 0pF, R_L = 1k (to V_{CC} for t_{OZL}, to GND for t_{OZH}). For t_{OZL} and t_{OZH} maximum, CL= 25pF and RL = 100Ω (to V_{CC} for t_{OZL}, to GND for t_{OZH}).
25. t_{OZL} maximum is measured at 0.5V. t_{OZH} maximum is measured at 2.4V.
26. These figures are for illustrations only. The actual ATE loads may vary.

AC Timing Diagrams[13]



Ordering Information

Propagation Delay (ps)	Max. Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
500	100	CY7B993V-5AC	A100	100-Lead Thin Quad Flat Pack	Commercial
500	100	CY7B993V-5AI	A100	100-Lead Thin Quad Flat Pack	Industrial
500	185	CY7B994V-5AC	A100	100-Lead Thin Quad Flat Pack	Commercial
500	185	CY7B994V-5BBC	BB100	100-Ball Thin Ball Grid Array	
500	185	CY7B994V-5AI	A100	100-Lead Thin Quad Flat Pack	Industrial
700	100	CY7B993V-7AC	A100	100-Lead Thin Quad Flat Pack	Commercial
700	185	CY7B994V-7AC	A100	100-Lead Thin Quad Flat Pack	

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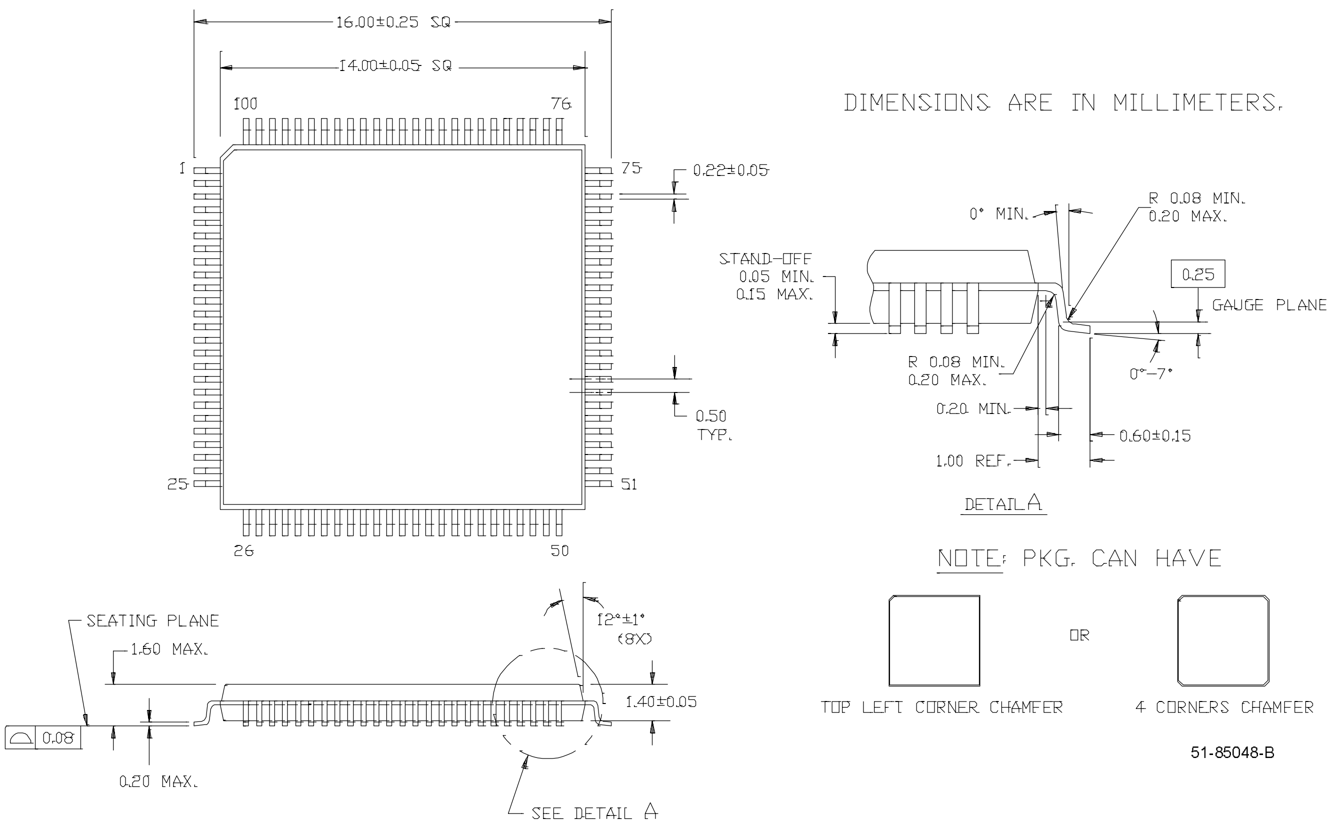
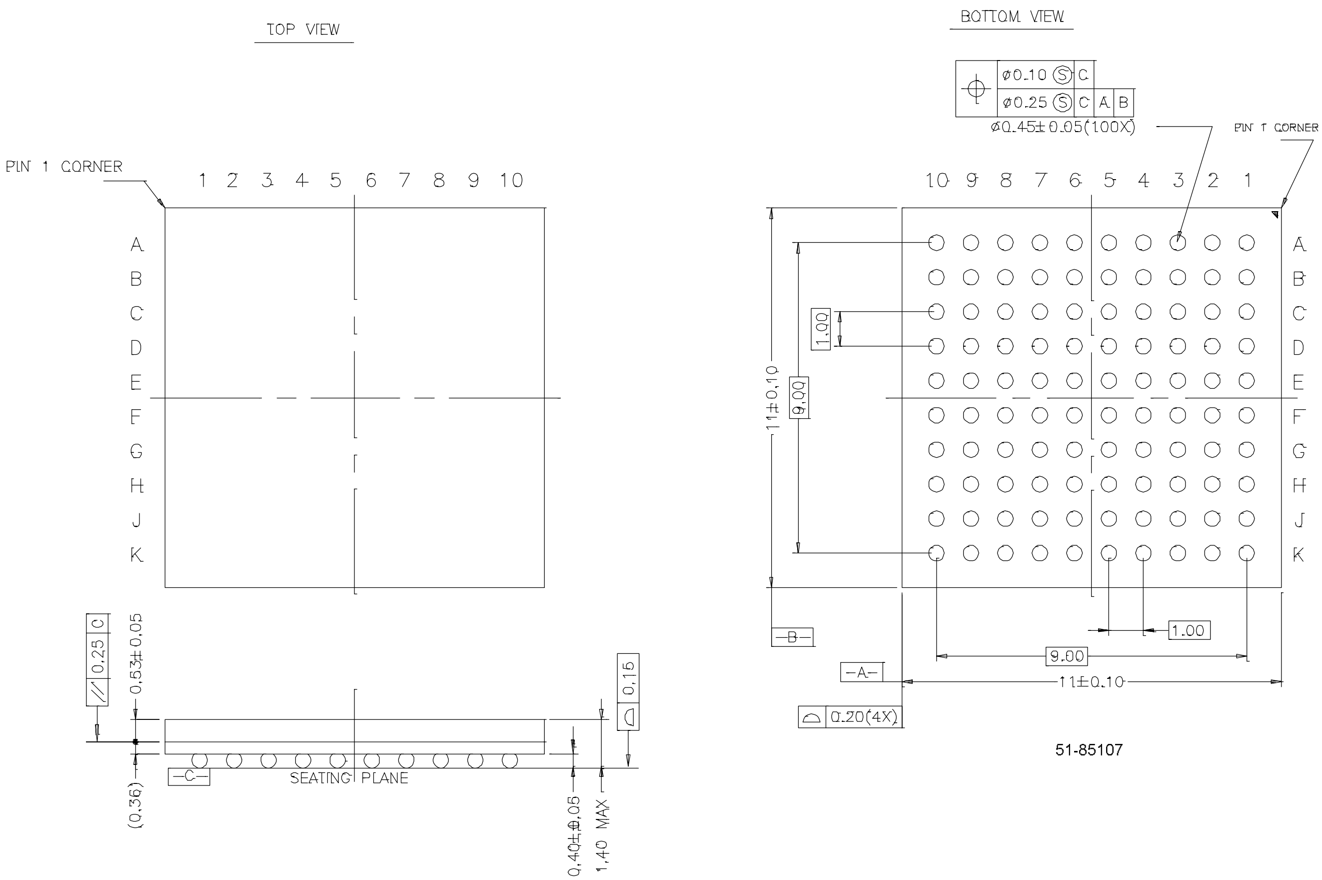
Package Diagrams

100-Pin Thin Plastic Quad Flat Pack (TQFP) A100



Package Diagrams (continued)

100-Ball Thin Ball Grid Array (11 x 11 x 1.4 mm) BB100



* THE BALL DIAMETER, BALL PITCH, STAND-OFF & PACKAGE THICKNESS ARE DIFFERENT FROM JEDEC SPEC M0192 (LOW PROFILE BGA FAMILY)

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