Dual Input SmartOR™ Power Switch

FEATURES

- Automatically selects V_{CC1} OR V_{CC2} input source
- Integrated low impedance switches (0.2Ω TYP)
- Operating supply range from 2.8V to 5.5V
- Glitch-free output during supply switching transitions
- Low operating supply current of 20µA (TYP)
- User-selectable hysteresis for supply selection
- 8-pin SOIC Narrow or 8-pin MSOP packages

APPLICATIONS

- PCI cards for Wake-On-LAN/Wake-On-Ring
- Dual power systems
- Systems with standby capabilities
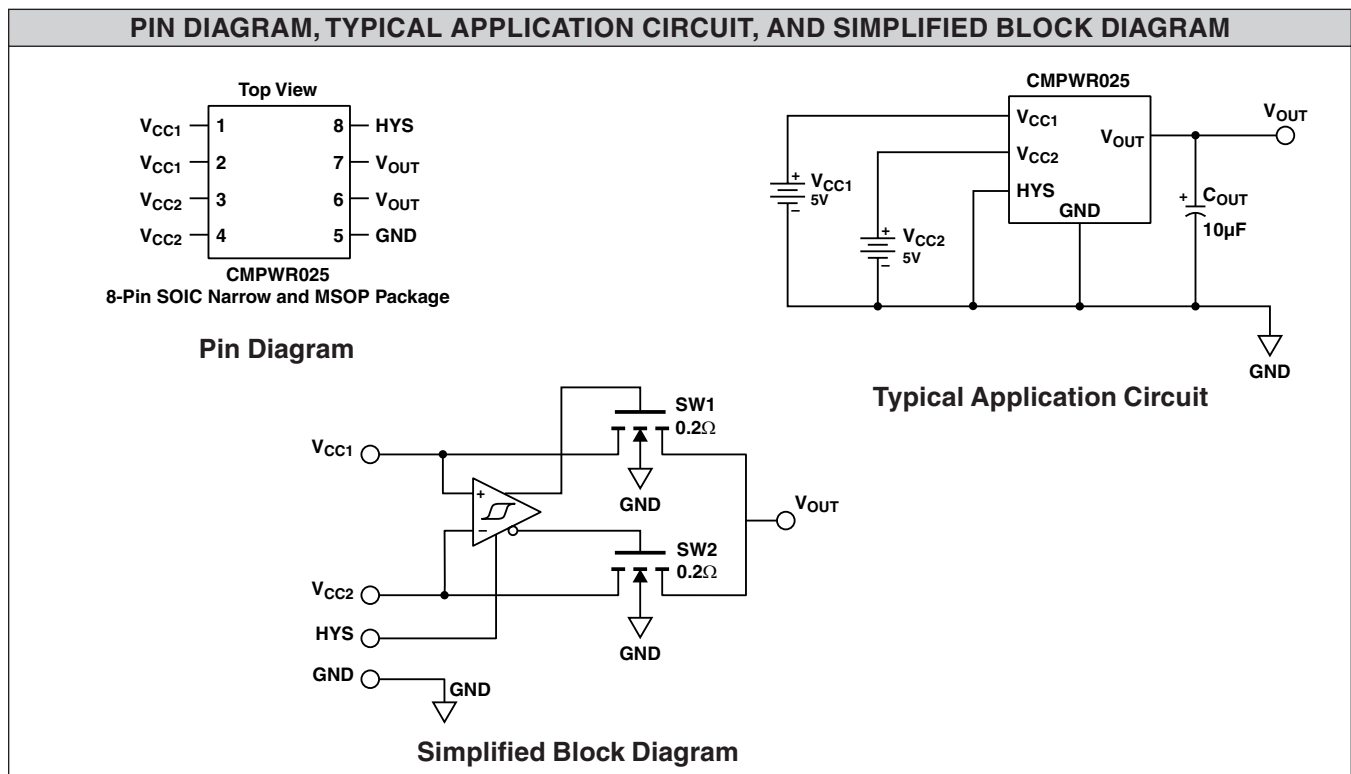- Battery backup systems
- See Application Note AP211

PRODUCT DESCRIPTION

California Micro Devices' SmartOR™ CMPWR025 is a dual input power switch that selects between two different power inputs and delivers it to one output. The device integrates two very low impedance power switches and automatically implements an OR function that selects the higher of the two inputs. A hysteresis is built in (and is user selectable) to prevent switch chatter.

The CMPWR025 is a much-improved solution to simply ORing two diodes, due to the greatly reduced losses of the CMPWR025 when compared to low forward drop Schottky diodes.

The CMPWR025 is designed to operate above the 1W (375mA at 3.3V) sleep mode rating stated in the PCI Rev 2.2 spec. In fact the CMPWR025 current rating is dependent upon the power dissipation resulting from the voltage drop across the internal switch elements. See the Typical DC Characteristics section in this data sheet for details.

For IAPC (Instantly Available Personal Computer) applications see the CAMD Applications Note AP211 "Instantly Available PCI Card Power Management".

PIN DIAGRAM, TYPICAL APPLICATION CIRCUIT, AND SIMPLIFIED BLOCK DIAGRAM

Pin Diagram

CMPWR025
8-Pin SOIC Narrow and MSOP Package

Typical Application Circuit

Simplified Block Diagram

C0970500

ABSOLUTE MAXIMUM RATINGS		
Parameter	Rating	Unit
ESD Protection (HBM)	2000	V
V_{CC1} V_{CC2} Input Voltage	+6.0, GND −0.5	V
Storage Temperature Range	−40 to +150	
Operating Ambient	0 to +70	°C
Operating Junction	0 to +125	
Maximum DC I_{OUT}	750	mA
Power Dissipation	0.3	W

OPERATING CONDITIONS		
Parameter	Rating	Unit
$V_{CC}1$, $V_{CC}2$ Input Voltage	2.8 to 5.5	V
Ambient Temperature	0 to 70	°C

ELECTRICAL OPERATING CHARACTERISTICS (over operating conditions unless specified otherwise)						
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CCDES1}	V_{CC1} Deselect Note 1	V_{CC1} Deselect level below V_{CC2} Pin 8 (HYS) floating	50	125	200	mV
V_{CCDES2}	V_{CC1} Deselect 2 Note 1	V_{CC1} Deselect level below V_{CC2} Pin 8 (HYS) grounded	90	200	300	mV
V_{CC1SEL}	V_{CC1} Select Preference Note 1		10	50	100	mV
V_{HYS1} V_{HYS2}	Hysteresis Note 1	V_{CC1SEL} − V_{CC1DES}, Pin 8 floating V_{CC1SEL} − V_{CC1DES}, Pin 8 grounded	40 80	75 150	100 200	mV mV
t_{DL} t_{DH}	Switching delay Note 3	$V_{CC1, 2}$ falltime < 100ns $V_{CC1, 2}$ risetime < 100ns		200 200		ns
R_{SW}	Switch Resistance	I_{LOAD} = 0 to 500mA $V_{CC1,2}$ = 2.8V		0.28	0.4	Ω
		I_{LOAD} = 0 to 500mA $V_{CC1,2}$ = 5.0V		0.21	0.3	Ω
V_{SW}	Voltage Drop Across Switch ($V_{CC1,2}$ − V_{OUT})	I_{OUT} = 100mA (V_{CC1}, V_{CC2} = 2.8V) I_{OUT} = 200mA (V_{CC1}, V_{CC2} = 2.8V) I_{OUT} = 500mA (V_{CC1}, V_{CC2} = 2.8V)		28 56 140	40 80 200	mV
		I_{OUT} = 100mA (V_{CC1}, V_{CC2} = 5V) I_{OUT} = 200mA (V_{CC1}, V_{CC2} = 5V) I_{OUT} = 500mA (V_{CC1}, V_{CC2} = 5V)		21 42 105	30 60 150	mV
I_{RCC1} I_{RCC2}	Reverse Leakage	V_{CC1} = 0V, V_{CC2} = 5V V_{CC1} = 5V, V_{CC2} = 0V			100 100	µA
I_{CC1}, I_{CC2}	Supply Current	When Selected (I_{OUT} = 0) When not Selected		20 1.0		µA
I_{GND}	Ground Pin Current	V_{CC1} = V_{CC2}, = 5V, I_{LOAD} = 0mA to 500mA		20	50	µA

Note 1: This parameter applies at 25°C only.
Note 2: Hysteresis level defines the maximum level of acceptable noise on V_{CC} during switching. Excessive parasitic inductance on V_{CC} board traces to the CMPWR025 may require an input capacitor to adequately filter the supply noise to below the hysteresis level. This will ensure that precise switching occurs between V_{CC1} and V_{CC2} supply inputs.
Note 3: This is the time, after the select/deselect threshold is reached, for the switches to react. Not tested, guaranteed by device design and characterization.

INTERFACE SIGNALS

V_{CC1} is the primary power source, which is given priority when present. If pin 8 (HYS) is unconnected, then the hysteresis level is 75mV (typ.). Whenever the primary power source drops below the secondary supply V_{CC2} by more than 125mV, it will immediately become deselected. When the primary power source is restored to within 50mV of the secondary supply, the primary power source will once again be selected and provide all the output current.

When V_{CC1} is selected, it will supply all the internal current requirements which are typically 20µA. When V_{CC1} is not selected, there will be no current loading on this input.

V_{CC2} is the secondary power source and is selected when the primary source has fallen below it by more than 125mV (or 200mV if pin 8 is grounded). The secondary source will be deselected immediately once the primary source is restored to within 50mV of V_{CC2}.

When V_{CC2} is selected, it will supply all the internal current requirements which are typically 20µA. When V_{CC2} is not selected, there will be no current loading on this input.

GND is the negative reference for all voltages.

V_{OUT} provides the power for the load. During normal operation the impedance from V_{OUT} to the selected supply is typically less than 0.28Ω, which results in minimal voltage loss from input to output.

During the cold-start interval when both inputs are initially applied, the internal circuitry provides a soft turn-on for the switches, which limits peak in-rush current.

HYS is the user-selectable hysteresis input. The hysteresis level is set to 150mV when grounding pin 8. The default hysteresis level is set to 75mV by leaving pin 8 unconnected. Using 150mV hysteresis is recommended, especially in environments with noisy power supplies, high power supply resistances or high load currents.

If the hysteresis level is set to 150mV, the primary supply V_{CC1} must now fall 200mV below the secondary supply V_{CC2} before it becomes deselected.

Important note: There is an internal connection between pins 1 and 2. These pins must be connected externally.

There is an internal connection between pins 3 and 4. These pins must be connected externally.

There is an internal connection between pins 6 and 7. These pins must be connected externally.

PIN FUNCTIONS		
Pin No.	**Symbol**	**Description**
1, 2	V_{CC1}	Primary Positive Supply input. This input must fall below the secondary input by more than 125mV (or 200mV if pin 8 is grounded) before it is deselected.
3, 4	V_{CC2}	Secondary Positive Supply input. This input will be deselected whenever the primary input has been restored to within 50mV of V_{CC2}.
5	GND	Negative reference for all voltages.
6, 7	V_{OUT}	Positive voltage output internally switched to either V_{CC1} or V_{CC2} input source. Pins 6 and 7 must be connected together externally.
8	HYS	Hysteresis adjust. Not Connected for 75mV hysteresis. Connect pin 8 to pin 5 (GND) for 150mV hysteresis.

SELECTION THRESHOLD DIAGRAMS
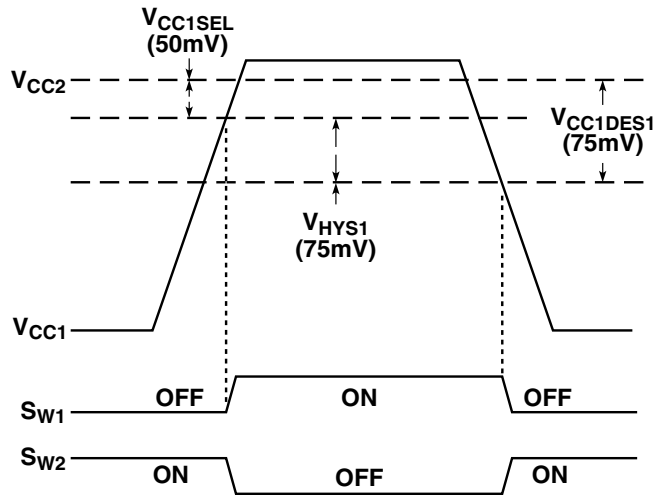
**Supply Selection Threshold Diagram (Hysteresis Pin Floating)**
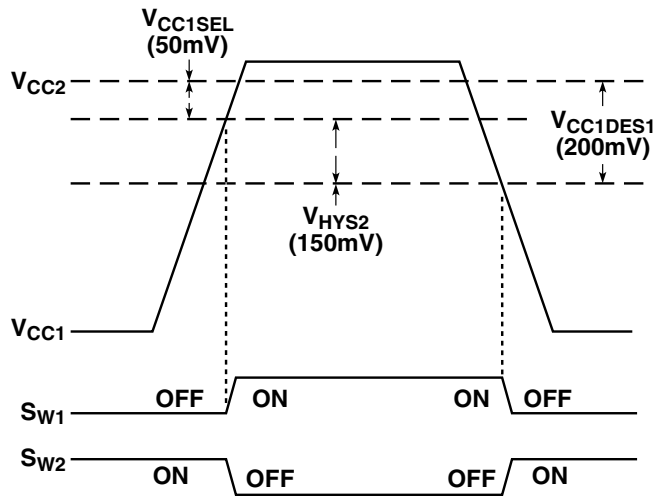
**Supply Selection Threshold Diagram (Hysteresis Pin Grounded)**

TYPICAL DC CHARACTERISTICS

Switch Resistance vs. V_{CC} with Temperature in Figure 1 shows the switch resistance measured at 500mA load, over a wide V_{CC} voltage range. The resistance is shown at ambient temperatures of 0°C, 25°C, and 70°C. When the temperature rises from 25°C to 70°C, the switch resistance increases by about 20%.
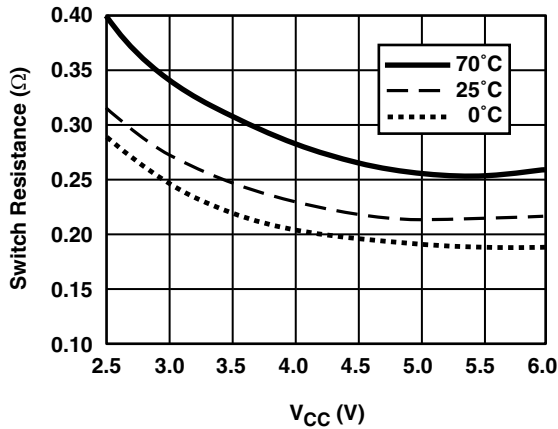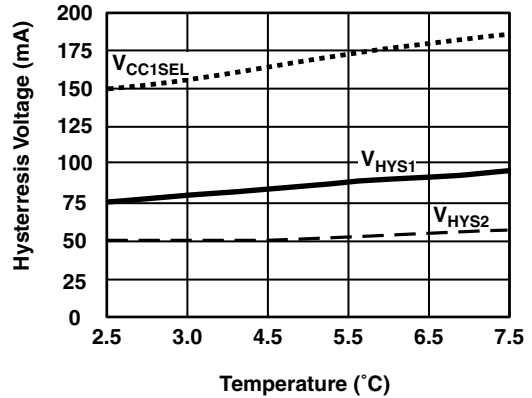

**Figure 1.
Switch Resistance vs. V_{CC} with Temperature**

Supply Current vs. V_{CC} with Temperature in Figure 2 shows how the small internal supply current varies with V_{CC} voltage and temperature. This current will be drawn from the selected V_{CC} input, and will be dissipated through ground pin 5. This current is independent of load current.
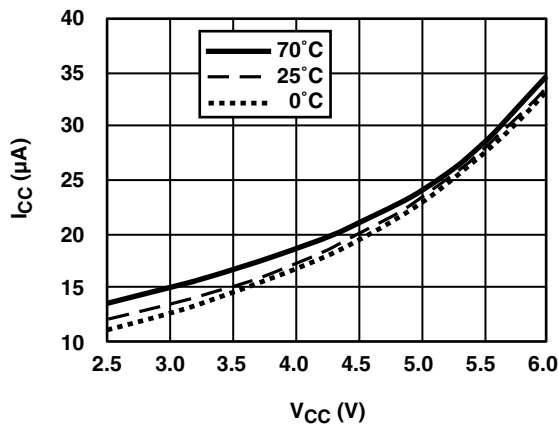
**Figure 2. Supply Current vs. V_{CC}
with Temperature (No Load)**

Figure 3. Hysteresis Voltage vs. Temperature

POWER DISSIPATION
AND OUTPUT CURRENT CONSIDERATION

The CMPWR025 is supplied in standard SOIC or MSOP packages, which have a maximum power dissipation rating of 0.3W. It is important that the heat generated within the part does not exceed this rating. The heat generated by the load current is given by:

$P_{DISS} = V_{SW} \times I_{LOAD}$ or $P_{DISS} = R_{SW} \times (I_{LOAD})^2$

At a typical load of 375mA the P_{DISS} is just $0.4 \times (0.375)^2 = 56mW$.

A primary consideration is Maximum Junction Temperature, $T_{J(max)}$, which can be calculated using the following formula:

$$T_{J(max)} = T_A + \theta_{JA} \times P_{DISS}$$

Where: T_A = The Ambient Temperature

θ_{JA} = Thermal Resistance = 100 °C/W

P_{DISS} = Power Dissipation

In the above example operating at an ambient of 70°C, $T_{j(max)}$ would be:

$T_{J(max)} = 70°C + (0.056W)(100°C/W) = 75.6°C$

Maximum power dissipation, including the power from the other circuitry within the device, suggests a current rating of approximately:

$$\sqrt{\frac{P_{DISS} - P_{INT}}{R_{SW}}} = I_{LOAD}$$

$$\sqrt{\frac{0.3W - 100\mu W}{0.4}} = 865mA$$

Note that this is beyond the maximum current rating of the device, which is to 750mA maximum.

TYPICAL TRANSIENT CHARACTERISTICS

The circuit schematic below shows the transient characterization test setup. It includes the power supply source impedances R_{S1} and R_{S2}, which represent the power supplies' output impedances and interconnection parasitics to the V_{CC1} and V_{CC2} input pins. In this test set-up, the series resistances on V_{CC1} and V_{CC2} are respectively $R_{S1} = 0.16\Omega$, and $R_{S2} = 0.06\Omega$, unless specified otherwise. A load resistance R_L of 11Ω is used, setting a load current of about 450mA at 5V.

The hysteresis level is increased by connecting pin 8 to ground, which will improve the transient performance in noisy environments. In the transient analysis, the rise time and fall time of V_{CC1} is very long, in the 20msec range, providing a worst case situation.

Important note: Power supply source impedance must be as low as possible to avoid chatter during power transition. When operating in a high load and long rise time power-up condition, we recommend not exceeding a value of 0.15Ω on both source resistances.

$$V_{HYS} > I(R_S + R_T)$$

Where: V_{HYS} = The Minimum Hysterisis Voltage = 80mV
R_S = The Power Supply Output Impedance
R_T = The PCB Trace Impedance

For a rated load of 500mA, $R_S + R_T < 0.15\Omega$.

Input and Output Capacitors

Filtering is typically unnecessary on the inputs, however power supply source impedance and parasitic resistance or inductance on the interconnections may result in chattering during the supply changeover. When an input is deselected and the input current drops to zero, the voltage at the input terminals will rise. If this voltage rise exceeds the hysteresis (75mV typical), the switch may chatter.

There are four ways to eliminate this chatter:

- Connect pin 8 to GND to select 150mV hysteresis,
- Position the device as close as possible to the power supply connectors,
- Use low-impedance PCB traces, or
- Include low-ESR input bypass capacitors at the V_{CC1} and V_{CC2} input pins. Capacitors of 10mF or greater are recommended.

V_{OUT} provides the power for the load. To ensure the output is glitch-free during dynamic switching of the inputs, it is recommended that an external capacitor of 10µF or greater is included. This will restrict any transient output disturbances to less than 300mV at 500mA loading during dynamic switching of the inputs.

The test set-up used in Figures 4 and 5 is described on page 5. The set-up for Figure 6 has larger series resistances on V_{CC1} and V_{CC2}.

V_{CC1} Rising from 0V to 5V/(V_{CC2} = 5V). Figure 4 shows the primary supply V_{CC1} becoming selected during a 0V to 5V transition. The secondary supply V_{CC2} is set to 5V DC. The channel 1 switch is turned on when V_{CC1} rises to within about 70mV of V_{CC2}. V_{CC1} drops when it is selected due to power supply source resistance R_{S1}. A positive glitch appears on V_{CC2} when channel 2 switch is turned off, due to power supply inductance. This has no effect on the output voltage.
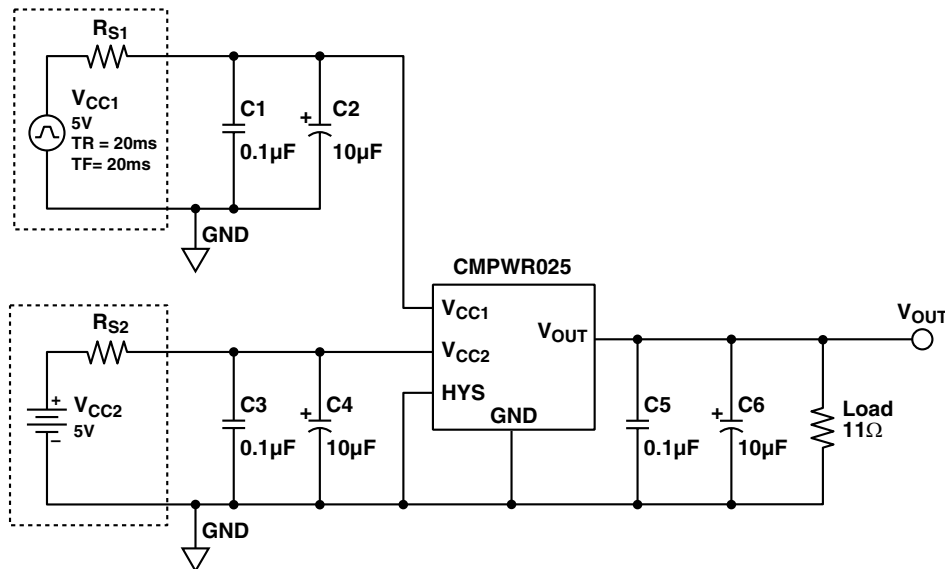

Transient Characterization Test Set-up
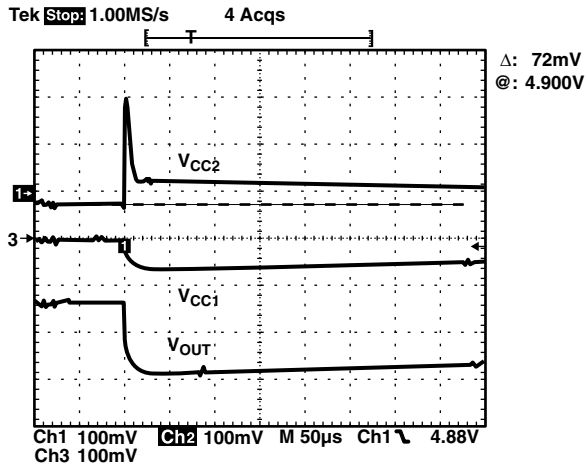
**Figure 4. V$_{CC1}$ rising from 0V to 5V, V$_{CC2}$ = 5V.
Ch1 and Ch2: V$_{CC1}$ and V$_{CC2}$, offset = 5V.
Ch3: V$_{OUT}$, offset = 5V.**

V$_{CC1}$ Falling from 5V to 0V (V$_{CC2}$ = 5V). Figure 5 shows the primary supply V$_{cc1}$ becoming deselected during a 5V to 0V transition. The test conditions are the same as in Figure 4. Channel 2 switch is turned on as soon as V$_{cc2}$ and V$_{cc1}$ are about 200mV. A negative glitch appears on V$_{cc2}$, when channel 2 is turned on. This has no effect on the output voltage.
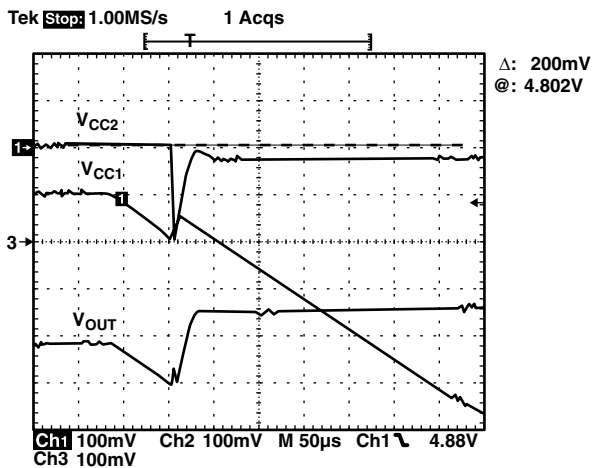
**Figure 5. V$_{CC1}$ falling from 0V to 5V (V$_{CC2}$ = 5V).
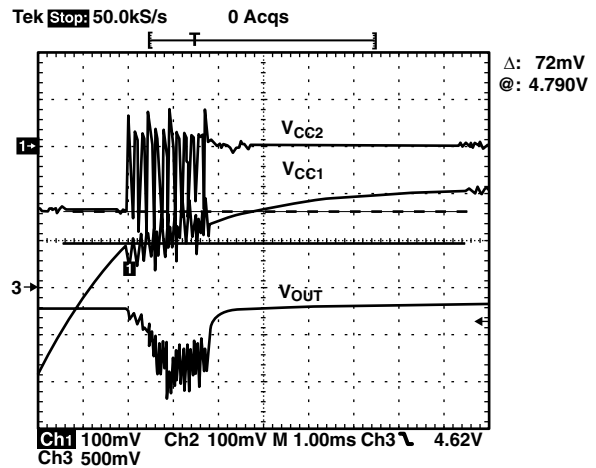Ch1 and Ch2: V$_{CC1}$ and V$_{CC2}$, offset = 5V.
Ch3: V$_{OUT}$, offset = 5V.**

V$_{CC1}$ Rising (V$_{CC2}$ = 5V). Figure 6 is a bad test set-up that shows what may happen if either power supply source resistance R$_{S1}$ or R$_{S2}$ is too large. In this example, R$_{S2}$ is increased to 0.3Ω.

The oscillation during the power transition is caused by the cumulated voltage change across R$_{S1}$ and R$_{S2}$ being greater than the hysteresis. The behavior is exacerbated by:

- a high load current,
- too many parasitics on power lines, and
- noisy power sources.

To avoid such behavior, the solution is to reduce the load or parasitic on power supply and layout, or use a more stable power supply.

See Application Note AP-211 for more information.

**Figure 6. V$_{CC1}$ Rising (V$_{CC2}$ @ = 5V).
Ch1 and Ch2: V$_{CC1}$ and V$_{CC2}$ @, offset = 5V.
Ch3: V$_{OUT}$, offset = 3.3V.**