Low Drift, Low Power Instrumentation Amplifier

AD621

FEATURES
EASY TO USE
Pin-Strappable Gains of 10 & 100
All Errors Specified for Total System Performance
Higher Performance than Discrete In-Amp Designs
Available in 8-Pin DIP and SOIC
Low Power, 1.3 mA max Supply Current
Wide Power Supply Range (±2.3 V to ±18 V)

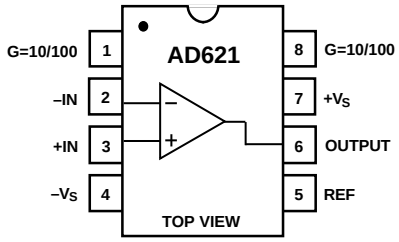
EXCELLENT DC PERFORMANCE
0.15% max, Total Gain Error
±5 ppm/°C, Total Gain Drift
125 μV max, Total Offset Voltage
1.0 μV/°C max, Offset Voltage Drift

LOW NOISE
9 nV/√Hz, @ 1 kHz, Input Voltage Noise
0.28 μV p-p Noise (0.1 Hz to 10 Hz)

EXCELLENT AC SPECIFICATIONS
800 kHz Bandwidth (G = 10), 200 kHz (G = 100)
12 μs Settling Time to 0.01%

APPLICATIONS
Weigh Scales
Transducer Interface & Data Acquisition Systems
Industrial Process Controls
Battery Powered and Portable Equipment

CONNECTION DIAGRAM
8-Pin Plastic Mini-DIP (N), Cerdip (Q) and SOIC (R) Packages

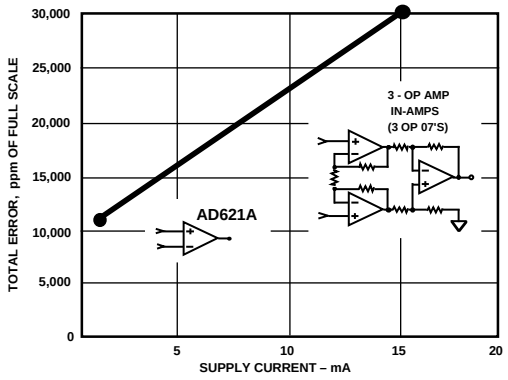


PRODUCT DESCRIPTION

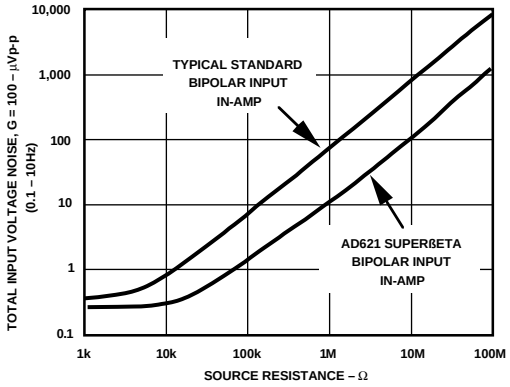
The AD621 is an easy to use, low cost, low power, high accuracy instrumentation amplifier which is ideally suited for a wide range of applications. Its unique combination of high performance, small size and low power, outperforms discrete in amp implementations. High functionality, low gain errors and low gain drift errors are achieved by the use of internal gain setting resistors. Fixed gains of 10 and 100 can be easily set via external pin strapping. The AD621 is fully specified as a total system, therefore, simplifying the design process.

For portable or remote applications, where power dissipation, size and weight are critical, the AD621 features a very low supply current of 1.3 mA max and is packaged in a compact 8-pin SOIC, 8-pin plastic DIP or 8-pin cerdip. The AD621 also excels in applications requiring high total accuracy, such as precision data acquisition systems used in weigh scales and transducer interface circuits. Low maximum error specifications including nonlinearity of 10 ppm, gain drift of 5 ppm/°C, 50 μV offset voltage and 0.6 μV/°C offset drift ("B" grade), make possible total system performance at a lower cost than has been previously achieved with discrete designs or with other monolithic instrumentation amplifiers.

When operating from high source impedances, as in ECG and blood pressure monitors, the AD621 features the ideal combination of low noise and low input bias currents. Voltage noise is specified as 9 nV/√Hz at 1 kHz and 0.28 μV p-p from 0.1 Hz to 10 Hz. Input current noise is also extremely low at 0.1 pA/√Hz. The AD621 outperforms FET input devices with an input bias current specification of 1.5 nA max over the full industrial temperature range.



Three Op Amp IA Designs vs. AD621



Total Voltage Noise vs. Source Resistance

REV. A

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Tel: 617/329-4700 **Fax: 617/326-8703**

AD621–SPECIFICATIONS

Gain = 10 (typical @ +25°C, V_S = ±15 V, and R_L = 2 kΩ, unless otherwise noted)

Model	Conditions	AD621A Min	AD621A Typ	AD621A Max	AD621B Min	AD621B Typ	AD621B Max	AD620S[1] Min	AD620S[1] Typ	AD620S[1] Max	Units
GAIN											
Gain Error	V_{OUT} = ±10 V			0.15			0.05			0.15	%
Nonlinearity,											
V_{OUT} = –10 V to +10 V	R_L = 2 kΩ		2	10		2	10		2	10	ppm of FS
Gain vs. Temperature			–1.5	±5		–1.5	±5		–1	±5	ppm/°C
TOTAL VOLTAGE OFFSET											
Offset (RTI)	V_S = ±15 V		75	250		50	125		75	250	µV
Over Temperature	V_S = ±5 V to ±15 V			400			215			500	µV
Average TC	V_S = ±5 V to ±15 V		1.0	2.5		0.6	1.5		1.0	2.5	µV/°C
Offset Referred to the											
Input vs. Supply (PSR)[2]	V_S = ±2.3 V to ±18 V	95	120		100	120		95	120		dB
Total NOISE											
Voltage Noise (RTI)	1 kHz		13	17		13	17		13	17	nV/√Hz
RTI	0.1 Hz to 10 Hz		0.55			0.55	0.8		0.55	0.8	µV p-p
Current Noise	f = 1 kHz		100			100			100		fA/√Hz
	0.1 Hz–10 Hz		10			10			10		pA p-p
INPUT CURRENT	V_S = ±15 V										
Input Bias Current			0.5	2.0		0.5	1.0		0.5	2	nA
Over Temperature				2.5			1.5			4	nA
Average TC			3.0			3.0			8.0		pA/°C
Input Offset Current			0.3	1.0		0.3	0.5		0.3	1.0	nA
Over Temperature				1.5			0.75			2.0	nA
Average TC			1.5			1.5			8.0		pA/°C
INPUT											
Input Impedance											
Differential			10‖2			10‖2			10‖2		GΩ‖pF
Common-Mode			10‖2			10‖2			10‖2		GΩ‖pF
Input Voltage Range[3]	V_S = ±2.3 V to ±5 V	$–V_S$ + 1.9		$+V_S$ – 1.2	$–V_S$ + 1.9		$+V_S$ – 1.2	$–V_S$ + 1.9		$+V_S$ – 1.2	V
Over Temperature		$–V_S$ + 2.1		$+V_S$ – 1.3	$–V_S$ + 2.1		$+V_S$ – 1.3	$–V_S$ + 2.1		$+V_S$ – 1.3	V
	V_S = ±5 V to ±l8 V	$–V_S$ + 1.9		$+V_S$ – 1.4	$–V_S$ + 1.9		$+V_S$ – 1.4	$–V_S$ + 1.9		$+V_S$ – 1.4	V
Over Temperature		$–V_S$ + 2.1		$+V_S$ – 1.4	$–V_S$ + 2.1		$+V_S$ – 1.4	$–V_S$ + 2.3		$+V_S$ – 1.4	V
Common-Mode Rejection											
Ratio DC to 60 Hz with											
1 kΩ Source Imbalance	V_{CM} = 0 V to ±10 V	93	110		100	110		93	110		dB
OUTPUT											
Output Swing	R_L = 10 kΩ,										
	V_S = ±2.3 V to ±5 V	$–V_S$ + 1.1		$+V_S$ – 1.2	$–V_S$ + 1.1		$+V_S$ – 1.2	$–V_S$ + 1.1		$+V_S$ – 1.2	V
Over Temperature		$–V_S$ + 1.4		$+V_S$ – 1.3	$–V_S$ + 1.4		$+V_S$ – 1.3	$–V_S$ + 1.6		$+V_S$ – 1.3	V
	V_S = ±5 V to ±18 V	$–V_S$ + 1.2		$+V_S$ – 1.4	$–V_S$ + 1.2		$+V_S$ – 1.4	$–V_S$ + 1.2		$+V_S$ – 1.4	V
Over Temperature		$–V_S$ + 1.6		$+V_S$ – 1.5	$–V_S$ + 1.6		$+V_S$ – 1.5	$–V_S$ + 2.3		$+V_S$ – 1.5	V
Short Current Circuit			±18			±18			±18		mA
DYNAMIC RESPONSE											
Small Signal,											
–3 dB Bandwidth			800			800			800		kHz
Slew Rate		0.75	1.2		0.75	1.2		0.75	1.2		V/µs
Settling Time to 0.01%	10 V Step		12			12			12		µs
REFERENCE INPUT											
R_{IN}			20			20			20		kΩ
I_{IN}	V_{IN} +, V_{REF} = 0		+50	+60		+50	+60		+50	+60	µA
Voltage Range		$–V_S$ + 1.6		$+V_S$ – 1.6	$–V_S$ + 1.6		$+V_S$ – 1.6	V_S + 1.6		$+V_S$ – 1.6	V
Gain to Output			1 ± 0.0001			1 ± 0.0001			1 ± 0.0001		
POWER SUPPLY											
Operating Range		±2.3		±18	±2.3		±18	±2.3		±18	V
Quiescent Current	V_S = ±2.3 V to ±18 V		0.9	1.3		0.9	1.3		0.9	1.3	mA
Over Temperature			1.1	1.6		1.1	1.6		1.1	1.6	mA
TEMPERATURE RANGE											
For Specified Performance			–40 to +85			–40 to +85			–55 to +125		°C

NOTES

[1]See Analog Devices military data sheet for 883B tested specifications.

[2]This is defined as the supply range over which PSRR is defined.

[3]Input Voltage Range = CMV + (Gain × V_{DIFF}).

Specifications subject to change without notice.

Gain = 100 (typical @ +25°C, V_S = ±15 V, and R_L = 2 kΩ, unless otherwise noted)

Model	Conditions	AD621A Min	AD621A Typ	AD621A Max	AD621B Min	AD621B Typ	AD621B Max	AD620S[1] Min	AD620S[1] Typ	AD620S[1] Max	Units
GAIN											
Gain Error	V_{OUT} = ±10 V			0.15			0.05			0.15	%
Nonlinearity,											
V_{OUT} = –10 V to +10 V	R_L = 2 kΩ		2	10		2	10		2	10	ppm of FS
Gain vs. Temperature			–1	±5		–1	±5		–1	±5	ppm/°C
TOTAL VOLTAGE OFFSET											
Offset (RTI)	V_S = ±15 V		35	125		25	50		35	125	µV
Over Temperature	V_S = ±5 V to ±15 V			185			215			225	µV
Average TC	V_S = ±5 V to ±15 V		0.3	1.0		0.1	0.6		0.3	1.0	µV/°C
Offset Referred to the											
Input vs. Supply (PSR)[2]	V_S = ±2.3 V to ±18 V	110	140		120	140		110	140		dB
Total NOISE											
Voltage Noise (RTI)	1 kHz		9	13		9	13		9	13	nV/√Hz
RTI	0.1 Hz to 10 Hz		0.28			0.28	0.4		0.28	0.4	µV p-p
Current Noise	f = 1 kHz		100			100			100		fA/√Hz
	0.1 Hz–10 Hz		10			10			10		pA p-p
INPUT CURRENT	V_S = ±15 V										
Input Bias Current			0.5	2.0		0.5	1.0		0.5	2	nA
Over Temperature				2.5			1.5			4	nA
Average TC			3.0			3.0			8.0		pA/°C
Input Offset Current			0.3	1.0		0.3	0.5		0.3	1.0	nA
Over Temperature				1.5			0.75			2.0	nA
Average TC			1.5			1.5			8.0		pA/°C
INPUT											
Input Impedance											
Differential			10‖2			10‖2			10‖2		GΩ‖pF
Common-Mode			10‖2			10‖2			10‖2		GΩ‖pF
Input Voltage Range[3]	V_S = ±2.3 V to ±5 V	$–V_S$ + 1.9		$+V_S$ – 1.2	$–V_S$ + 1.9		$+V_S$ – 1.2	$–V_S$ + 1.9		$+V_S$ – 1.2	V
Over Temperature		$–V_S$ + 2.1		$+V_S$ – 1.3	$–V_S$ + 2.1		$+V_S$ – 1.3	$–V_S$ + 2.1		$+V_S$ – 1.3	V
	V_S = ±5 V to ±l8 V	$–V_S$ + 1.9		$+V_S$ – 1.4	$–V_S$ + 1.9		$+V_S$ – 1.4	$–V_S$ + 1.9		$+V_S$ – 1.4	V
Over Temperature		$–V_S$ + 2.1		$+V_S$ – 1.4	$–V_S$ + 2.1		$+V_S$ – 1.4	$–V_S$ + 2.3		$+V_S$ – 1.4	V
Common-Mode Rejection											
Ratio DC to 60 Hz with											
1 kΩ Source Imbalance	V_{CM} = 0 V to ±10 V	110	130		120	130		110	130		dB
OUTPUT											
Output Swing	R_L = 10 kΩ,										
	V_S = ±2.3 V to ±5 V	$–V_S$ + 1.1		$+V_S$ – 1.2	$–V_S$ + 1.1		$+V_S$ – 1.2	$–V_S$ + 1.1		$+V_S$ – 1.2	V
Over Temperature		$–V_S$ + 1.4		$+V_S$ – 1.3	$–V_S$ + 1.4		$+V_S$ – 1.3	$–V_S$ + 1.6		$+V_S$ – 1.3	V
	V_S = ±5 V to ±18 V	$–V_S$ + 1.2		$+V_S$ – 1.4	$–V_S$ + 1.2		$+V_S$ – 1.4	$–V_S$ + 1.2		$+V_S$ – 1.4	V
Over Temperature		$–V_S$ + 1.6		$+V_S$ – 1.5	$–V_S$ + 1.6		$+V_S$ – 1.5	$–V_S$ + 2.3		$+V_S$ – 1.5	V
Short Current Circuit			±18			±18			±18		mA
DYNAMIC RESPONSE											
Small Signal,											
–3 dB Bandwidth			200			200			200		kHz
Slew Rate		0.75	1.2		0.75	1.2		0.75	1.2		V/µs
Settling Time to 0.01%	10 V Step		12			12			12		µs
REFERENCE INPUT											
R_{IN}			20			20			20		kΩ
I_{IN}	V_{IN} +, V_{REF} = 0		+50	+60		+50	+60		+50	+60	µA
Voltage Range		$–V_S$ + 1.6		$+V_S$ – 1.6	$–V_S$ + 1.6		$+V_S$ – 1.6	V_S + 1.6		$+V_S$ – 1.6	V
Gain to Output			1 ± 0.0001			1 ± 0.0001			1 ± 0.0001		
POWER SUPPLY											
Operating Range		±2.3		±18	±2.3		±18	±2.3		±18	V
Quiescent Current	V_S = ±2.3 V to ±18 V		0.9	1.3		0.9	1.3		0.9	1.3	mA
Over Temperature			1.1	1.6		1.1	1.6		1.1	1.6	mA
TEMPERATURE RANGE											
For Specified Performance			–40 to +85			–40 to +85			–55 to +125		°C

NOTES

[1]See Analog Devices military data sheet for 883B tested specifications.

[2]This is defined as the supply range over which PSEE is defined.

[3]Input Voltage Range = CMV + (Gain × V_{DIFF}).

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Internal Power Dissipation[2] . . . . . 650 mW
Input Voltage (Common Mode) . . . . . $\pm V_S$
Differential Input Voltage . . . . . ±25 V
Output Short Circuit Duration . . . . . Indefinite
Storage Temperature Range (Q) . . . . . –65°C to +150°C
Storage Temperature Range (N, R) . . . . . –65°C to +125°C
Operating Temperature Range
AD621 (A, B) . . . . . –40°C to +85°C
AD621 (S) . . . . . –55°C to +125°C
Lead Temperature Range
(Soldering 10 seconds) . . . . . +300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Specification is for device in free air:
8-Pin Plastic Package: θ_{JA} = 95°C/Watt
8-Pin Cerdip Package: θ_{JA} = 110°C/Watt
8-Pin SOIC Package: θ_{JA} = 155°C/Watt

ESD SUSCEPTIBILITY

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 volts, which readily accumulate on the human body and on test equipment, can discharge without detection. Although the AD621 features proprietary ESD protection circuitry, permanent damage may still occur on these devices if they are subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid any performance degradation or loss of functionality.

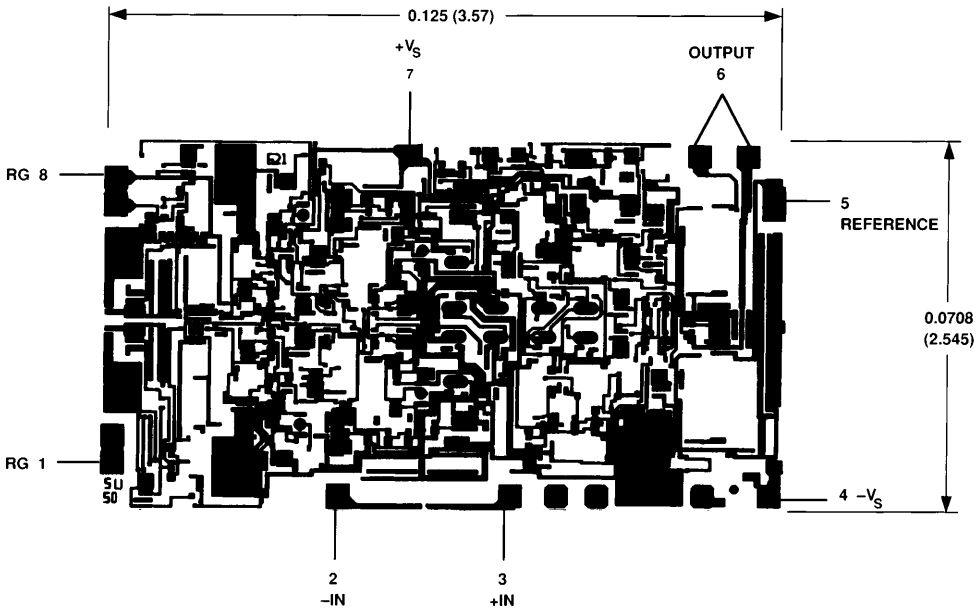
ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option[1]
AD621AN	–40°C to +85°C	8-Pin Plastic DIP	N-8
AD621BN	–40°C to +85°C	8-Pin Plastic DIP	N-8
AD621AR	–40°C to +85°C	8-Pin Plastic SOIC	R-8
AD621BR	–40°C to +85°C	8-Pin Plastic SOIC	R-8
AD621SQ/883B[2]	–55°C to +125°C	8-Pin Cerdip	Q-8
AD621ACHIPS	–40°C to +85°C	Die	

NOTES
[1]N = Plastic DIP; Q = Cerdip; R = SOIC.
[2]See Analog Devices' military data sheet for 883B specifications.

METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).
Contact factory for latest dimensions.



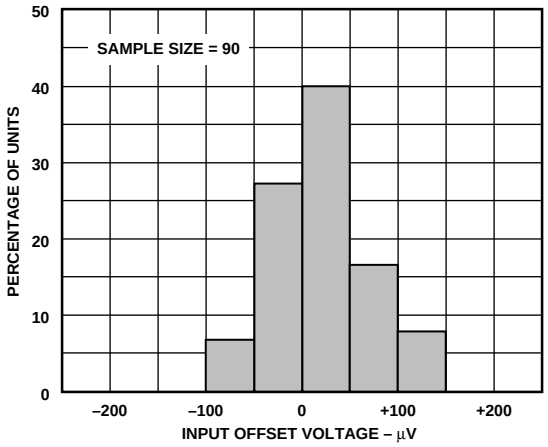


Figure 1. Typical Distribution of $V_{OS,}$ Gain = 10

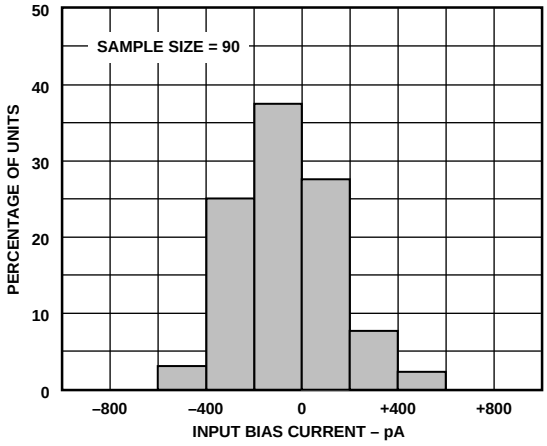


Figure 4. Typical Distribution of Input Bias Current

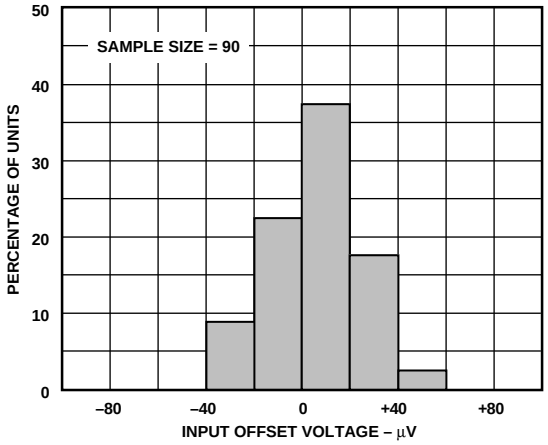


Figure 2. Typical Distribution of V_{OS}, Gain = 100

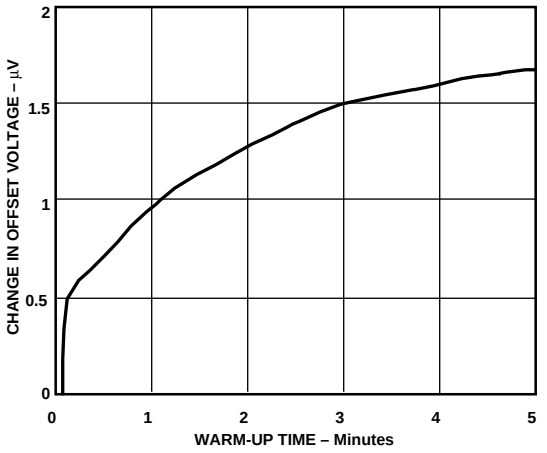


Figure 5. Change in Input Offset Voltage vs. Warm-Up Time

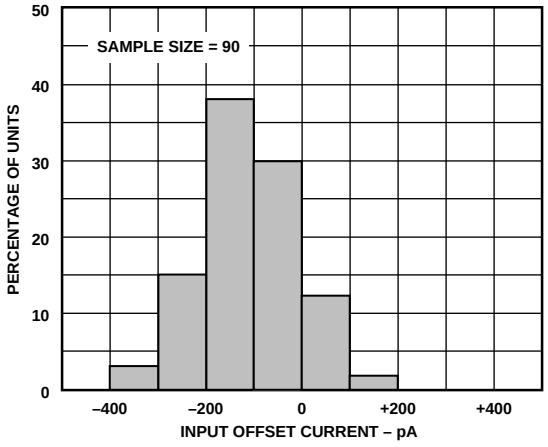


Figure 3. Typical Distribution of Input Offset Current

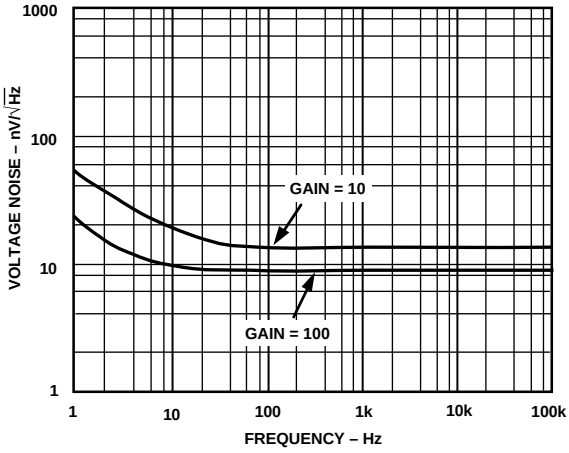


Figure 6. Voltage Noise Spectral Density

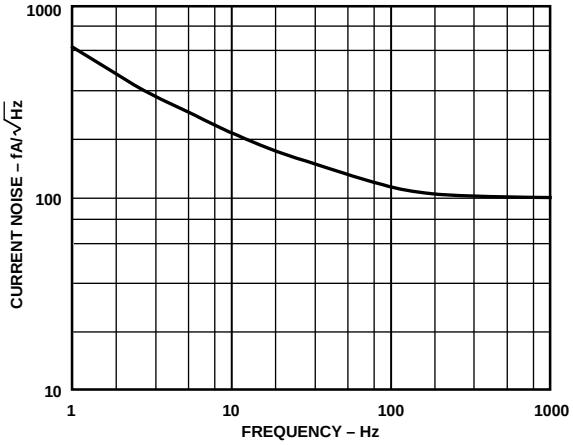


Figure 7. Current Noise Spectral Density vs. Frequency

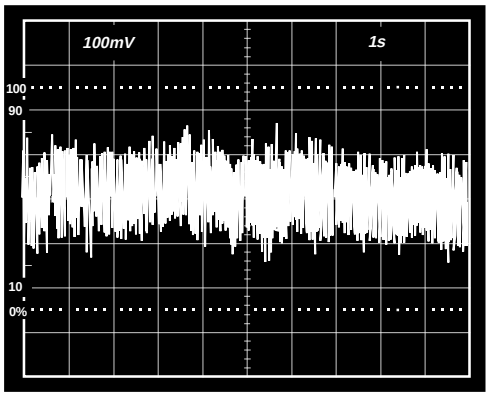


Figure 9. 0.1 Hz to 10 Hz Current Noise, 5 pA per Vertical Div, 1 Second per Horizontal Div

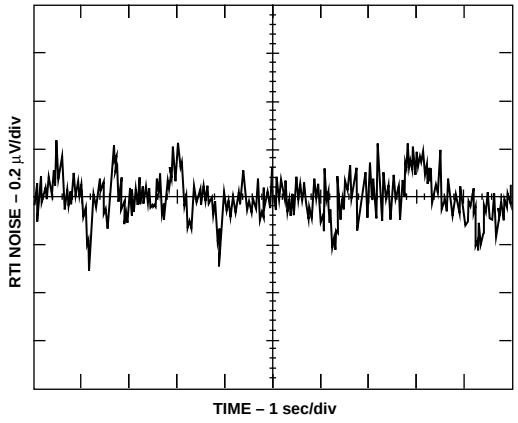


Figure 8a. 0.1 Hz to 10 Hz RTI Voltage Noise, Gain = 10

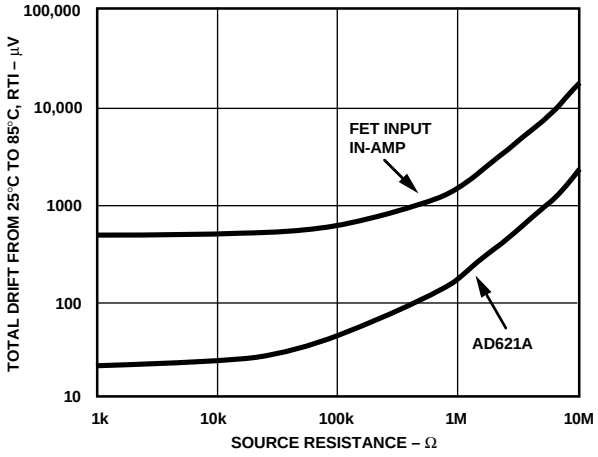


Figure 10. Total Drift vs. Source Resistance

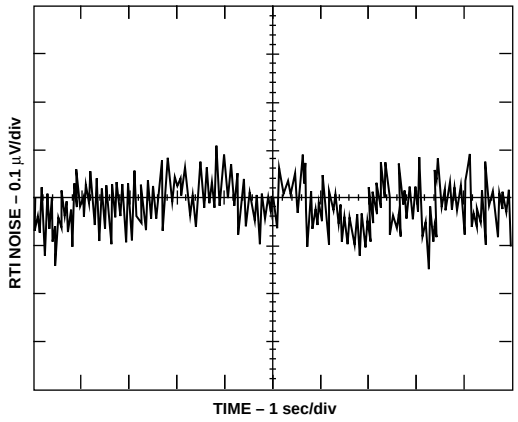


Figure 8b. 0.1 Hz to 10 Hz RTI Voltage Noise, G = 100

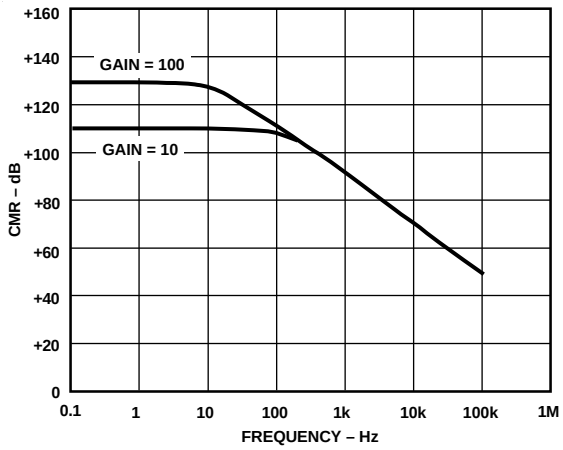


Figure 11. CMR vs. Frequency, RTI, for a Zero to 1 kΩ Source Imbalance

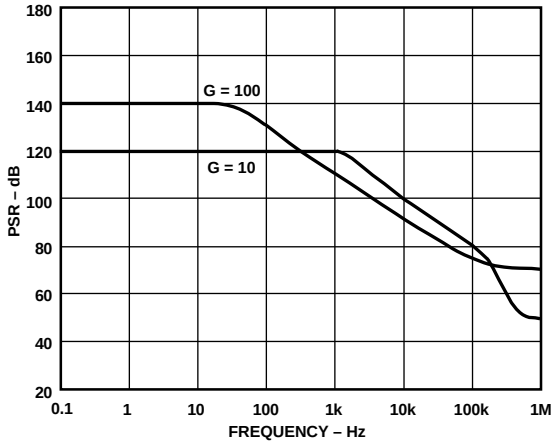


Figure 12. Positive PSR vs. Frequency

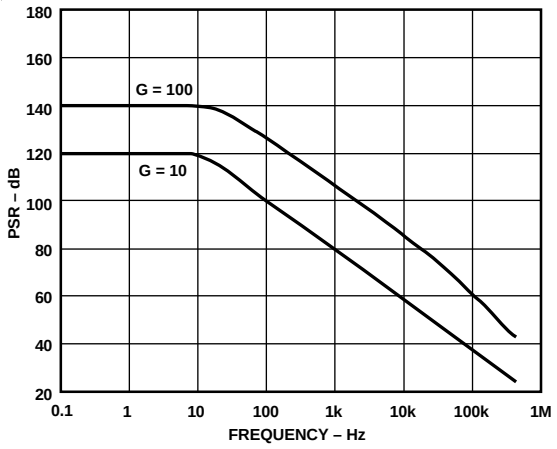


Figure 13. Negative PSR vs. Frequency

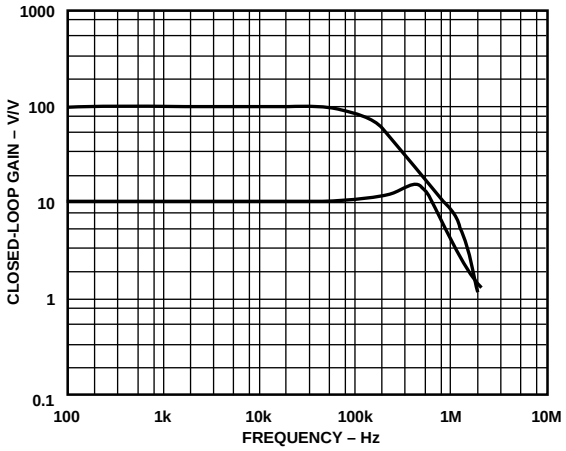


Figure 14. Closed-Loop Gain vs. Frequency

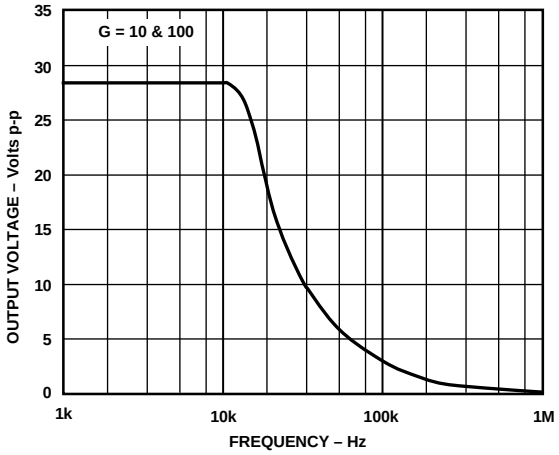


Figure 15. Large Signal Frequency Response

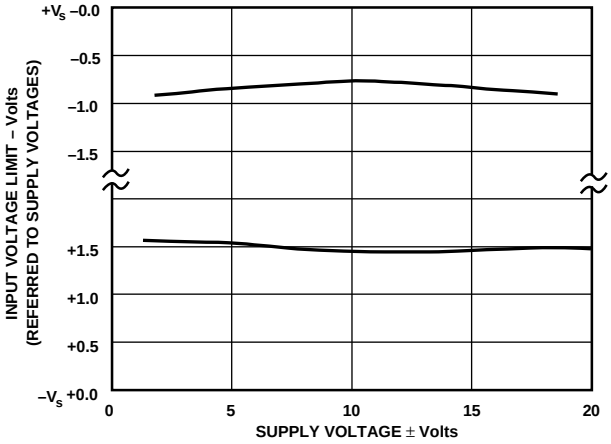


Figure 16. Input Voltage Range vs. Supply Voltage

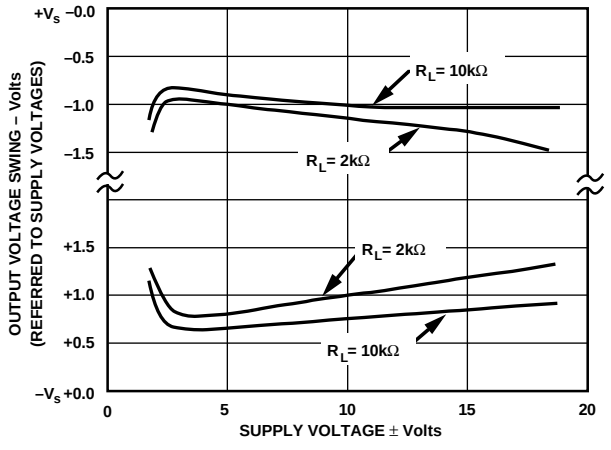


Figure 17. Output Voltage Swing vs. Supply Voltage, G = 10

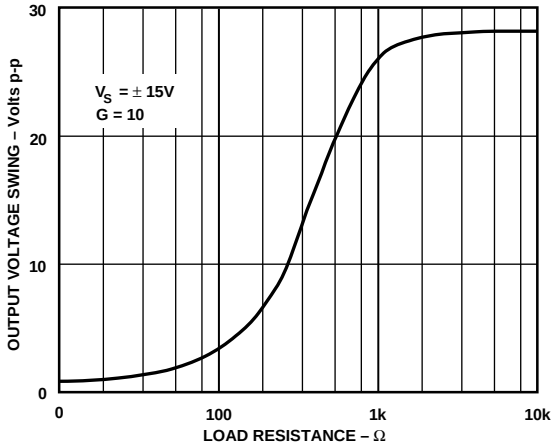


Figure 18. Output Voltage Swing vs. Resistive Load

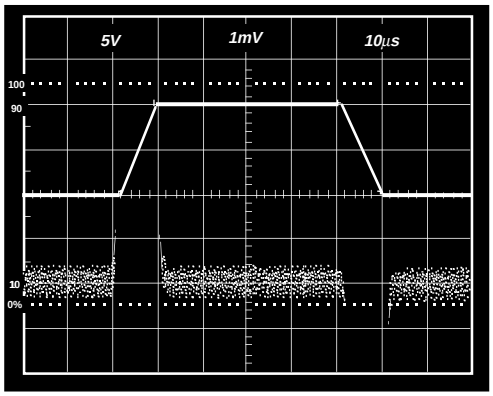


Figure 21. Large Signal Pulse Response and Settling Time, G = 100 (0.5 mV = 0.1%), R_L = 2 kΩ, C_L = 100 pF

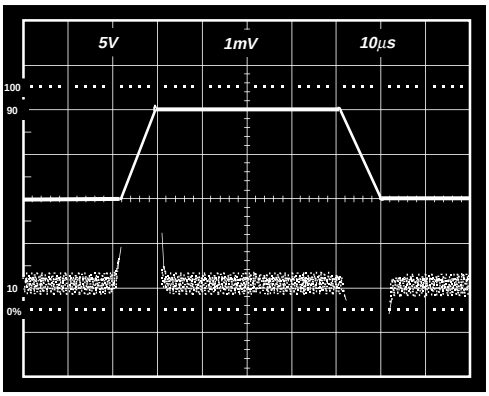


Figure 19. Large Signal Pulse Response and Settling Time Gain, G = 10 (0.5 mV = 0.01%), R_L = 1 k Ω, C_L = 100 pF

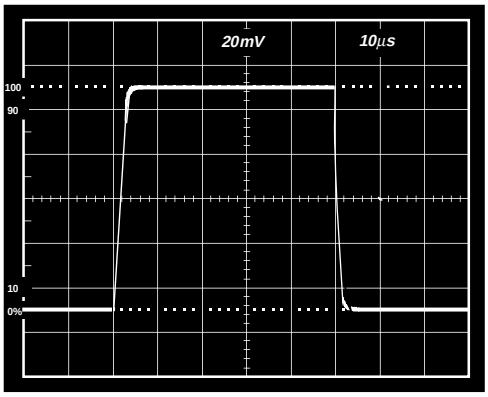


Figure 22. Small Signal Pulse Response, G = 100, R_L = 2 kΩ, C_L = 100 pF

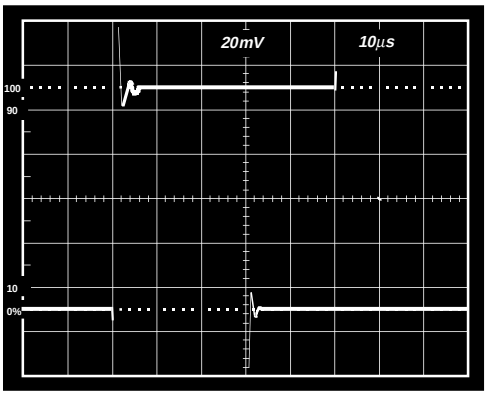


Figure 20. Small Signal Pulse Response, G = 10, R_L = 1 k Ω, C_L = 100 pF

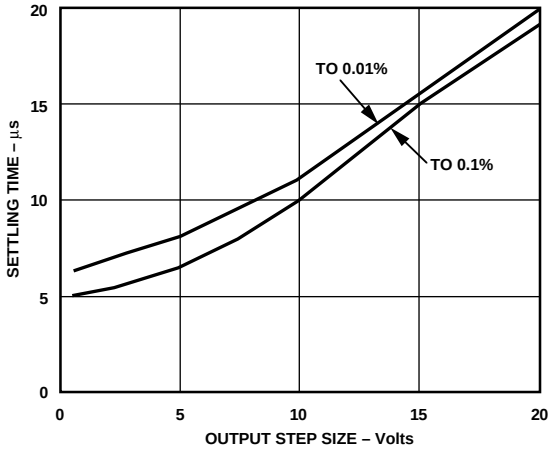


Figure 23. Settling Time vs. Step Size, G = 10

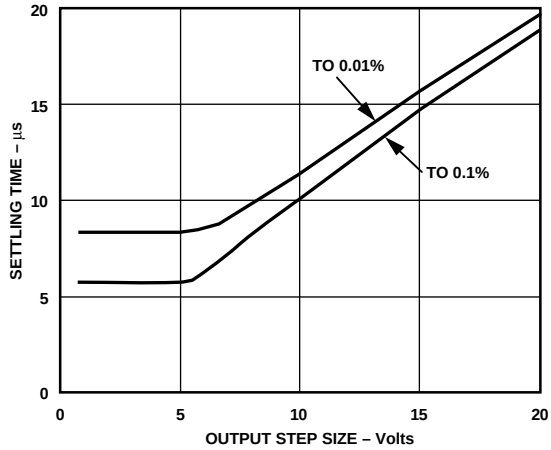


Figure 24. Settling Time vs. Step Size, Gain = 100

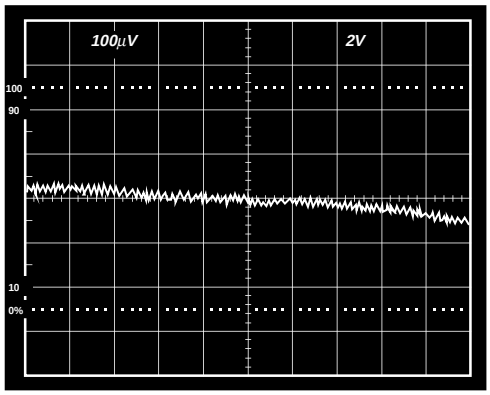


Figure 27. Gain Nonlinearity, G = 10, R_L = 10 kΩ, Vertical Scale: 100 µV/Div = 100 ppm/Div, Horizontal Scale: 2 Volts/Div

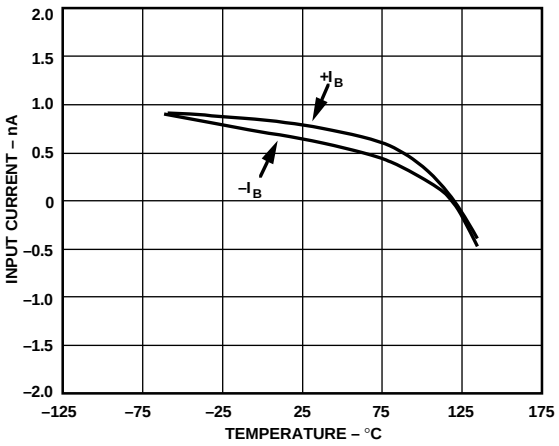


Figure 25. Input Bias Current vs. Temperature

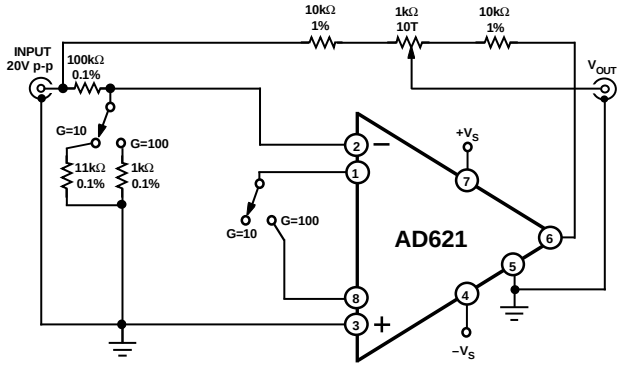


Figure 28. Settling Time Test Circuit

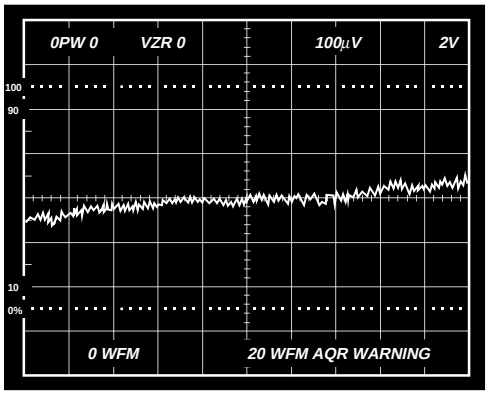


Figure 26. Gain Nonlinearity, G = 100, R_L = 10 kΩ, C_L = 0 pF. Vertical Scale: 100 µV/Div = 100 ppm/Div Horizontal Scale: 2 Volts/Div

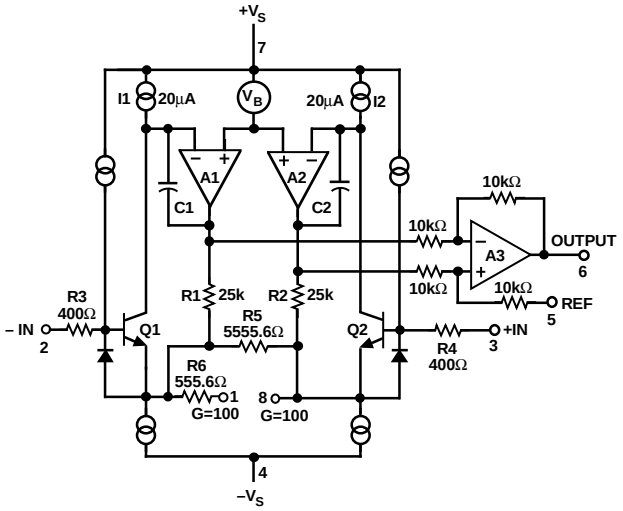


Figure 29. Simplified Schematic of AD621

THEORY OF OPERATION

The AD621 is a monolithic instrumentation amplifier based on a modification of the classic three op amp circuit. Careful layout of the chip, with particular attention to thermal symmetry builds in tight matching and tracking of critical components, thus preserving the high level of performance inherent in this circuit, at a low price.

On chip gain resistors are pretrimmed for gains of 10 and 100. The AD621 is preset to a gain of 10. A single external jumper (between Pins 1 and 8) is all that is needed to select a gain of 100. Special design techniques assure a low gain TC of 5 ppm/°C max, even at a gain of 100.

Figure 29 is a simplified schematic of the AD621. The input transistors Q1 and Q2 provide a single differential-pair bipolar input for high precision, yet offer 10× lower Input Bias Current, thanks to Superβeta processing. Feedback through the Q1-A1-R1 loop and the Q2-A2-R2 loop maintains constant collector current of the input devices Q1 and Q2, thereby impressing the input voltage across the gain-setting resistor, RG, which equals R5 at a gain of 10 or the parallel combination of R5 and R6 at a gain of 100.

This creates a differential gain from the inputs to the A1/A2 outputs given by G = (R1 + R2) / RG + 1. The unity-gain subtracter A3 removes any common-mode signal, yielding a single-ended output referred to the REF pin potential.

The value of RG also determines the transconductance of the preamp stage. As RG is reduced for larger gains, the transconductance increases asymptotically to that of the input transistors. This has three important advantages: (a) Open-loop gain is boosted for increasing programmed gain, thus reducing gain-related errors. (b) The gain-bandwidth product (determined by C1, C2 and the preamp transconductance) increases with programmed gain, thus optimizing frequency response. (c) The input voltage noise is reduced to a value of 9 nV/$\sqrt{\text{Hz}}$, determined mainly by the collector current and base resistance of the input devices.

Make vs. Buy: A Typical Bridge Application Error Budget

The AD621 offers improved performance over discrete three op amp IA designs, along with smaller size, fewer components and 10 times lower supply current. In the typical application, shown in Figure 30, a gain of 100 is required to amplify a bridge output of 20 mV full scale over the industrial temperature range of –40°C to +85°C. The error budget table below shows how to calculate the effect various error sources have on circuit accuracy.

Regardless of the system it is being used in, the AD621 provides greater accuracy, and at low power and price. In simple systems, absolute accuracy and drift errors are by far the most significant contributors to error. In more complex systems with an intelligent processor, an auto-gain/auto-zero cycle will remove all absolute accuracy and drift errors leaving only the resolution errors of gain nonlinearity and noise, thus allowing full 14-bit accuracy.

Note that for the discrete circuit, the OP07 specifications for input voltage offset and noise have been multiplied by 2. This is because a three op amp type in amp has two op amps at its inputs, both contributing to the overall input error.

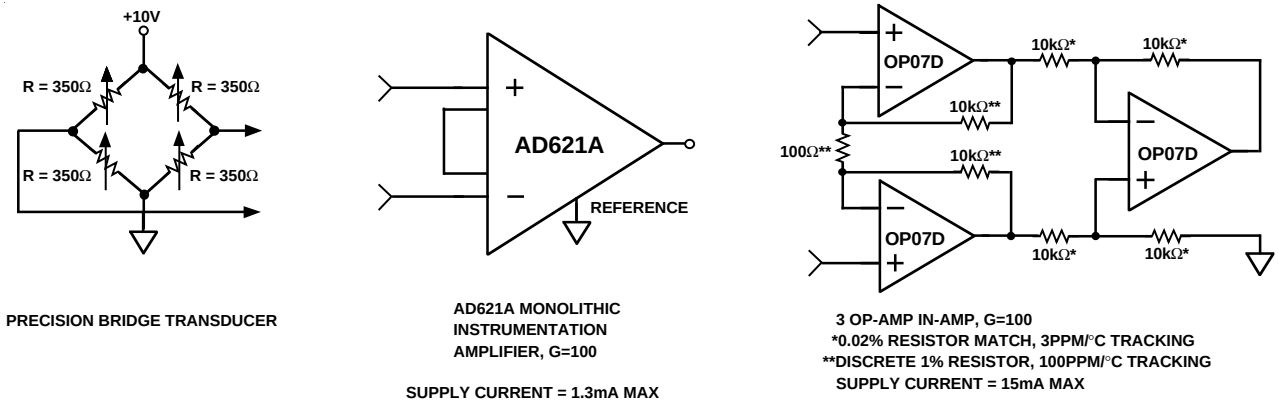


Figure 30. Make vs. Buy

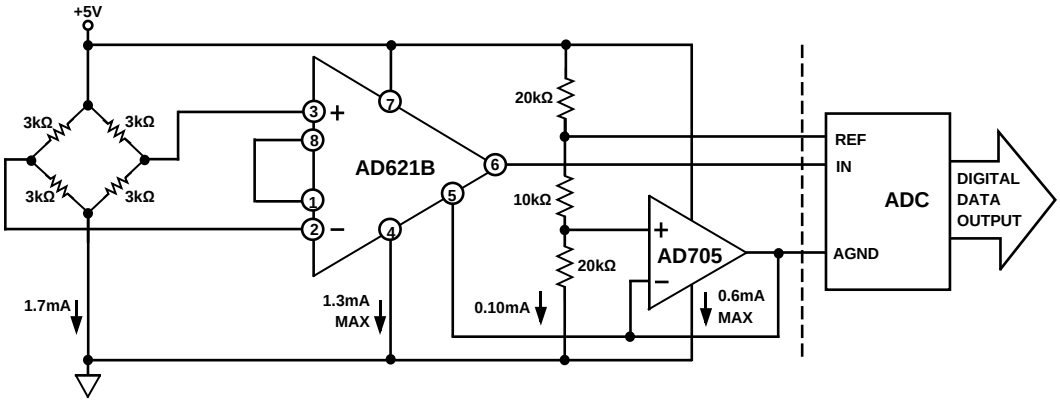


Figure 31. A Pressure Monitor Circuit which Operates on a +5 V Power Supply

Pressure Measurement

Although useful in many bridge applications such as weigh-scales, the AD621 is especially suited for higher resistance pressure sensors powered at lower voltages where small size and low power become more even significant.

Figure 31 shows a 3 kΩ pressure transducer bridge powered from +5 V. In such a circuit, the bridge consumes only 1.7 mA. Adding the AD621 and a buffered voltage divider allows the signal to be conditioned for only 3.8 mA of total supply current.

Small size and low cost make the AD621 especially attractive for voltage output pressure transducers. Since it delivers low noise and drift, it will also serve applications such as diagnostic noninvasion blood pressure measurement.

Wide Dynamic Range Gain Block Suppresses Large Common-Mode and Offset Signals

The AD621 is especially useful in wide dynamic range applications such as those requiring the amplification of signals in the presence of large, unwanted common-mode signals or offsets. Many monolithic in amps achieve low total input drift and noise errors only at relatively high gains (~100). In contrast the AD621's low output errors allow such performance at a gain of 10, thus allowing larger input signals and therefore greater dynamic range. The circuit of Figure 32 (±15 V supply, G = 10) has only 2.5 µV/°C max. V_{OS} drift and 0.55 µV p-p typical 0.1 Hz to 10 Hz noise, yet will amplify a ±0.5 V differential signal while suppressing a ±10 V common-mode signal, or it will amplify a ±1.25 V differential signal while suppressing a 1 V offset by use of the DAC driving the reference pin of the AD621. An added benefit, the offsetting DAC connected to the reference pin allows removal of a dc signal without the associated time-constant of ac coupling. Note the representations of a differential and common-mode signal shown in Figure 32 such that a single-ended (or normal mode) signal of +1 V would be composed of a +0.5 V common-mode component and a +1 V differential component.

Table I. Make vs. Buy Error Budget

Error Source	AD621 Circuit Calculation	Discrete Circuit Calculation	Error, ppm of Full Scale AD621	Discrete
ABSOLUTE ACCURACY at T_A = +25°C				
Input Offset Voltage, µV	125 µV/20 mV	(150 µV × 2/20 mV	6,250	15,000
Output Offset Voltage, µV	N/A	((150 µV × 2)/100)/20 mV	N/A	150
Input Offset Current, nA	2 nA × 350 Ω/20 mV	(6 nA × 350 Ω)/20 mV	18	53
CMR, dB	110 dB→3.16 ppm, × 5 V/20 mV	(0.02% Match × 5 V)/20 mV	791	4,988
		Total Absolute Error	7,558	20,191
DRIFT TO +85°C				
Gain Drift, ppm/°C	5 ppm × 60°C	100 ppm/°C Track × 60°C	300	600
Input Offset Voltage Drift, µV/°C	1 µV/°C × 60°C/20 mV	(2.5 µV/°C × 2 × 60°C)/20 mV	3,000	15,000
Output Offset Voltage Drift, µV/°C	N/A	(2.5 µV/°C × 2 × 60°C)/100/20 mV	N/A	150
		Total Drift Error	3,690	15,750
RESOLUTION				
Gain Nonlinearity, ppm of Full Scale	40 ppm	40 ppm	40	40
Typ 0.1 Hz–10 Hz Voltage Noise, µV p-p	0.28 µV p-p/20 mV	(0.38 µV p-p × $\sqrt{2}$)120 mV	14	27
		Total Resolution Error	54	67
		Grand Total Error	11,472	36,008

G = 100, V_S = ±15 V.
(All errors are min/max and referred to input.)

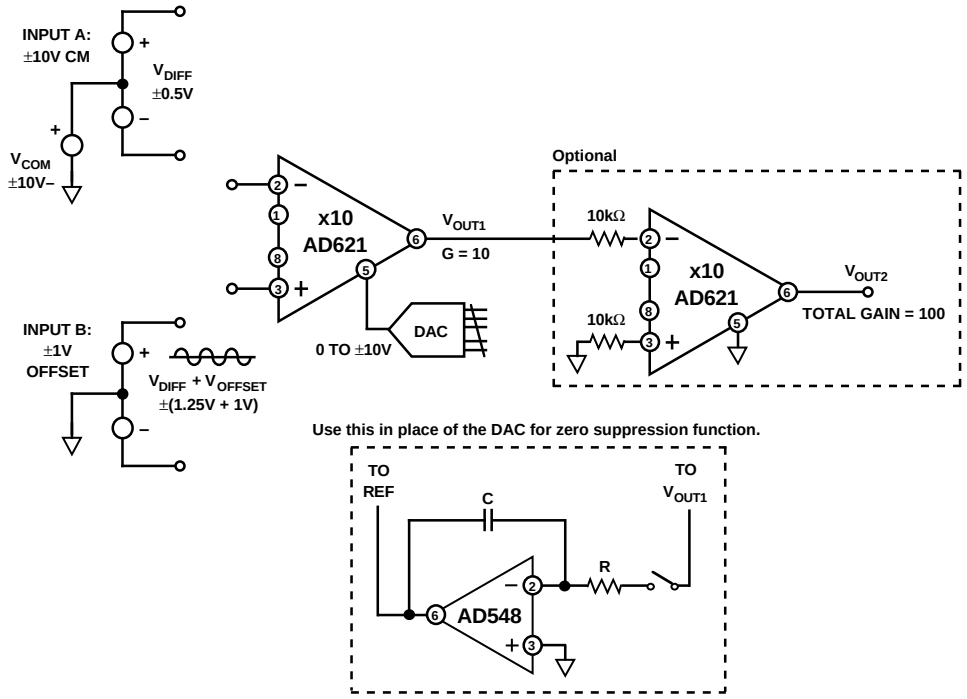


Figure 32. Suppressing a Large Common-Mode or Offset Voltage in Order to Measure a Small Differential Signal (V_S = ±15 V)

The AD621, as well as many other monolithic instrumentation amplifiers, is based on the "three op amp" in amp circuit (Figure 33) amplifier. Since the input amplifiers (A1 and A2) have a common-mode gain of unity and a differential gain equal to the set gain of the overall in amp, the voltages V1 and V2 are defined by the equations

$$V_1 = V_{CM} + G \times V_{DIFF}/2$$
$$V_2 = V_{CM} - G \times V_{DIFF}/2$$

The common-mode voltage will drive the outputs of amplifiers A1 and A2 to the differential-signal voltage, multiplied by the gain, spreads them apart. For a +10 V common-mode +0.1 V differential input, V1 would be at +10.5 V and V2 at +9.5 V.

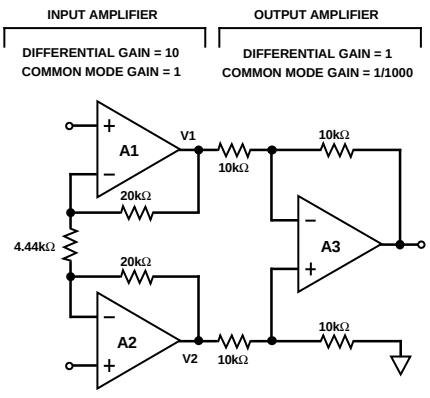


Figure 33. Typical Three Op Amp Instrumentation Amplifier, Differential Gain = 10

The AD621's input amplifiers can provide output voltage within 2.5 V of the supplies. To avoid saturation of the input amplifier the input voltage must therefore obey the equations:

$$V_{CM} + G \times V_{DIFF}/2 \leq (Upper\ \text{Supply} - 2.5\ V)$$
$$V_{CM} - G \times V_{DIFF}/2 \geq (Lower\ \text{Supply} + 2.5\ V)$$

Figure 34 shows the trade-off between common-mode and differential-mode input for ±15 V supplies and G = 10.

By cascading with use of the optional AD621, the circuit of Figure 32 will provide ±1 V of zero suppression at gains of 10 and 100 (at V_{OUT1} and V_{OUT2} respectively) with maximum TCs of ±4 ppm/°C and ±8 ppm/°C, respectively. Therefore, depending on the magnitude of the differential input signal, either V_{OUT1} or V_{OUT2} may be used as the output.

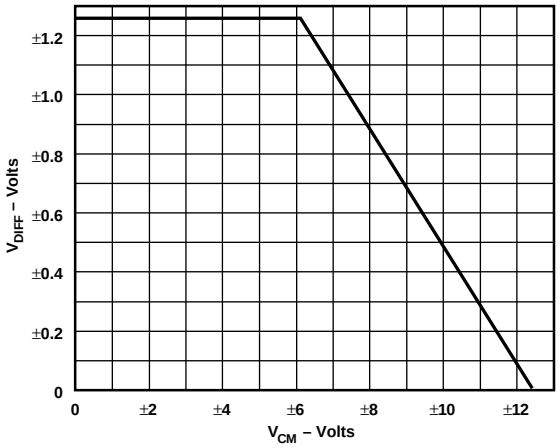


Figure 34. Trade-Off Between V_{CM} and V_{DIFF} Range (V_S = ±15 V, G = 10), for Reference Pin at Ground

Precision V-I Converter

The AD621 along with another op amp and two resistors make a precision current source (Figure 35). The op amp buffers the reference terminal to maintain good CMR. The output voltage V_X of the AD621 appears across R1 which converts it to a current. This current less only the input bias current of the op amp then flows out to the load.

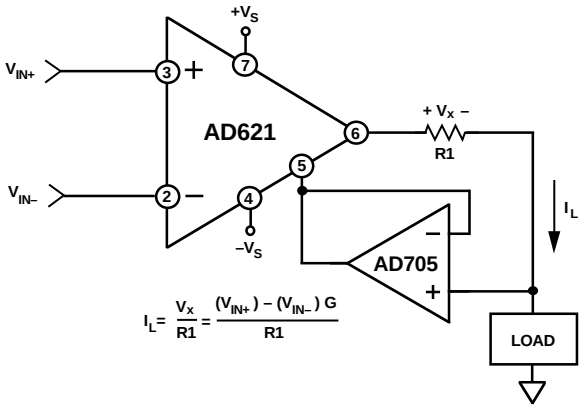


Figure 35. Precision Voltage to Current Converter (Operates on 1.8 mA, ±3 V)

INPUT AND OUTPUT OFFSET VOLTAGE

The AD621 is fully specified for total input errors at gains of 10 and 100. That is, effects of all error sources within the AD621 are properly included in the guaranteed input error specs, eliminating the need for separate error calculation.

Total Error RTI = *Input Error* + (*Output Error*/*G*)

Total Error RTO = (Input Error × G) + *Output Error*

REFERENCE TERMINAL

Although usually grounded, the reference terminal may be used to offset the output of the AD621. This is useful when the load is "floating" or does not share a ground with the rest of the system. It also provides a direct means of injecting a precise offset.

Another benefit of having a reference terminal is that it can be quite effective in eliminating ground loops and noise in a circuit or system.

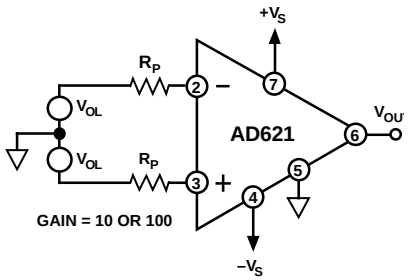


Figure 36. Input Overload Protection

INPUT OVERLOAD CONSIDERATIONS

Failure of a transducer, faults on input lines, or power supply sequencing can subject the inputs of an instrumentation amplifier to voltages well beyond their linear range, or even the supply voltage, so it is essential that the amplifier handle these overloads without being damaged.

The AD621 will safely withstand continuous input overloads of ±3.0 volts (±6.0 mA). This is true for gains of 10 and 100, with power on or off.

The inputs of the AD621 are protected by high current capacity dielectrically isolated 400 Ω thin-film resistors R3 and R4 (Figure 29) and by diodes which protect the input transistors Q1 and Q2 from reverse breakdown. If reverse breakdown occurred, there would be a permanent increase in the amplifier's input current.

The input overload capability of the AD621 can be easily increased while only slightly degrading the noise, common-mode rejection and offset drift of the device by adding external resistors in series with the amplifier's inputs as shown in Figure 36.

Table II summarizes the overload voltages and total input noise for a range of range of r values. Note that a 2 kΩ resistor in series with each input will protect the AD621 from a ±15 volt continuous overload, while only increasing input noise to 13 nV√Hz—about the same level as would be expected from a typical unprotected 3 op amp in amp.

Table II. Input Overload Protection vs. Value of Resistor R_P

Value of Resistor R_P	Total Input Noise in nV√Hz @ 1 kHz		Maximum Continuous Overload Voltage, V_{OL} In Volts
	G = 10	G = 100	
0	14	9	3
499 Ω	14	10	6
1.00 kΩ	14	11	9
2.00 kΩ	15	13	15
3.01 kΩ*	16	14	21
4.99 kΩ*	17	16	33

*1/4 watt, 1% metal-film resistor. All others are 1/8 watt, 1% RN55 or equivalent.

Gain Selection

The AD621 has accurate, low temperature coefficient (TC), gains of 10 and 100 available. The gain of the AD621 is nominally set at 10; this is easily changed to a gain of 100 by simply connecting a jumper between Pins 1 and 8.

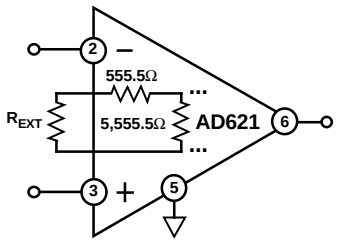


Figure 37. Programming the AD621 for Gains Between 10 and 100

As shown in Figure 37, the device can be programmed for any gain between 10 and 100 by connecting a single external resistor between Pins 1 and 8. Note that adding the external resistor will degrade both the gain accuracy and gain TC. Since the gain equation of the AD621 yields:

$$G = 1 + \frac{9\,(R_X + 6{,}111.111)}{(R_X + 555.555)}$$

This can be solved for the nominal value of external resistor for gains between 10 and 100:

$$R_X = \frac{(G-1)\,555.555 - 55{,}000}{(10 - G)}$$

Table III gives practical 1% resistor values for several common gains.

Table III. Practical 1% External Resistor Values for Gains Between 10 and 100

Desired Gain	Recommended 1% Resistor Value	Gain Error	Temperature Coefficient (TC)
10	∞ (Pins 1 and 8 Open)	*	*5 ppm/°C max
20	4.42 k	≈±10%	≈0.4 (50 ppm/°C + Resistor TC)
50	698 Ω	≈±10%	≈0.4 (50 ppm/°C + Resistor TC)
100	0 (Pins 1 and 8 Shorted)*		*5 ppm/°C max

A High Performance Programmable Gain Amplifier

The excellent performance of the AD621 at a gain of 10 make it a good choice to team up with the AD526 programmable gain amplifier (PGA) to yield a differential input PGA with gains of 10, 20, 40, 80, 160. As shown in Figure 38, the low offset of the AD621 allows total circuit offset to be trimmed using the offset null of the AD526, with only a negligible increase in total drift error. The total gain TC will be 9 ppm/°C max, with 2 μV/°C typical input offset drift. Bandwidth is 600 kHz to gains of 10 to 80, and 350 kHz at G = 160. Settling time is 13 μs to 0.01% for a 10 V output step for all gains.

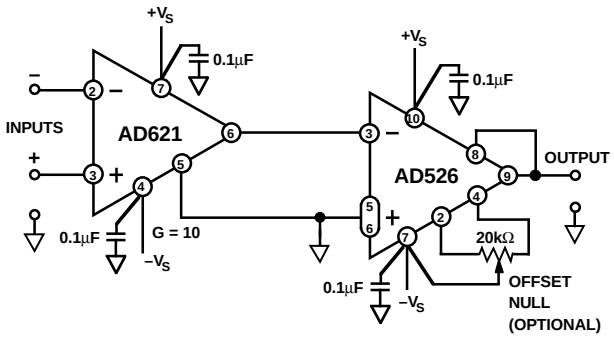


Figure 38. A High Performance Programmable Gain Amplifier

COMMON-MODE REJECTION

Instrumentation amplifiers like the AD621 offer high CMR which is a measure of the change in output voltage when both inputs arc changed by equal amounts. These specifications are usually given for a full-range input voltage change and a specified source imbalance.

For optimal CMR the reference terminal should be tied to a low impedance point, and differences in capacitance and resistance should be kept to a minimum between the two inputs. In many applications shielded cables are used to minimize noise, and for best CMR over frequency the shield should he properly driven. Figures 39 and 40 show active data guards which are configured to improve ac common-mode rejections by "bootstrapping" the capacitances of input cable shields, thus minimizing the capacitance mismatch between the inputs.

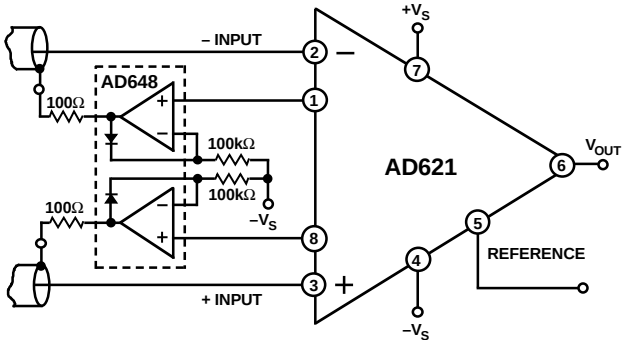


Figure 39. Differential Shield Driver, G = 10

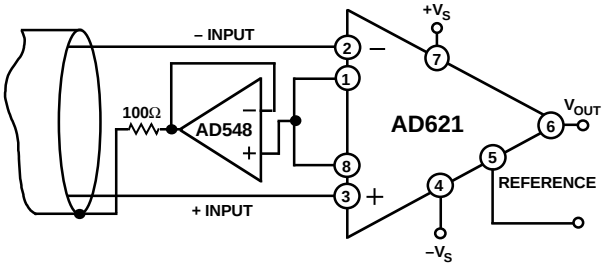


Figure 40. Common-Mode Shield Driver, G = 100

GROUNDING

Since the AD621 output voltage is developed with respect to the potential on the reference terminal, it can solve many grounding problems by simply tying the REF pin to the appropriate "local ground."

In order to isolate low level analog signals from a noisy digital environment, many data-acquisition components have separate analog and digital ground pins (Figure 41). It would be convenient to use a single ground line; however, current through ground wires and PC runs of the circuit card can cause hundreds of millivolts of error. Therefore, separate ground returns should be provided to minimize the current flow from the sensitive points to the system ground. These ground returns must be tied together at some point, usually best at the ADC package as shown.

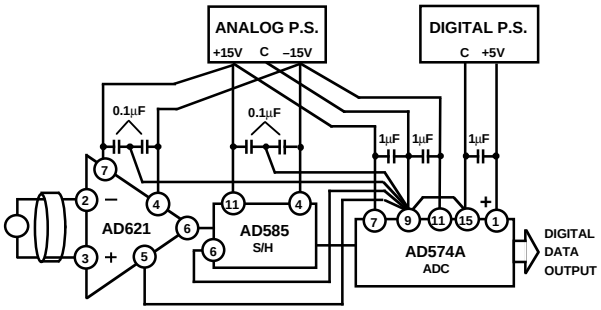


Figure 41. Basic Grounding Practice

GROUND RETURNS FOR INPUT BIAS CURRENTS

Input bias currents are those currents necessary to bias the input transistors of an amplifier. There must be a direct return path for these currents; therefore when amplifying "floating" input sources such as transformers, or ac-coupled sources, there must be a dc path from each input to ground as shown in Figures 42a through 42c. Refer to the *Instrumentation Amplifier Application Guide* (free from Analog Devices) for more information regarding in amp applications.

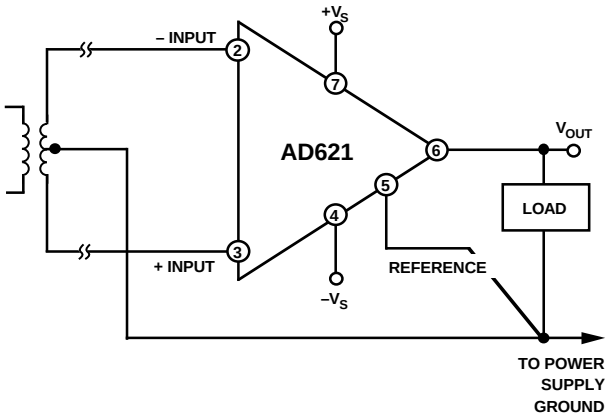


Figure 42a. Ground Returns for Bias Currents when Using Transformer Input Coupling

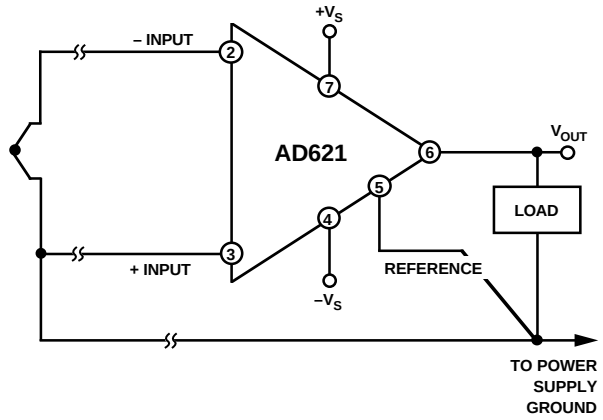


Figure 42b. Ground Returns for Bias Currents when Using a Thermocouple Input

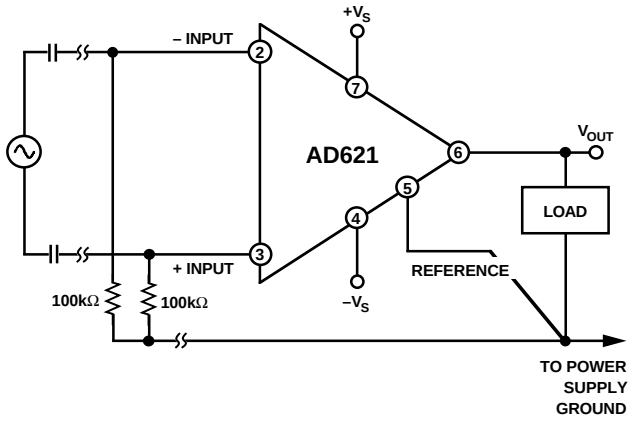
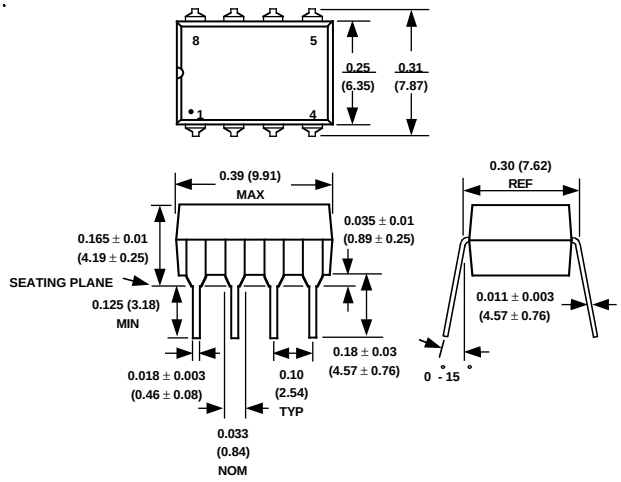


Figure 42c. Ground Returns for Bias Currents when Using AC Input Coupling

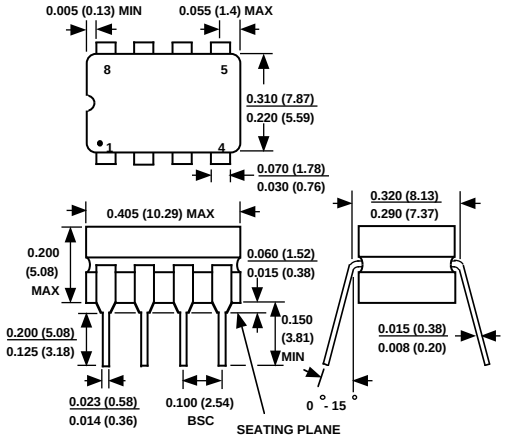
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

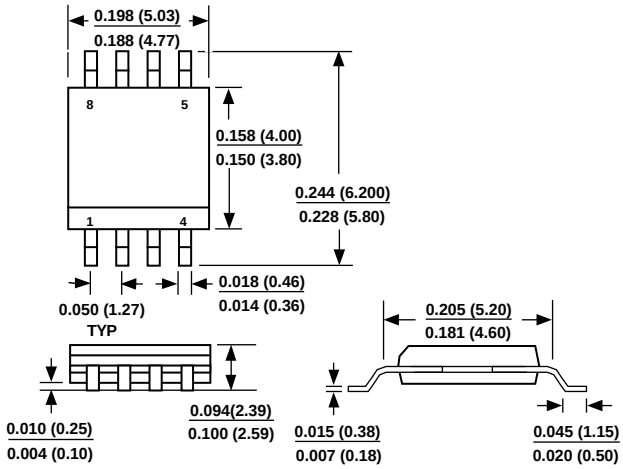
Plastic DIP (N-8) Package



Cerdip (Q-8) Package



SOIC (R-8) Package



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