NEC

MOS INTEGRATED CIRCUIT

μPD75304B,75306B,75308B

4-BIT SINGLE-CHIP MICROCOMPUTER

DESCRIPTION

The μPD75308B is a 75X Series 4-bit single-chip microcomputer capable of the same data processing as an 8-bit microcomputer.

It is a low voltage operation version of the μPD75308 with on-chip LCD controller/driver. Operation at an ultra-low voltage of 2.0 V is possible. An ultra small-sized plastic QFP (12 × 12 mm) is also provided and it is perfect for small-sized set that uses an LCD panel.

Functions, etc., are described in detail in the User's Manual. Please be sure to read this manual when carrying out design work.

μPD75308 User's Manual: IEM-5016

FEATURES

- Ultra-low-voltage operation possible: V_{DD} = 2.0 to 6.0 V
  - Can be driven by two 1.5 V manganese batteries.
- On-chip memory
  - Program memory (ROM) : 8064 × 8 bit (μPD75308B)
    : 6016 × 8 bit (μPD75306B)
    : 4096 × 8 bit (μPD75304B)
  - Data memory (RAM) : 512 × 4 bit
- Instruction execution time adjustment function convenient in high-speed operation and power saving
  - 0.95 μs, 1.91 μs, 15.3 μs (4.19 MHz operation)
  - 122 μs (32.768 kHz operation)
- Built-in programmable LCD controller/driver
  - LCD drive voltage: 2.0 V to V_{DD}
- An ultra small-sized plastic QFP (12 × 12 mm) is provided.
  - Suitable for small-sized set, such as a camera.
- On-chip PROM products available
  - On-chip one-time PROM products : μPD75P308, 75P316A
  - On-chip EPROM products : μPD75P308, 75P316B

APPLICATIONS

Remote control, integrated camera type VCR, camera, gas meter, etc.

Unless there are any particular functional differences, the μPD75308B is described in this document as a representative product.

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Date Published January 1994 P
Printed in Japan

The mark ★ shows major revised points.

ORDERING INFORMATION

Ordering Code	Package	Quality Grade
μPD75304BGC-×××-3B9	80-pin plastic QFP (□14 mm)	Standard
μPD75304BGF-×××-3B9	80-pin plastic QFP (14 × 20 mm)	Standard
μPD75304BGK-×××-BE9	80-pin plastic TQFP(fine pitch)(□12 mm)	Standard
μPD75306BGC-×××-3B9	80-pin plastic QFP (□14 mm)	Standard
μPD75306BGF-×××-3B9	80-pin plastic QFP (14 × 20 mm)	Standard
μPD75306BGK-×××-BE9	80-pin plastic TQFP(fine pitch)(□12 mm))	Standard
μPD75308BGC-×××-3B9	80-pin plastic QFP (□14 mm)	Standard
μPD75308BGF-×××-3B9	80-pin plastic QFP (14 × 20 mm)	Standard
μPD75308BGK-×××-BE9	80-pin plastic TQFP(fine pitch)(□12 mm)	Standard

Remarks ××× is the ROM code number.

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

FUNCTION OUTLINE (1/2)

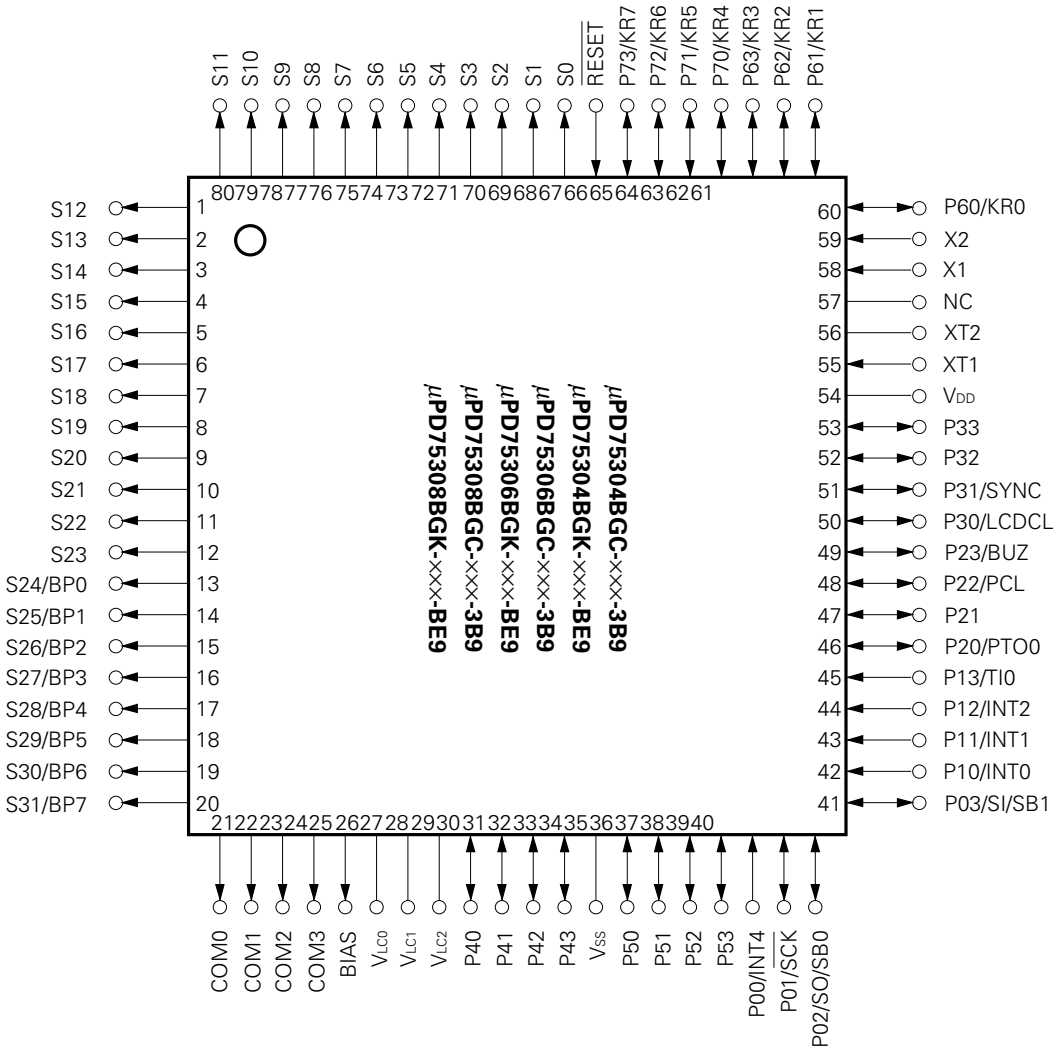
Item		Function			
Number of basic instructions		41			
Instruction cycle		0.95 μs, 1.91 μs, 15.3 μs (main system clock: 4.19 MHz operation) 122 μs (subsystem clock: 32.768 kHz operation)			
On-chip memory	ROM	8064 × 8 bits (μPD75308B), 6016× 8 bits (μPD75306B), 4096× 8 bits (μPD75304B)			
	RAM	512 × 4 bits			
General register		• 4-bit manipulation: 8 (B, C, D, E, H, L, X, A) • 8-bit manipulation: 4 (BC, DE, HL, XA)			
Accumulators		• Bit accumulator (CY) • 4-bit accumulator (A) • 8-bit accumulator (XA)			
Instruction set		• Various bit manipulation instructions • Efficient 4-bit data manipulation instructions • 8-bit data transfer instructions • GETI instruction that can implement arbitrary 2-byte/3-byte instructions with 1 byte			
I/O lines		40	8	CMOS input	Pull-up by software possible : 23
			16	CMOS input/output	
			8	CMOS output	Used with segment pin
			8	N-ch open-drain input/output	10 V withstand voltage, pull-up by mask option possible : 8
LCD controller/driver		• Number of segments selection: 24/28/32 segments (4/8 can be switched at bit port output.) • Display mode selection: Static, 1/2 duty, 1/3 duty (1/2 bias), 1/3 duty (1/3 bias), 1/4 duty • LCD drive division resistor can be incorporated by mask option			
Supply voltage range		V_{DD} = 2.0 to 6.0 V			
Timer		3 channels	• 8-bit timer/event counter • Clock source: 4 stages • Event count possible		
			• 8-bit basic interval timer • Standard clock generation: 1.95 ms, 7.82 ms, 31.3 ms, 250 ms (4.19 MHz operation) • Watchdog timer application possible		

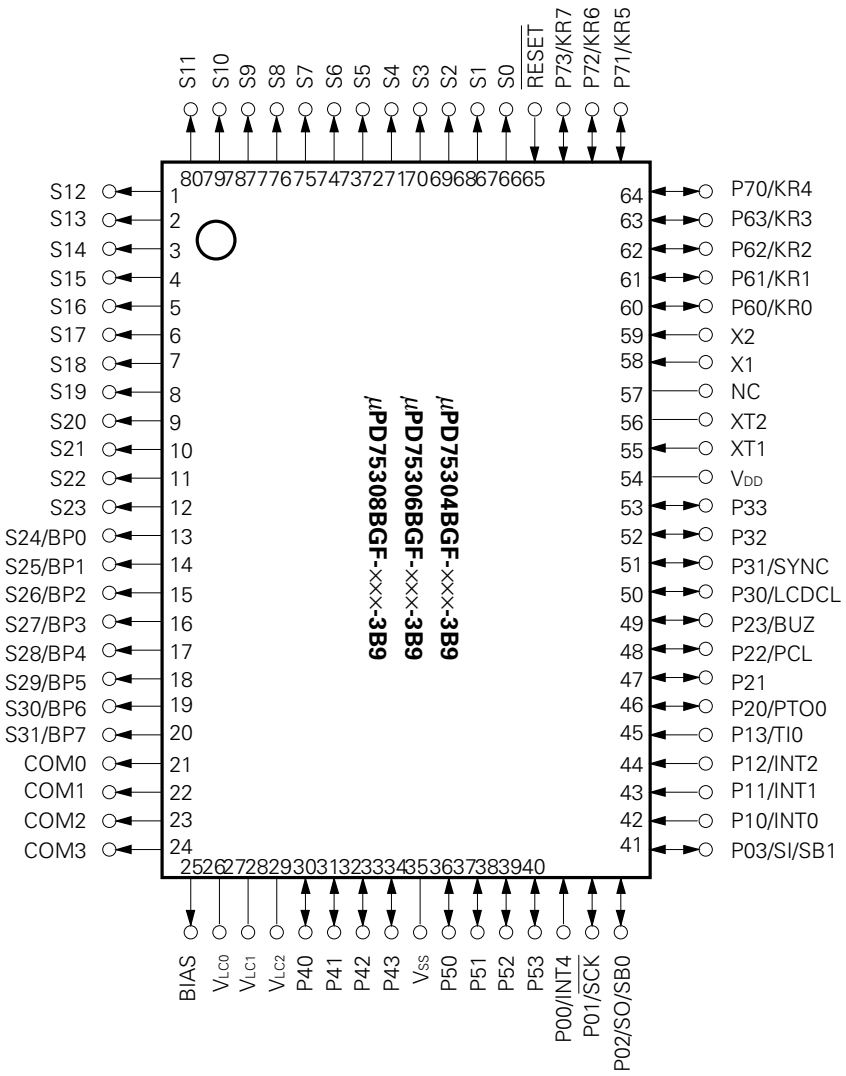
FUNCTION OUTLINE (2/2)

Item	Function	
Timer	3 channels	• Watch timer • 0.5 seconds time interval generation • Count clock source: Main system clock and subsystem clock switchable • Fast watch mode (3.9 ms time interval generation) • Buzzer output possible (2 kHz)
8-bit serial interface	• Three modes application possible • 3-wire serial I/O mode • 2-wire serial I/O mode • SBI mode	
	• LSB top/MSB top switchable	
Bit sequential buffer	Special bit manipulation memory: 16 bits • Perfect for remote control application	
Clock output function	Timer/event counter output (PTO0): Arbitrary frequency square wave output	
	Clock output (PCL): Φ, 524, 262, 65.5 kHz (4.19 MHz operation)	
	Buzzer output (BUZ): 2 kHz (4.19 MHz or 32.768 kHz operation)	
Vectored interrupt	• External: 3 • Internal: 3	
Test input	• External: 1 • Internal: 1	
System clock oscillator	• Main system clock oscillation ceramic/crystal oscillation circuit: 4.194304 MHz • Subsystem clock oscillation crystal oscillation circuit: 32.768 kHz	
Standby	STOP/HALT mode	
Package	• 80-pin plastic QFP (14 × 20 mm) • 80-pin plastic QFP (□14 mm) • 80-pin plastic TQFP (fine pitch) (□12 mm)	

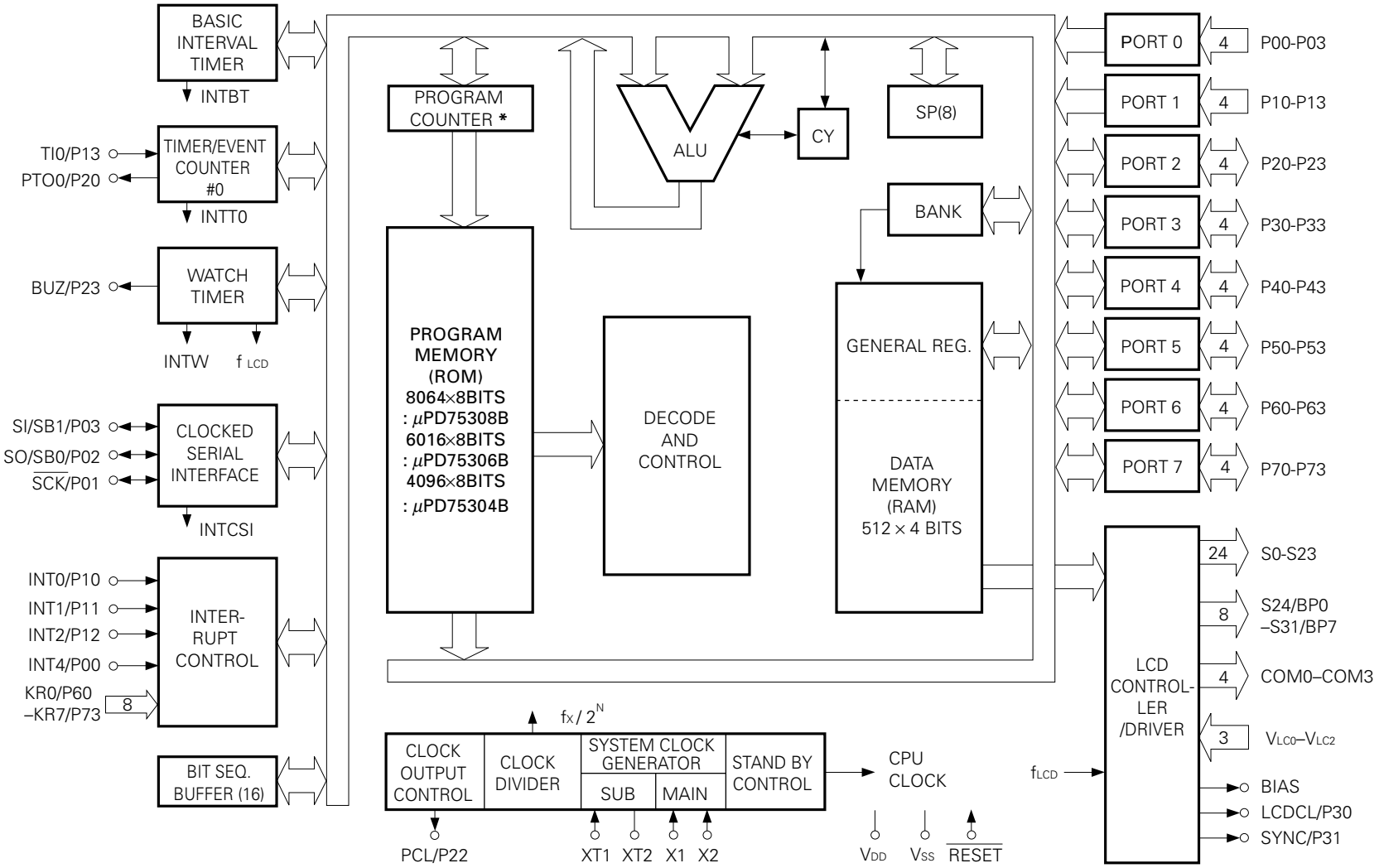
CONTENTS

1. PIN CONFIGURATION (TOP VIEW)





P00 to 03	: Port 0	S0 to 31	: Segment Output 0 to 31
P10 to 13	: Port 1	COM0 to 3	: Common Output 0 to 3
P20 to 23	: Port 2	V_{LC0-2}	: LCD Power Supply 0 to 2
P30 to 33	: Port 3	BIAS	: LCD Power Supply Bias Control
P40 to 43	: Port 4	LCDCL	: LCD Clock
P50 to 53	: Port 5	SYNC	: LCD Synchronization
P60 to 63	: Port 6	TI0	: Timer Input 0
P70 to 73	: Port 7	PTO0	: Programmable Timer Output 0
BP0 to 7	: Bit Port	BUZ	: Buzzer Clock
KR0 to 7	: Key Return	PCL	: Programmable Clock
$\overline{SCK}$	: Serial Clock	INT0, 1, 4	: External Vectored Interrupt 0, 1, 4
SI	: Serial Input	INT2	: External Test Input 2
SO	: Serial Output	X1, 2	: Main System Clock Oscillation 1, 2
SB0,1	: Serial Bus 0, 1	XT1, 2	: Subsystem Clock Oscillation 1, 2
$\overline{RESET}$	: Reset Input	NC	: No Connection



* 13bits : μPD75306B, 75308B
12bits : μPD75304B

3. PIN FUNCTIONS

3.1 PORT PINS (1/2)

Pin Name	Input/Output	Dual-Function Pin	Function	8-bit I/O	After Reset	I/O Circuit Type *1
P00	Input	INT4	4-bit input port (PORT 0) On-chip pull-up resistor can be specified for P01 to P03 as a 3-bit unit by software.	×	Input	Ⓑ
P01	Input/output	$\overline{SCK}$				Ⓕ - A
P02	Input/output	SO/SB0				Ⓕ - B
P03	Input/output	SI/SB1				Ⓜ - C
P10	Input	INT0	With noise elimination function 4-bit input port (PORT 1) On-chip pull-up resistor can be specified as a 4-bit unit by software.	×	Input	Ⓑ - C
P11		INT1				
P12		INT2				
P13		TI0				
P20	Input/output	PTO0	4-bit input/output port (PORT 2) On-chip pull-up resistor can be specified as a 4-bit unit by software.	×	Input	E - B
P21		—				
P22		PCL				
P23		BUZ				
P30 *2	Input/output	LCDCL	Programmable 4-bit input/output port (PORT 3) Input/output can be specified bit-wise. On-chip pull-up resistor can be specified as a 4-bit unit by software.	×	Input	E - B
P31 *2		SYNC				
P32 *2		—				
P33 *2		—				
P40 to P43 *2	Input/output	—	N-ch open-drain 4-bit input/output port (PORT 4) On-chip pull-up resistor can be specified bit-wise (mask option). Open-drain: 10 V withstand voltage	○	High level (on-chip pull-up resistor) or high-impedance	M
P50 to P53 *2	Input/output	—	N-ch open-drain 4-bit input/output port (PORT 5) On-chip pull-up resistor can be specified bit-wise (mask option). Open-drain: 10 V withstand voltage		High level (on-chip pull-up resistor) or high-impedance	M

* **1.** ◯ : Schmitt trigger input

2. LED direct drive possible

3.1 PORT PINS (2/2)

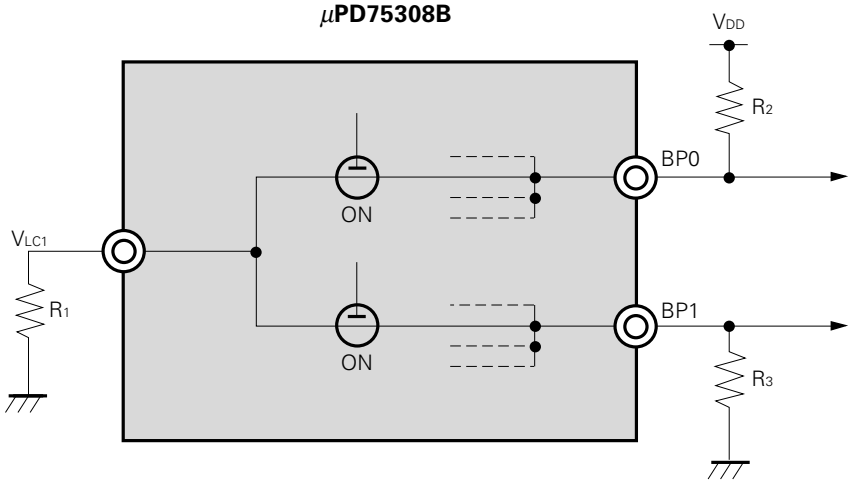
Pin Name	Input/Output	Dual-Function Pin	Function	8-bit I/O	After Reset	I/O Circuit Type *1
P60	Input/output	KR0	Programmable 4-bit input/output port (PORT 6) Input/output can be specified bit-wise. On-chip pull-up resistor can be specified as a 4-bit unit by software.	○	Input	Ⓕ - A
P61		KR1				
P62		KR2				
P63		KR3				
P70	Input/output	KR4	4-bit input/output port (PORT 7) On-chip pull-up resistor can be specified as a 4-bit unit by software.		Input	Ⓕ - A
P71		KR5				
P72		KR6				
P73		KR7				
BP0	Output	S24	1-bit output port (BIT PORT) Also used as segment output pin.	×	* 2	G - C
BP1		S25				
BP2		S26				
BP3		S27				
BP4	Output	S28				
BP5		S29				
BP6		S30				
BP7		S31				

* **1.** ◯ : Schmitt trigger input

2. BP0 to BP7 select V_{LC1} as the input source.
However, the output level depends on BP0 to BP7 and V_{LC1} external circuit.

Example BP0 to BP7 are connected mutually within the μPD75308B. Therefore, the output level of BP0 to BP7 is determined by the value of R_1, R_2 and R_3.

μPD75308B



3.2 NON-PORT PINS

Pin Name	Input/Output	Dual-Function Pin	Function		After Reset	I/O Circuit Type *1
TI0	Input	P13	External event pulse input pin to timer/event counter		Input	Ⓑ - C
PTO0	Input/output	P20	Timer/event counter output pin		Input	E - B
PCL	Input/output	P22	Clock output pin		Input	E - B
BUZ	Input/output	P23	Fixed frequency output pin (for buzzer or system clock trimming)		Input	E - B
$\overline{SCK}$	Input/output	P01	Serial clock input/output pin		Input	Ⓕ - A
SO/SB0	Input/output	P02	Serial data output pin Serial bus input/output pin		Input	Ⓕ - B
SI/SB1	Input/output	P03	Serial data input pin Serial bus input/output pin		Input	Ⓜ - C
INT4	Input	P00	Edge detection vectored interrupt input pin (both rising edge and falling edge detection effective)		Input	Ⓑ
INT0	Input	P10	Edge detection vectored interrupt input pin (detection edge selectable)	Clock synchronous system	Input	Ⓑ - C
INT1		P11		Asynchronous		
INT2	Input	P12	Edge detection testable input pin (rising edge detection)	Asynchronous	Input	Ⓑ - C
KR0 to KR3	Input/output	P60 to P63	Parallel falling edge detection testable input pin		Input	Ⓕ - A
KR4 to KR7	Input/output	P70 to P73	Parallel falling edge detection testable input pin		Input	Ⓕ - A
S0 to S23	Output	—	Segment signal output pin		*2	G - A
S24 to S31	Output	BP0 to BP7	Segment signal output pin		*2	G - C
COM0 to COM3	Output	—	Common signal output pin		*2	G - B
V_{LC0} to V_{LC2}	—	—	LCD drive power supply pin On-chip split resistor (mask option)		—	—
BIAS	Output	—	External split resistor cut output pin		*3	—
LCDCL *4	Input/output	P30	External expansion driver drive clock output pin		Input	E - B
SYNC *4	Input/output	P31	External expansion driver synchronization clock output pin		Input	E - B
X1, X2	Input	—	Main system clock oscillation crystal/ceramic connection pin. For external clock, the external clock signal is input to X1 and its opposite phase is input to X2.		—	—
XT1	Input	—	Subsystem clock oscillation crystal connection pin. For external clock, the external clock signal is input to XT1 and XT2 is opened. XT1 can be used as a 1-bit input (test) pin.		—	—
XT2	—	—				
$\overline{RESET}$	Input	—	System reset input pin		—	Ⓑ
NC *5	—	—	NO CONNECTION		—	—
V_{DD}	—	—	Positive power supply pin		—	—
V_{SS}	—	—	GND potential pin		—	—

* **1.** ◯ : Schmitt trigger input

2. Display outputs are selected with V_{LCX} shown below as the input source.

S0 to S31: V_{LC1}, COM0 to COM2: V_{LC2}, COM3: V_{LC0}

However, the level of each display output depends on the display output and V_{LCX} external circuit.

* **3.** On-chip split resistor ..... Low level
No on-chip split resistor ... High-impedance

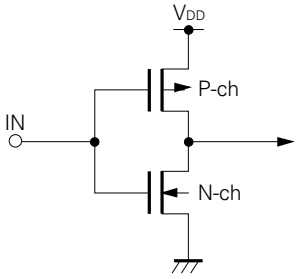
4. Pins provided for system expansion. Currently, only used as P30 and P31.

5. If a printed wiring board is shared with the μPD75P316A/75P316B, the NC pin should be connected to V_{DD}.

3.3 PIN INPUT/OUTPUT CIRCUITS

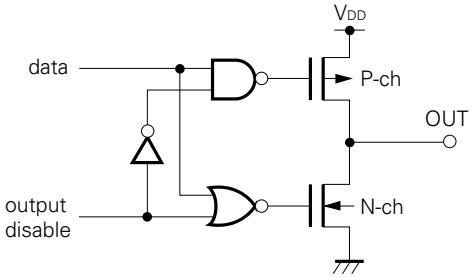
The input/output circuits of each pin of the μPD75308B are shown by in abbreviated form.

TYPE A (For TYPE E-B)



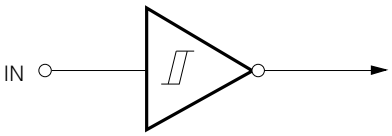
CMOS Standard Input Buffer

TYPE D (For TYPE E-B, F-A)



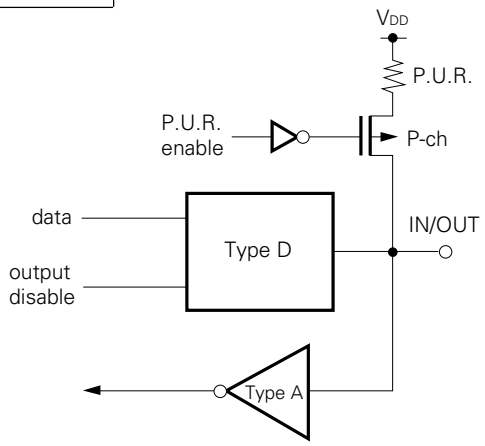
Push-pull output that can be made high-impedance output (P-ch and N-ch OFF)

TYPE B



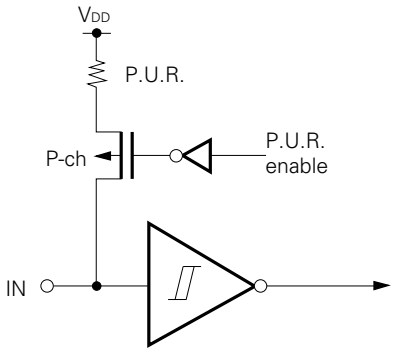
Schmitt-Trigger Input with Hysteresis Characteristic

TYPE E-B



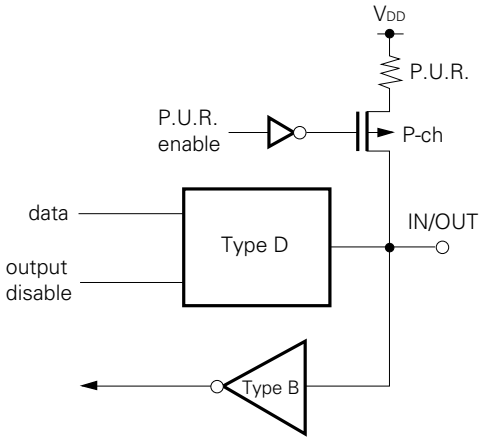
P.U.R.:Pull-Up Resistor

TYPE B-C



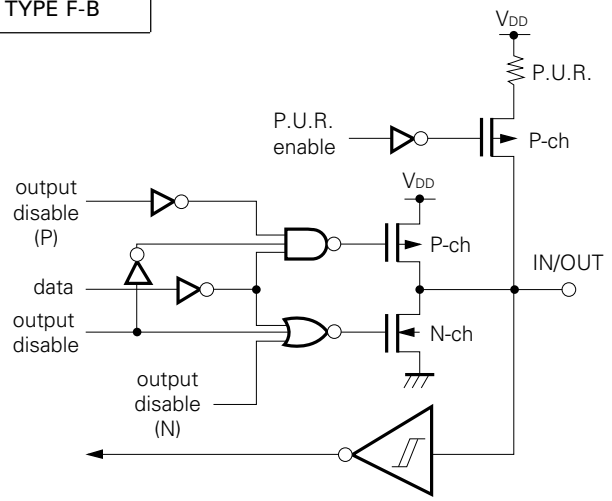
P.U.R. : Pull-Up Resistor

TYPE F-A



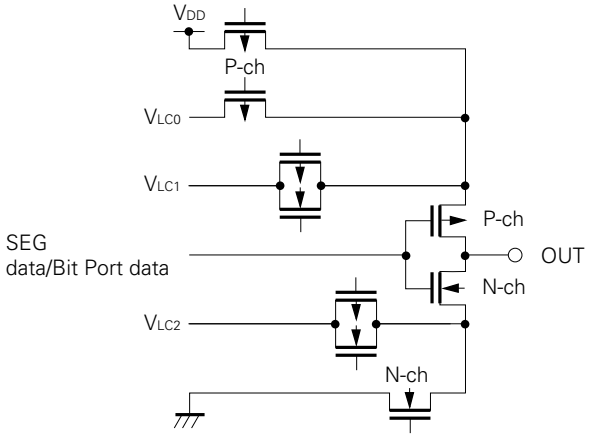
P.U.R.:Pull-Up Resistor

TYPE F-B

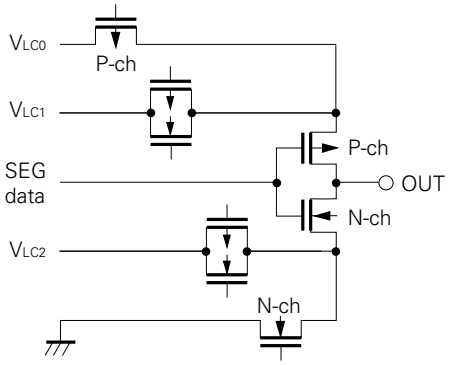


P.U.R.:Pull-Up Resistor

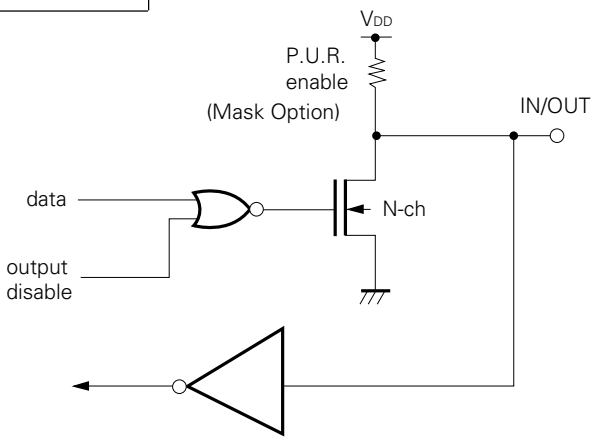
TYPE G-C



TYPE G-A



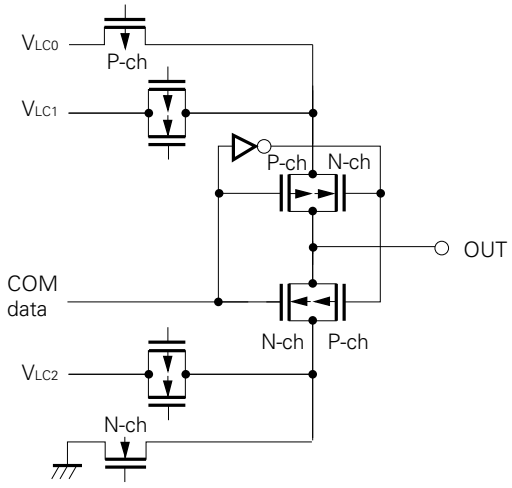
TYPE M



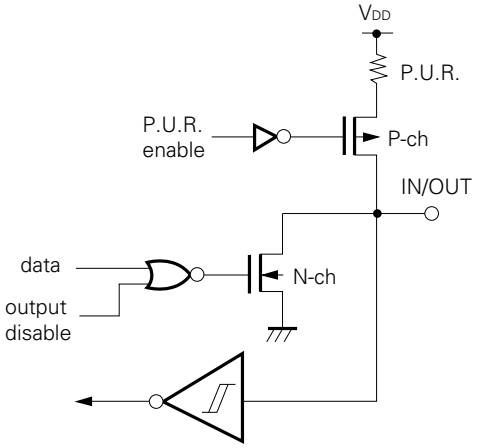
Middle-High Voltage Input Buffer
(+10 V Withstand Voltage)

P.U.R.:Pull-Up Resistor

TYPE G-B



TYPE M-C



P.U.R.:Pull-Up Resistor

3.4 RECPMMENDED CONNECTION OF UNUSED PINS ★

Table 3-1 Connection of Unused Pins

Pin	Recommended Connection
P00/INT4	Connect to V_{SS}
P01/$\overline{SCK}$	Connect to V_{SS} or V_{DD}
P02/SO/SB0	
P03/SI/SB1	
P10/INT0-P12/INT2	Connect to V_{SS}
P13/TI0	
P20/PTO0	Input state : Connect to V_{SS} or V_{DD} Outputstate : Leave open
P21	
P22/PCL	
P23/BUZ	
P30/LCDCL	
P31/SYNC	
P32	
P33	
P40 to P43	
P50 to P53	
P60/KR0 to P63/KR3	
P70/KR4 to P73/KR7	
S0 to S23	Leave open
S24/BP0 to S31/BP7	
COM0 to COM3	
V_{LC0} to V_{LC2}	Connect to V_{SS}
BIAS	Connect to V_{SS} only when V_{LC0} to V_{LC2} are all unused; otherwise leave open
XT1	Connect to V_{SS} or V_{DD}
XT2	Leave open

★ **3.5 PRECAUTIONS CONCERNING P00/INT4 PIN AND $\overline{\text{RESET}}$ PIN**

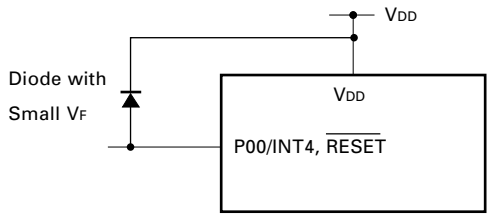
In addition to the functions shown in 3.1 and 3.2, the P00/INT4 pin and $\overline{\text{RESET}}$ pin are also used to set the test mode for testing internal μPD75308B operation (for IC testing).

The test mode is set when a voltage greater than V_{DD} is applied to either of these pins. Consequently, if noise exceeding V_{DD} is applied during normal operation, the test mode may be entered, making it impossible for normal operation to continue.

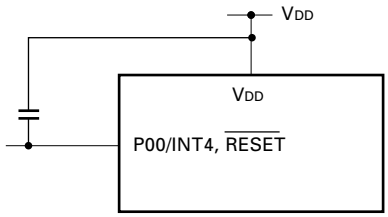
For example, misoperation may result if inter-wiring noise is applied to the P00/INT4 or $\overline{\text{RESET}}$ pin due to the length of the wiring from these pins, and the pin voltage exceeds V_{DD}.

Wiring should therefore be carried out so that inter-wiring noise is suppressed as far as possible. If it is completely impossible to suppress noise, noise prevention measures should be taken using an external component as shown below.

o **Diode connected between P00/INT4 or $\overline{\text{RESET}}$ and V_{DD}**



o **Capacitor connected between P00/INT4 or $\overline{\text{RESET}}$ and V_{DD}**



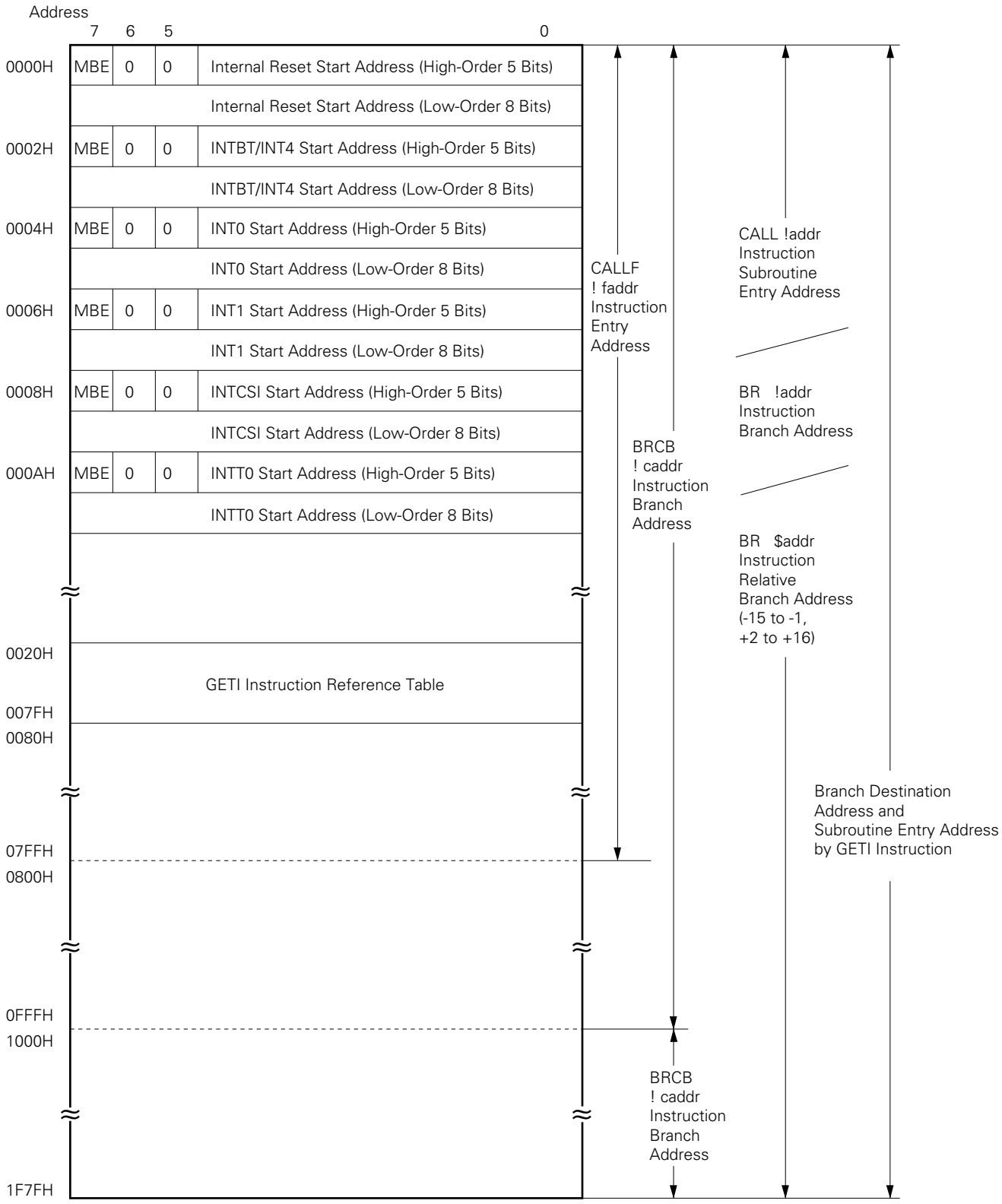
4. MEMORY CONFIGURATION

- Program memory (ROM) ... 8064 × 8 bits (0000H to 1F7FH): μPD75308B
  6016 × 8 bits (0000H to 177FH): μPD75306B
  4096 × 8 bits (0000H to 0FFFH): μPD75304B
  - 0000H to 0001H: Vector table in which the program start address after a reset is written.
  - 0002H to 000BH: Vector table in which program start addresses in case of interrupts are written.
  - 0020H to 007FH: Table area referenced by the GETI instruction.

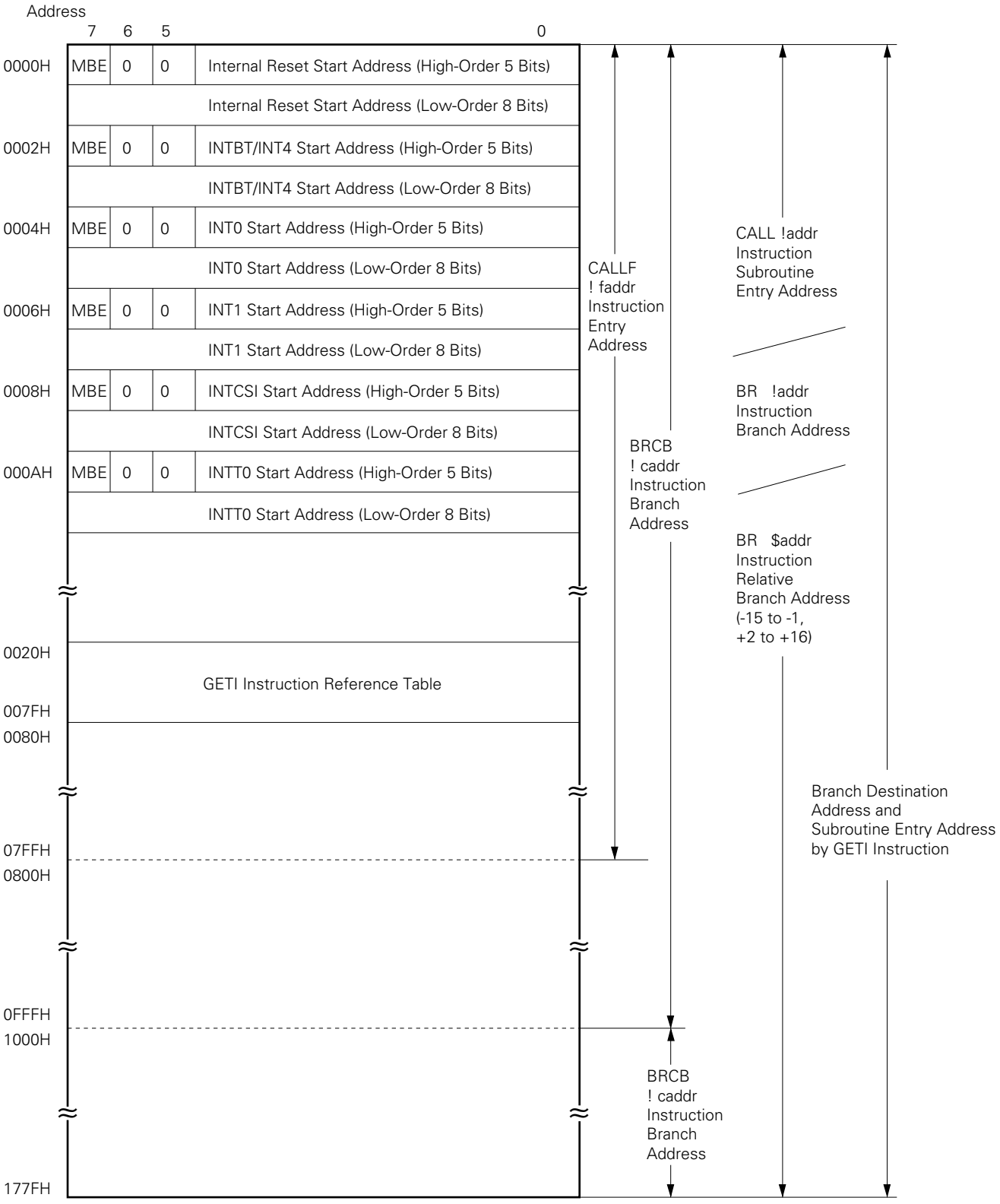
- Data memory
  - Data area ... 512 × 4 bits (000H to 1FFH)
  - Peripheral hardware area ... 128 × 4 bits (F80H to FFFH)

Fig. 4-1 Program Memory Map

(a) μPD75308B



(b) μPD75306B


Address
7 6 5 0
0000H MBE 0 0 Internal Reset Start Address (High-Order 5 Bits)
Internal Reset Start Address (Low-Order 8 Bits)
0002H MBE 0 0 INTBT/INT4 Start Address (High-Order 5 Bits)
INTBT/INT4 Start Address (Low-Order 8 Bits)
0004H MBE 0 0 INT0 Start Address (High-Order 5 Bits)
INT0 Start Address (Low-Order 8 Bits)
0006H MBE 0 0 INT1 Start Address (High-Order 5 Bits)
INT1 Start Address (Low-Order 8 Bits)
0008H MBE 0 0 INTCSI Start Address (High-Order 5 Bits)
INTCSI Start Address (Low-Order 8 Bits)
000AH MBE 0 0 INTT0 Start Address (High-Order 5 Bits)
INTT0 Start Address (Low-Order 8 Bits)
0020H
GETI Instruction Reference Table
007FH
0080H
07FFH
0800H
0FFFH
1000H
177FH
CALLF ! faddr Instruction Entry Address
BRCB ! caddr Instruction Branch Address
CALL !addr Instruction Subroutine Entry Address
BR !addr Instruction Branch Address
BR $addr Instruction Relative Branch Address (-15 to -1, +2 to +16)
BRCB ! caddr Instruction Branch Address
Branch Destination Address and Subroutine Entry Address by GETI Instruction

(c) μPD75304B

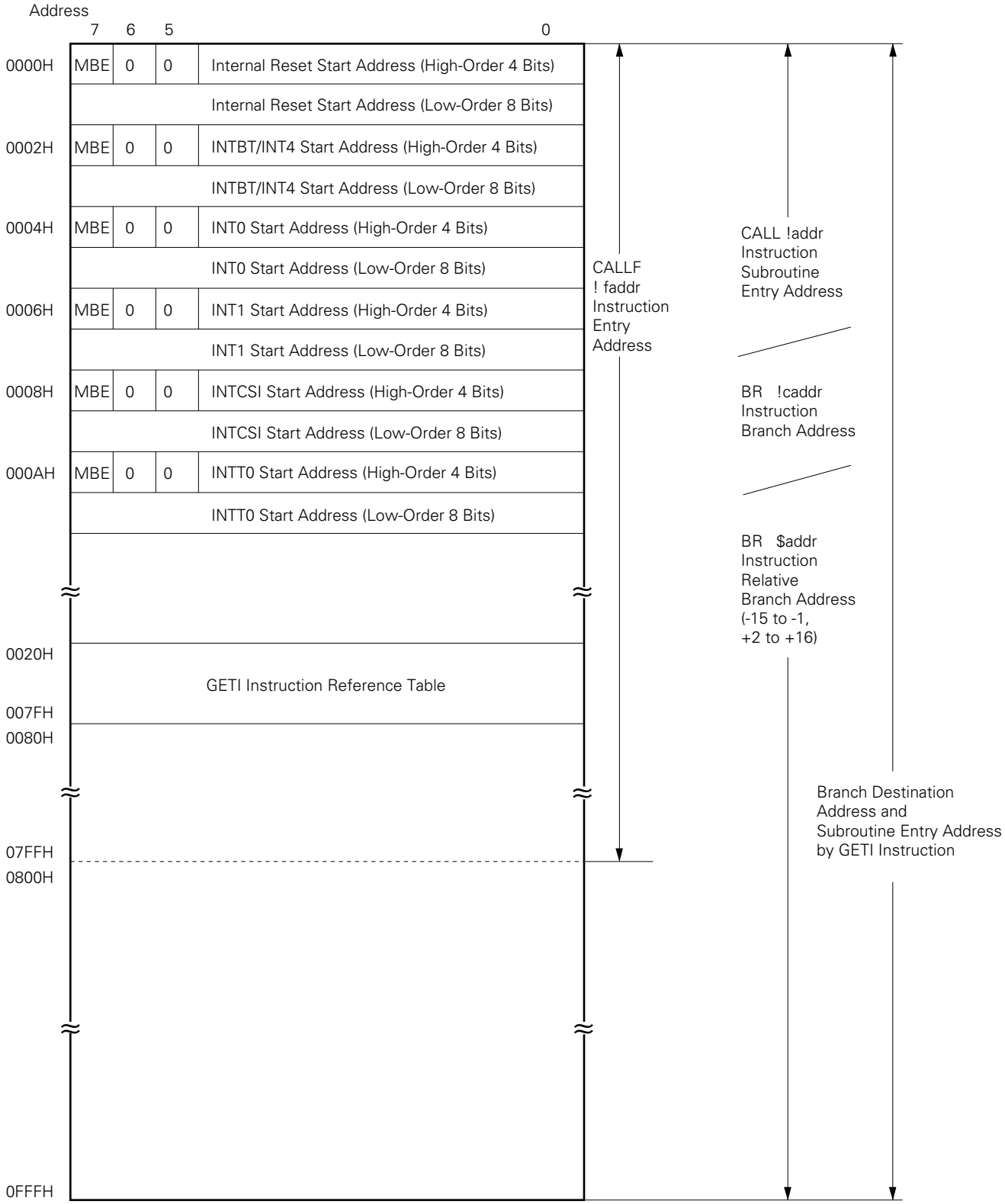
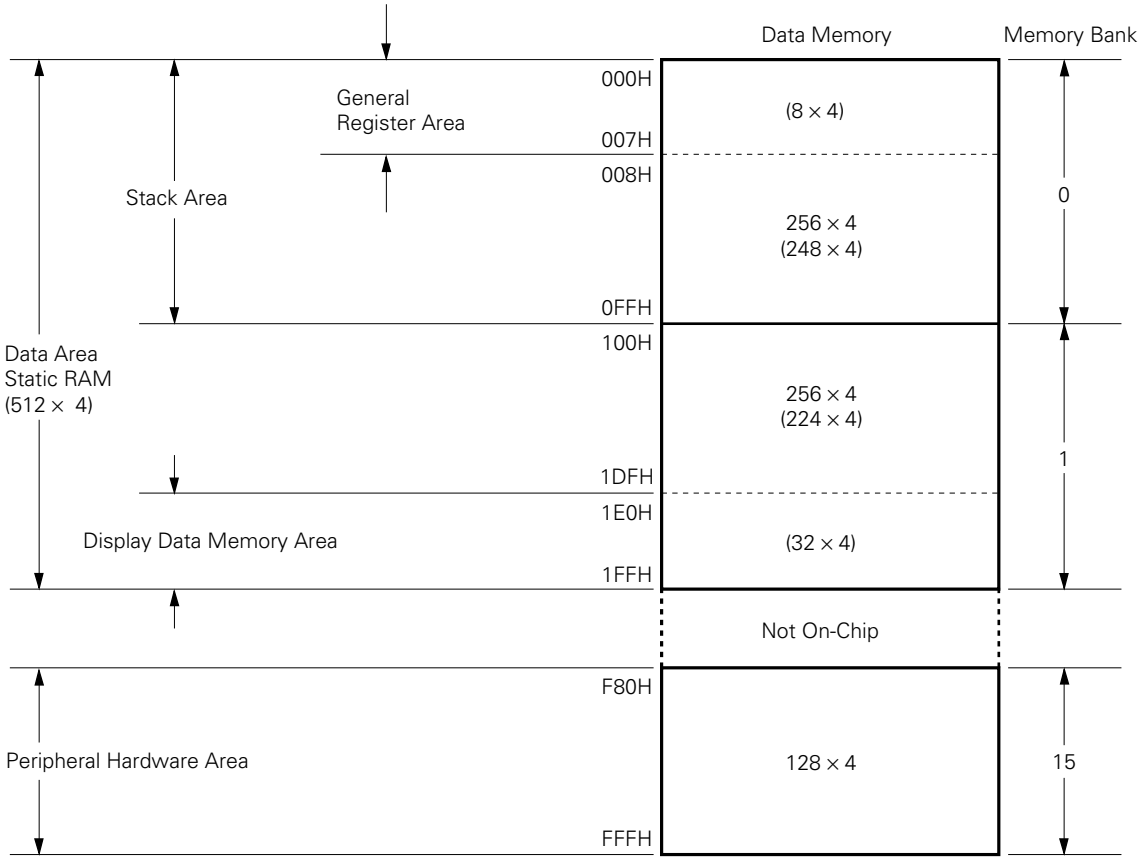

Address
7 6 5 0
0000H MBE 0 0 Internal Reset Start Address (High-Order 4 Bits)
Internal Reset Start Address (Low-Order 8 Bits)
0002H MBE 0 0 INTBT/INT4 Start Address (High-Order 4 Bits)
INTBT/INT4 Start Address (Low-Order 8 Bits)
0004H MBE 0 0 INT0 Start Address (High-Order 4 Bits)
INT0 Start Address (Low-Order 8 Bits)
0006H MBE 0 0 INT1 Start Address (High-Order 4 Bits)
INT1 Start Address (Low-Order 8 Bits)
0008H MBE 0 0 INTCSI Start Address (High-Order 4 Bits)
INTCSI Start Address (Low-Order 8 Bits)
000AH MBE 0 0 INTT0 Start Address (High-Order 4 Bits)
INTT0 Start Address (Low-Order 8 Bits)
0020H
GETI Instruction Reference Table
007FH
0080H
07FFH
0800H
0FFFH
CALLF ! faddr Instruction Entry Address
CALL !addr Instruction Subroutine Entry Address
BR !caddr Instruction Branch Address
BR $addr Instruction Relative Branch Address (-15 to -1, +2 to +16)
Branch Destination Address and Subroutine Entry Address by GETI Instruction

Fig. 4-2 Data Memory Map



5. PERIPHERAL HARDWARE FUNCTIONS

5.1 PORTS

There are four kinds of I/O ports, as follows.

- CMOS input (PORT0, 1) : 8
- CMOS input/output (PORT2, 3, 6, 7) : 16
- N-ch open drain (PORT4, 5) : 8
- CMOS output (BP0 to BP7) : 8

Total 40

Fig. 5-1 Port Functions

Port (Symbol)	Function	Operation/Features	Remarks
PORT 0	4-bit input	Always readable or testable irrespective of dual-function pin operating mode.	Dual function as INT4, $\overline{SCK}$, SO/SB0 & SI/SB1 pins
PORT 1			Dual function as pins INT0 to INT2 & TI0
PORT 2	4-bit input/output	Can be set to input or output mode as 4-bit unit. Ports 6 & 7 can be paired for 8-bit data input/output.	Dual function as PTO0, PCL & BUZ pins
PORT 7			Dual function as pins KR4 to KR7
PORT 3 *		Can be set to input or output mode bit-wise.	Dual function as LCDCL & SYNC pins
PORT 6			Dual function as pins KR0 to KR3
PORT 4 * PORT 5 *	4-bit input/output (N-ch open-drain 10 V withstand voltage)	Can be set to input or output mode as 4-bit unit. Ports 4 & 5 can be paired for 8-bit data input/output.	Incorporation of pull-up resistor can be specified bit-wise by mask option.
BP0 to BP7	1-bit output	Outputs data bit-wise. Switchable by software with LCD drive segment outputs S24 to S31.	Small drive capability. For CMOS load drive.

* Direct LED drive capability

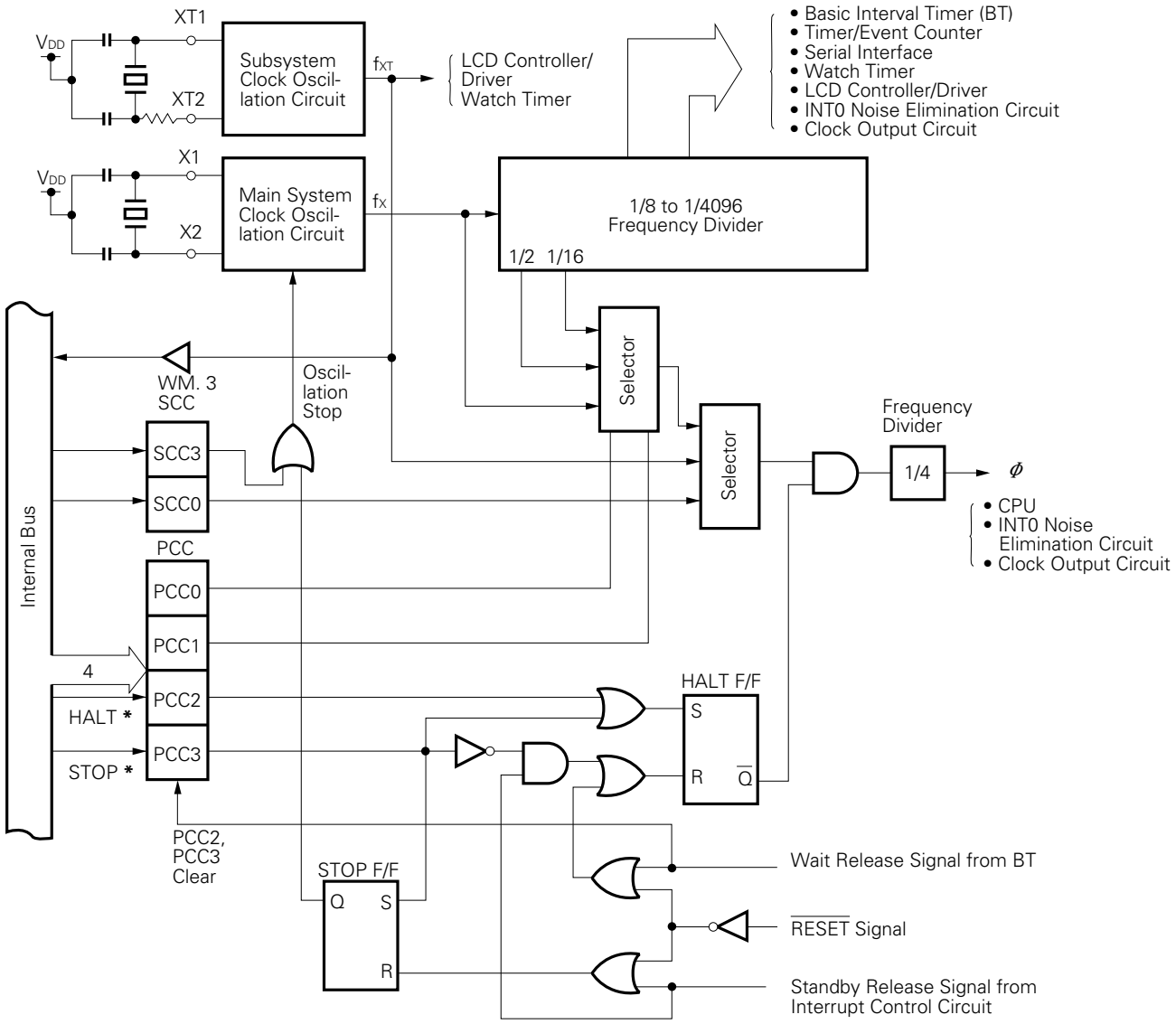
5.2 CLOCK GENERATOR

The operation of the clock generator is determined by the processor clock control register (PCC) and system clock control register (SCC).

There are two kinds of clock, the main system clock and subsystem clock, and the instruction execution time can be changed.

- 0.95 μs/1.91 μs/15.3 μs (4.19 MHz main system clock operation)
- 122 μs (32.768 kHz subsystem clock operation)

Fig. 5-1 Clock Generator Block Diagram



Remarks
1. fX = Main system clock frequency
2. fXT = Subsystem clock frequency
3. PCC: Processor clock control register
4. SCC: System clock control register
5. * indicates instruction execution.
6. ★ One Φ clock cycle (tCY) is one machine cycle. See "AC CHARACTERISTICS" in **11. "ELECTRICAL SPECIFICATIONS"** for details of tCY.

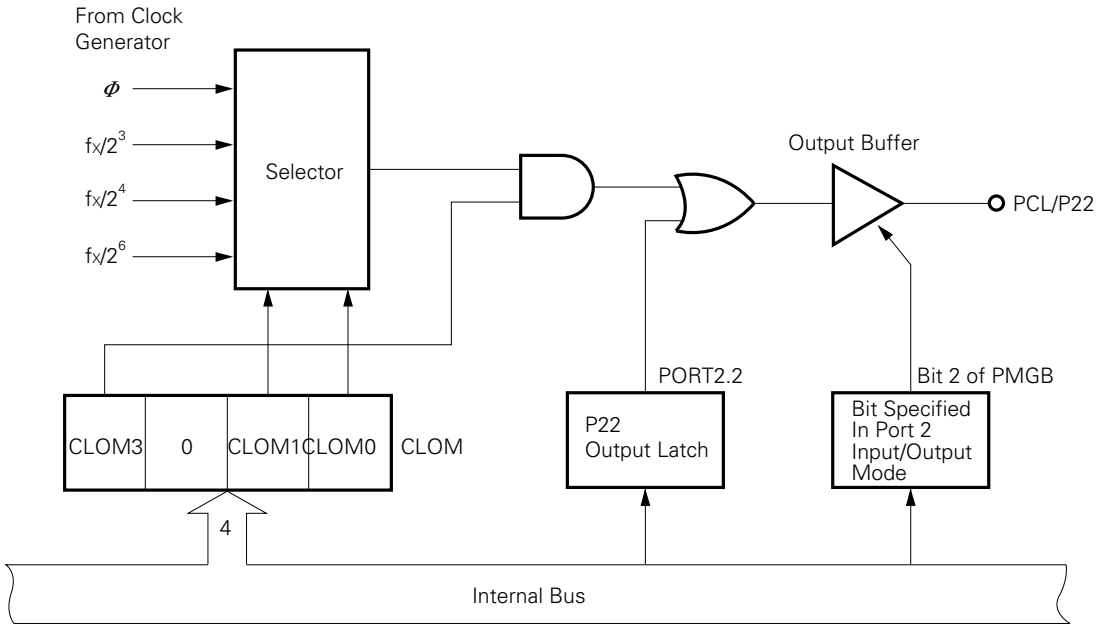
5.3 CLOCK OUTPUT CIRCUIT

The clock output circuit is a circuit which outputs a clock pulse from P22/PCL pin and is used to supply clock pulses to remote control outputs or peripheral LSI's.

- Clock output (PCL) : Φ 524, 262, 65.5 kHz (at 4.19 MHz operation)
- Buzzer output (BUZ): 2 kHz (at 4.19 MHz or 32.768 kHz operation)

The configuration of the clock output circuit is shown below.

Fig. 5-2 Clock Output Circuit Configuration



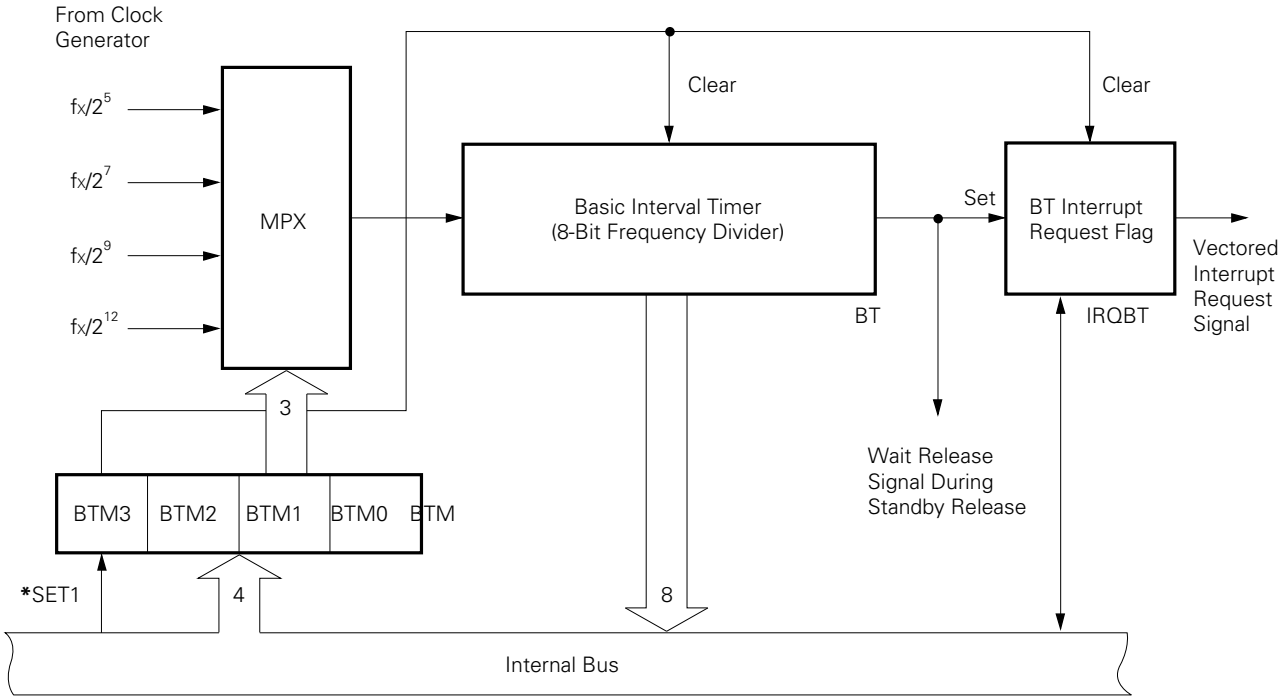
Remarks Consideration is given so that a low amplitude pulse is not output when switching between clock output enable and disable.

5.4 BASIC INTERVAL TIMER

The basic interval timer includes the following functions.

- It operates as an interval timer which generates reference time interrupts.
- It can be applied as a watchdog timer which detects when a program is out of control.
- Selects and counts wait times when the standby mode is released.
- It reads count contents.

Fig. 5-3 Basic Interval Timer Configuration



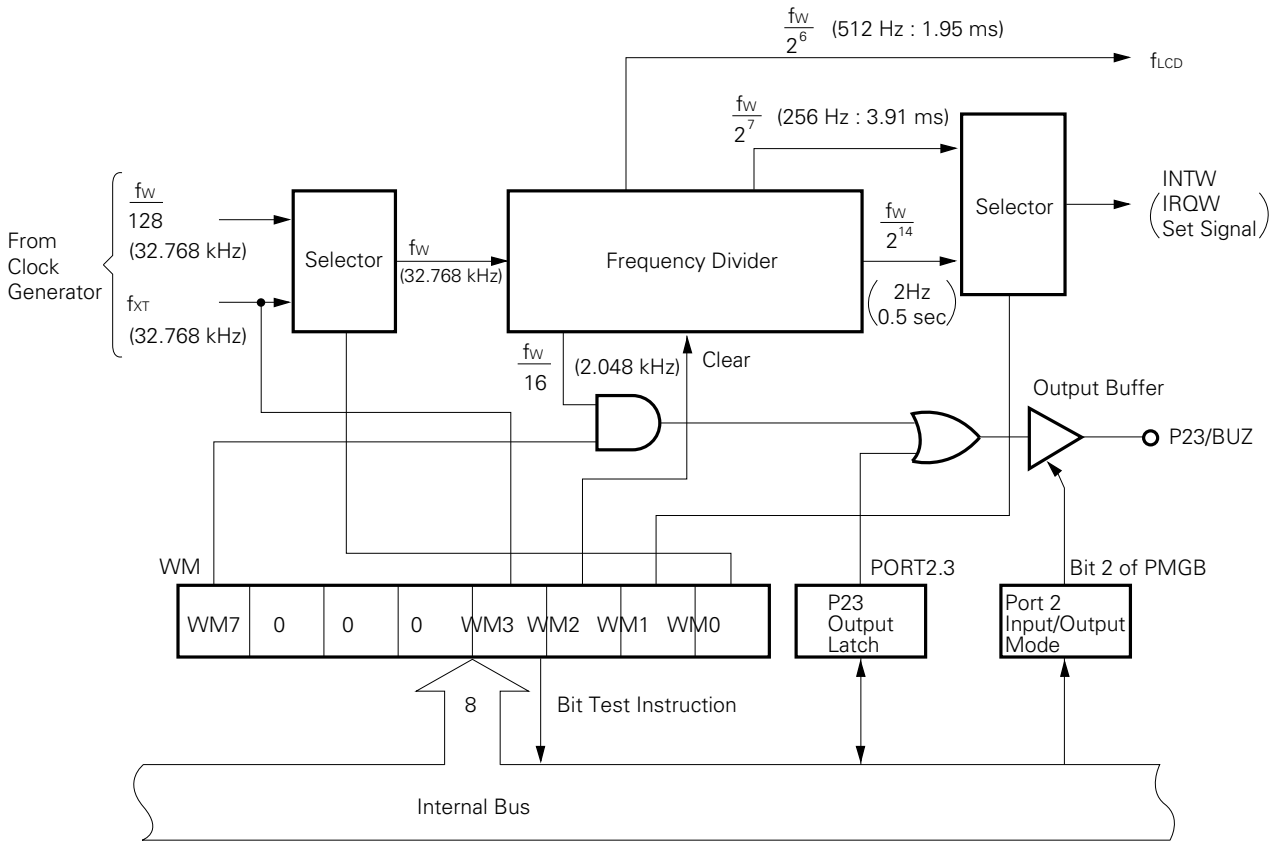
Remarks * indicates instruction execution.

5.5 WATCH TIMER

The μPD75308B incorporates a single watch timer channel. The watch timer has the following functions.

- Sets test flags (IRQW) at 0.5 second intervals. The standby mode can be released with IRQW.
- 0.5 sec. time intervals can be created in either the main system clock or the subsystem clock.
- In the fast watch mode, time intervals which are 128 times normal (3.91 ms) can be set, making this function convenient for program debugging and testing.
- A fixed frequency (2.048 kHz) can be output to the P23/BUZ pin for use in generating buzzer sounds and trimming system clock oscillation frequencies.
- The frequency divider can be cleared, so this clock can be started at 0 second.

Fig. 5-4 Watch Timer Block Diagram



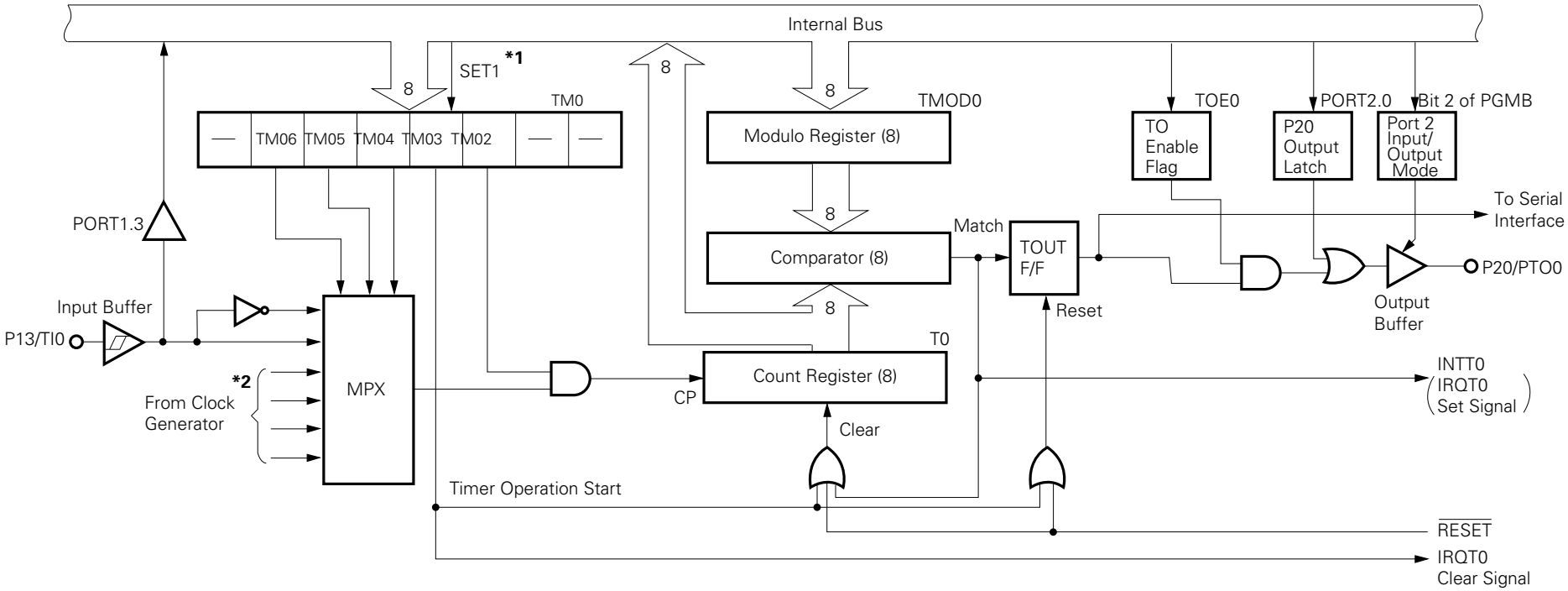
Remarks Values in parentheses are when fx = 4.194304 MHz and fXT = 32.768 kHz.

5.6 TIMER/EVENT COUNTER

The μPD75308B incorporates a single timer/event counter channel. The timer/event counter has the following functions.

- Operates as a programmable interval timer.
- Outputs square waves in the desired frequency to the PTO0 pin.
- Operates as an event counter.
- Divides the TI0 pin input into N divisions and outputs it to the PTO0 pin (frequency divider operation).
- Supplies a serial shift clock to the serial interface circuit.
- Count status read function.

Fig. 5-5 Timer/Event Counter Block Diagram



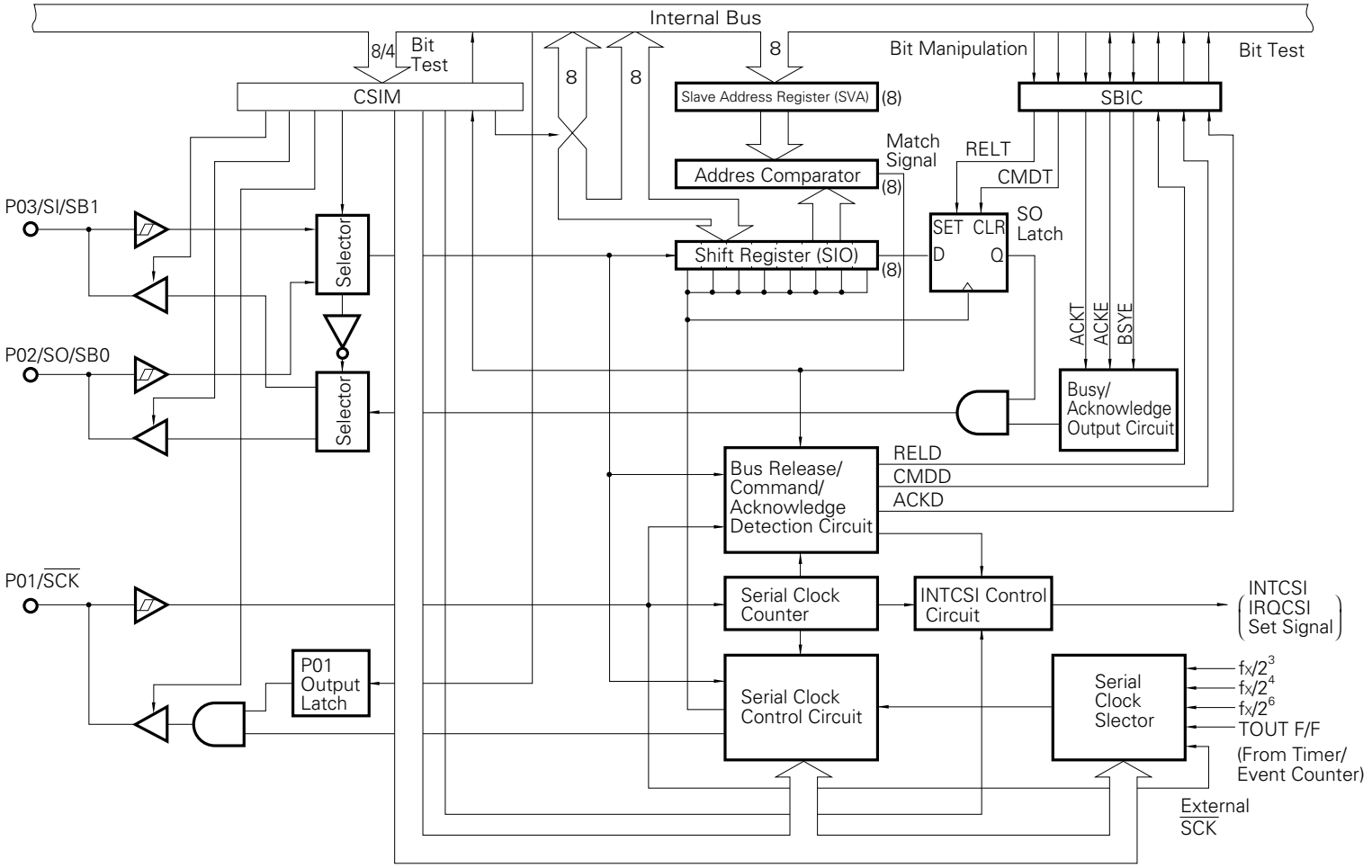
* **1** SET1: Instruction execution
2 For detail, see **Fig. 5-1.**

5.7 SERIAL INTERFACE

The μPD75308B incorporates a clocked 8-bit serial interface. The serial interface has the following three modes.

- 3-wire serial I/O mode
- 2-wire serial I/O mode
- SBI mode (serial bus interface mode)

Fig. 5-6 Serial Interface Block Diagram



5.8 LCD CONTROLLER/DRIVER

The μPD75308B has an on-chip display controller which generates segment signals and common signals in accordance with data in display data memory as well as a segment driver and common driver capable of directly driving the LCD panel.

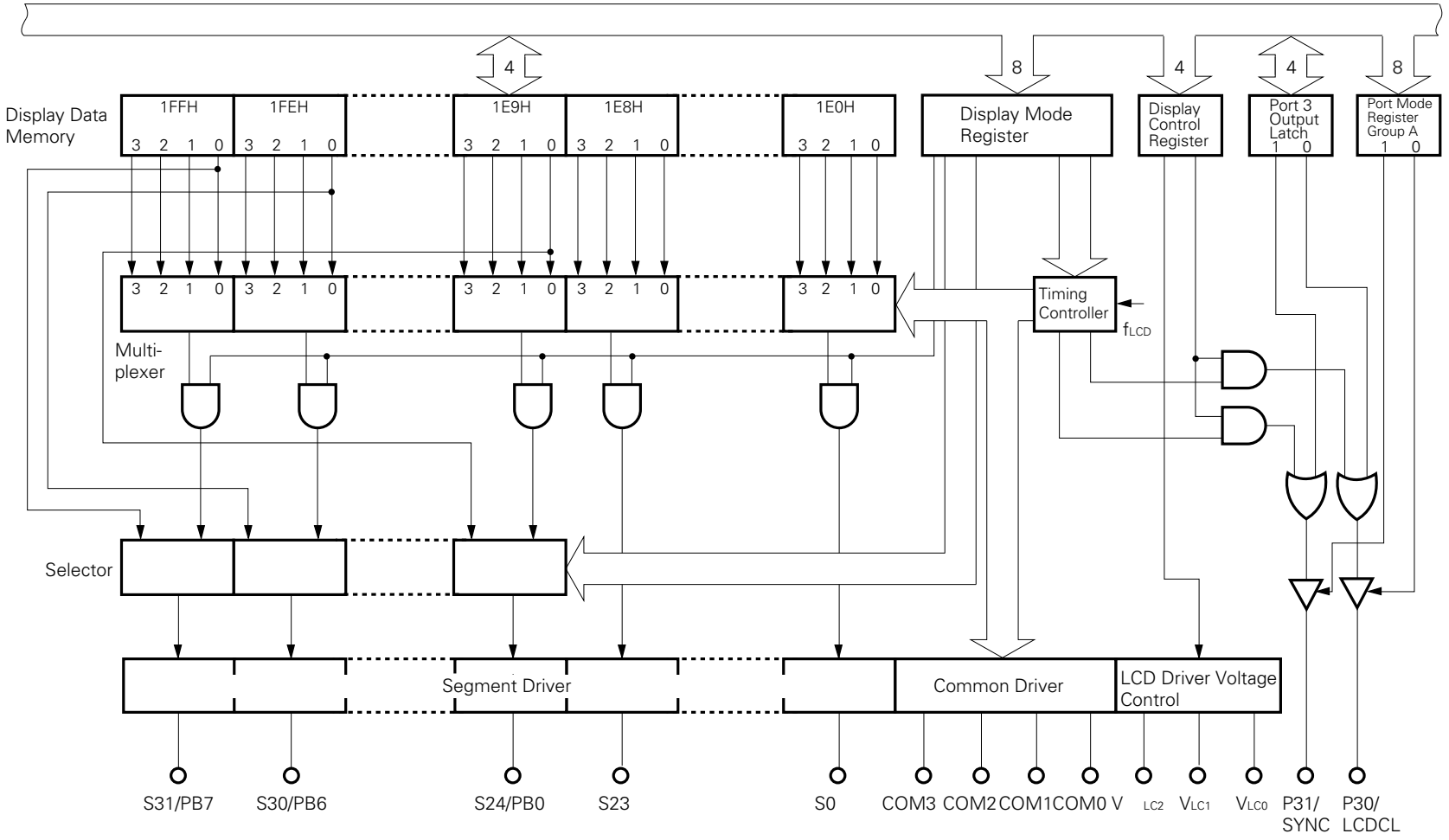
The configuration of the LCD controller/driver is shown in Fig. 5-7

The functions of the on-chip LCD controller/driver of the μPD75308B are as follows.

- Display data memory are read automatically through DMA operations and segment signals and common signals are generated.
- 5 different display modes can be selected.
  - ① Static
  - ② 1/2 duty (1/2 bias)
  - ③ 1/3 duty (1/2 bias)
  - ④ 1/3 duty (1/3 bias)
  - ⑤ 1/4 duty (1/3 bias)
- In each of the display modes, 4 types of frame frequency can be selected.
- The segment signal output is a maximum of 32 segments (S0 to S31) and 4 common outputs (COM0 to COM3).
- Segment signal outputs (S24 to S27, S28 to S31) are in 4-segment units and they can be switched for use as output ports (BP0 to BP3, BP4 to BP7).
- Split resistors can be built-in for the LCD driver power supply (mask option).
  - Conformity to various bias methods and LCD driver voltages is possible.
  - When the display is OFF, the current flowing to the split resistors is cut.
- Display data memory not used for the display can be used as ordinary data memory.
- Operation by the subsystem clock is also possible.

.

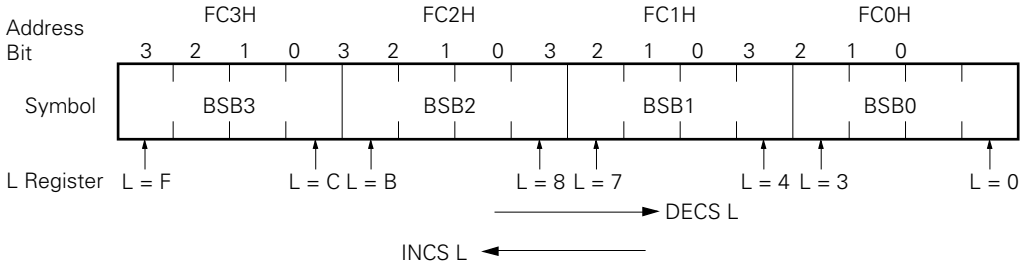
Fig. 5-7 LCD Controller/Driver Block Diagram



5.9 BIT SEQUENTIAL BUFFER ..... 16 BITS

The bit sequential buffer is special data memory for bit manipulations and can be used easily particularly for bit manipulations where addresses and bit specifications are changed sequentially, so it is convenient for processing data with long bit lengths bit-wise.

Fig. 5-8 Bit Sequential Buffer Format



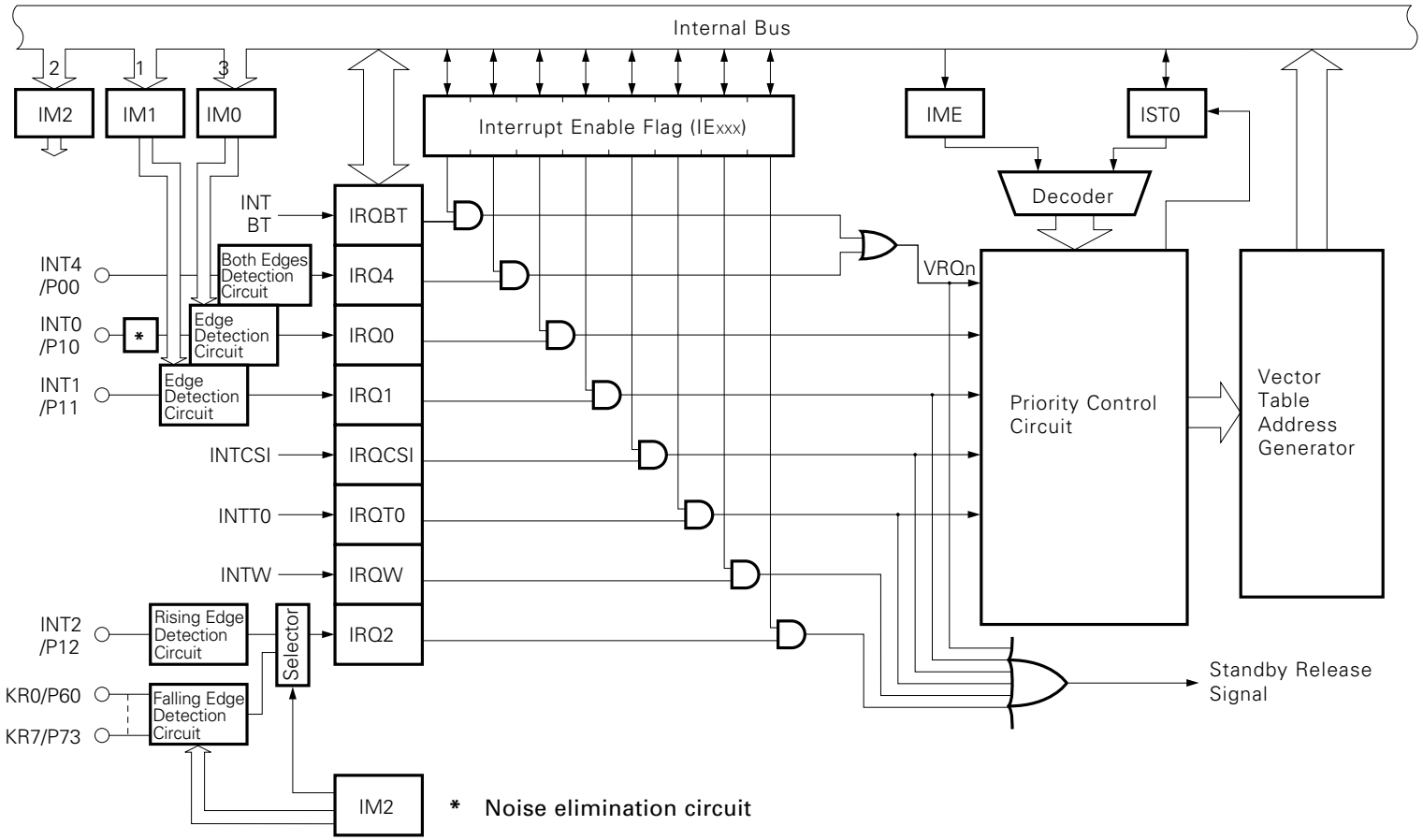
Remarks In pmem.@L addressing, the specified bit corresponding to the L register is moved.

6. INTERRUPT FUNCTION

The μPD75218has 8 interrupt sources, and prioritized multiple interrupts are possible.
There are also two test sources, of which INT2 is an edge-detected testable input.
The μPD75218 interrupt control circuit has the following functions

- Hardware control vectored interrupt function that can control interrupt acceptance by interrupt flag (IE×××) and interrupt master enable flag (IME).
- Arbitrary setting of interrupt start address.
- Multiple interrupt function with priority specifiable by the interrupt priority selection register (IPS).
- Interrupt request flag (IRQ×××) test function (interrupt generation confirmation by software possible).
- Standby mode release (selection of interrupt that releases the standby mode by interrupt enable flag possible).

Fig. 6-1 Interrupt Control Circuit Block Diagram



7. STANDBY FUNCTION

To reduce the power consumption during program wait, the μPD75308B has two standby modes: STOP mode and HALT mode.

Table 7-1 Operation Status at Standby Mode

		STOP Mode	HALT Mode
Setting instruction		STOP instruction	HALT instruction
System clock at setting		Only main system clock settable	Main system clock or subsystem clock settable
Operation Status	Clock oscillator	Only main system clock oscillation stopped	Only CPU clock Φ stopped (oscillation continued)
	Basic interval timer	Stopped	Operating (IRQBT set at reference time intervals)*
	Serial interface	Operable only when external $\overline{SCK}$ input selected as serial clock	Operable*
	Timer/event counter	Operable only when TI0 pin input specified as count clock	Operable*
	Watch timer	Operable only when f_{XT} selected as count clock	Operable
	LCD controller	Operable only when f_{XT} selected as LCDCL	Operable
	External interrupt	INT1, 2, 4: Operable Only INT0 inoperable	
	CPU	Stopped	
Release signal		Interrupt request signal from operable hardware enabled by interrupt enable flag, or $\overline{RESET}$ input	Interrupt request signal from operable hardware enabled by interrupt enable flag, or $\overline{RESET}$ input

* In-operable only with main system clock oscillation stopped.

8. RESET FUNCTION

The μPD75308B is reset and the hardware is initialized as shown in Table 8-1 by $\overline{\text{RESET}}$ input. The reset operation timing is shown in Fig. 8-1.

Fig. 8-1 Reset Operation by $\overline{\text{RESET}}$ Input

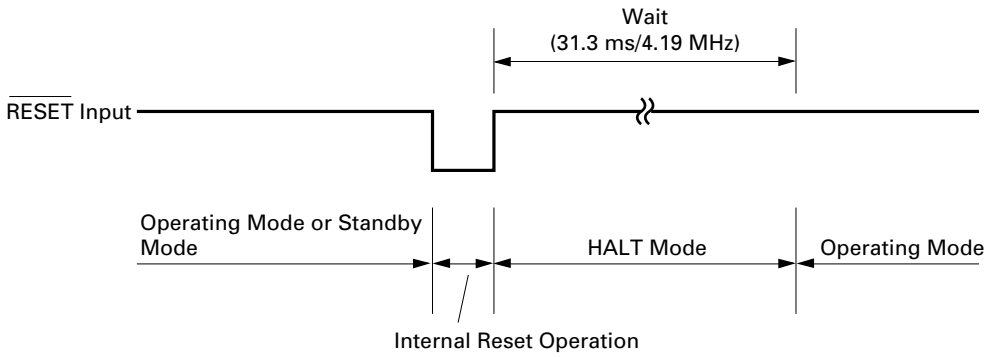


Table 8-1 Status of Each Hardware after Resetting (1/2)

Hardware		$\overline{\text{RESET}}$ Input in Standby Mode	$\overline{\text{RESET}}$ Input during Operation
Program counter (PC)		Low-order 5(4)***1** bits of program memory address 0000H are set in PC12(11)***1** to 8 and the contents of address 0001H are set in PC7 to 0.	Low-order 5(4)***1** bits of program memory address 0000H are set in PC12(11)***1** to 8 and the contents of address 0001H are set in PC7 to 0.
PSW	Carry flag (CY)	Held	Undefined
	Skip flag (SK0 to 2)	0	0
	Interrupt status flag (IST0)	0	0
	Bank enable flag (MBE)	Bit 7 of program memory address 0000H is set in MBE.	Bit 7 of program memory address 0000H is set in MBE.
Stack pointer (SP)		Undefined	Undefined
Data memory (RAM)		Held***2**	Undefined
General register (X, A, H, L, D, E, B, C)		Held	Undefined
Bank selection register (MBS)		0	0

* **1.** Figures in parentheses apply to the μPD75304B.

2. Data of data memory addresses 0F8H to 0FDH becomes undefined by $\overline{\text{RESET}}$ input.

Table 8-1 Status of Each Hardware after Resetting (2/2)

Hardware		$\overline{\text{RESET}}$ Input in Standby Mode	$\overline{\text{RESET}}$ Input during Operation
Basic interval timer	Counter (BT)	Undefined	Undefined
	Mode register (BTM)	0	0
Timer/event counter	Counter (To)	0	0
	Modulo register (TMOD0)	FFH	FFH
	Mode Register (TM0)	0	0
	TOE0, TOUT F/F	0,0	0,0
Watch timer	Mode register (WM)	0	0
Serial interface	Shift register (SIO)	Held	Undefined
	Operating mode register (CSIM)	0	0
	SBI control register (SBIC)	0	0
	Slave address register (SVA)	Held	Undefined
Clock generator, clock output circuit	Processor clock control register (PCC)	0	0
	System clock control register (SCC)	0	0
	Clock output mode register (CLOM)	0	0
LCD controller	Display mode register (LCDM)	0	0
	Display control register (LCDC)	0	0
Interrupt function	Interrupt request flag (IRQ×××)	Reset (0)	Reset (0)
	Interrupt enable flag (IE×××)	0	0
	Interrupt master enable flag (IME)	0	0
	INT0, 1, 2 mode registers (IM0, 1, 2)	0, 0, 0	0, 0, 0
Digital port	Output buffer	OFF	OFF
	Output latch	Clear (0)	Clear (0)
	I/O mode register (PMGA, B)	0	0
	Pull-up resistor specification register (POGA)	0	0
Bit sequential buffer (BSB0 to 3)		Held	Undefined

9. INSTRUCTION SET

(1) Operand identifier and description

The operand is described in the operand field of each instruction in accordance with the description for the operand identifier of the instruction. (See the **RA75X Assembler Package User's Manual Language Volume (EEU-730)** for details.) When there are multiple elements in the description, one of the elements is selected. Upper case letters and symbols (+,–) are keywords and are described unchanged.

For immediate data, a suitable value or label is described.

Various register or flag symbols can be used as a label instead of mem, fmem, pmem, bit, etc. (See the **μPD75308 User's Manual (IEM-5016)** for details). However, there are restrictions on the labels for which fmem and pmem can be used (see the table on the previous page).

Identifier	Description	
reg regl	X, A, B, C, D, E, H, L X, B, C, D, E, H, L	
rp rpl rp2	XA, BC, DE, HL BC, DE, HL BC, DE	
rpa rpal	HL, DE, DL DE, DL	
n4 n8	4-bit immediate data or label 8-bit immediate data or label	
mem* bit	8-bit immediate data or label 2-bit immediate data or label	
fmem pmem	FB0H to FBFH, FF0H to FFFH immediate data or label FC0H to FFFH immediate data or label	
addr	μPD75304B	0000H to 0FFFH immediate data or lebel
	μPD75306B	0000H to 177FH immediate data or lebel
	μPD75308B	0000H to 1F7FH immediate data or lebel
caddr	12-bit immediate data or label	
faddr	11-bit immediate data or label	
taddr	20H to 7FH immediate data (however, bit0 = 0) or label	
PORTn IE××× MBn	PORT 0 to PORT 7 IEBT, IECSI, IET0, IE0, IE1, IE2, IE4, IEW MB0, MB1, MB15	

* Only an even address can be written for mem in the case of 8-bit data processing.

(2) Operation description legend

A	:	A register; 4-bit accumulator
B	:	B register;
C	:	C register;
D	:	D register;
E	:	E register;
H	:	H register;
L	:	L register;
X	:	X register; 4-bit accumulator
XA	:	Register pair (XA); 8-bit accumulator
BC	:	Register pair (BC)
DE	:	Register pair (DE)
HL	:	Register pair (HL)
PC	:	Program counter
SP	:	Stack pointer
CY	:	Carry flag; bit accumulator
PSW	:	Program status word
MBE	:	Memory bank enable flag
PORTn	:	Portn (n = 0 to 7)
IME	:	Interrupt master enable flag
IE×××	:	Interrupt enable flag
MBS	:	Memory bank selection register
PCC	:	Processor clock control register
•	:	Address, bit delimiter
(××)	:	Contents addressed by ××
××H	:	Hexadecimal data

(3) Description of addressing area field symbols

*1	MB = MBE • MBS (MBS = 0, 1, 15)		Data memory addressing
*2	MB = 0		
*3	MBE = 0 : MB = 0 (00H to 7FH) MB = 15 (80H to FFH) MBE = 1 : MB = MBS (MBS = 0, 1, 15)		
*4	MB = 15, fmem = FB0H to FBFH, FF0H to FFFH		
*5	MB = 15, pmem = FC0H to FFFH		
*6	μPD75304B	addr=0000H to 0FFFH	Program memory addressing
	μPD75306B	addr=0000H to 177FH	
	μPD75308B	addr=0000H to 1F7FH	
*7	addr = (Current PC) –15 to (Current PC) –1 (Current PC) + 2 to (Current PC) + 16		
*8	μPD75304B	caddr= 0000H to 0FFFH	
	μPD75306B	caddr= 0000H to 0FFFH (PC_{12}=0) or 1000H to 177FH (PC_{12}=1)	
	μPD75308B	caddr=0000H to 0FFFH (PC_{12}=0) or 1000H to 1F7FH (PC_{12}=1)	
*9	faddr = 0000H to 07FFH		
*10	taddr = 0020H to 007FH		

Remarks **1.** MB indicates the accessible memory bank.
2. For *2, MB = 0 without regard to MBE and MBS.
3. For *4 and *5, MB = 15 without regard to MBE and MBS.
4. *6 to *10 indicate the addressable area.

(4) Explanation of machine cycle field

S shows the number of machine cycles required when skip is performed by an instruction with skip. The value of S changes as follows:

- No skip ..... S = 0
- When instruction to be skipped is 1-byte or 2-byte instruction ..... S = 1
- When instruction to be skipped is 3-byte instruction (BR !addr, CALL !addr instruction) ..... S = 2

Note One machine cycle is required to skip a GETI instruction.

One machine cycle is equivalent to one cycle (=t_{CY}) of the CPU clock Φ. Three times can be selected by PCC setting.

Note	Mnemonic	Operand	Bytes	Machine Cycles	Operation	Addressing Area	Skip Condition
Transfer	MOV	A, #n4	1	1	A ← n4		Stack A
		regl, #n4	2	2	regl ← n4		
		XA, #n8	2	2	XA ← n8		Stack A
		HL, #n8	2	2	HL ← n8		Stack B
		rp2, #n8	2	2	rp2 ← n8		
		A, @HL	1	1	A ← (HL)	*1	
		A, @rpal	1	1	A ← (rpal)	*2	
		XA, @HL	2	2	XA ← (HL)	*1	
		@HL, A	1	1	(HL) ← A	*1	
		@HL, XA	2	2	(HL) ← XA	*1	
		A, mem	2	2	A ← (mem)	*3	
		XA, mem	2	2	XA ← (mem)	*3	
		mem, A	2	2	(mem) ← A	*3	
		mem, XA	2	2	(mem) ← XA	*3	
		A, reg	2	2	A ← reg		
		XA, rp	2	2	XA ← rp		
		regl, A	2	2	regl ← A		
		rpl, XA	2	2	rpl ← XA		
	XCH	A, @HL	1	1	A ↔ (HL)	*1	
		A, @rpal	1	1	A ↔ (rpal)	*2	
		XA, @HL	2	2	XA ↔ (HL)	*1	
		A, mem	2	2	A ↔ (mem)	*3	
		XA, mem	2	2	XA ↔ (mem)	*3	
		A,regl	1	1	A ↔ regl		
		XA, rp	2	2	XA ↔ rp		
Table reference	MOVT	XA, @PCDE	1	3	● **μPD75304B** XA ← $(PC_{11-8} + DE)_{ROM}$ ● **μPD75306B, 75308B** XA ← $(PC_{12-8} + DE)_{ROM}$		
		XA, @PCXA	1	3	● **μPD75304B** XA ← $(PC_{11-8} + XA)_{ROM}$ ● **μPD75306B, 75308B** XA ← $(PC_{12-8} + XA)_{ROM}$		
Operation	ADDS	A, #n4	1	1 + S	A ← A + n4		carry
		A, @HL	1	1 + S	A ← A + (HL)	*1	carry
	ADDC	A, @HL	1	1	A, CY ← A + (HL) + CY	*1	
	SUBS	A, @HL	1	1 + S	A ← A – (HL)	*1	borrow
	SUBC	A, @HL	1	1	A, CY ← A – (HL) – CY	*1	

Note Instruction Group

Note 1	Mnemonic	Operand	Bytes	Machine Cycles	Operation	Addressing Area	Skip Condition
Operation	AND	A, #n4	2	2	A ← A ∧ n4		
		A, @HL	1	1	A ← A ∧ (HL)	*1	
	OR	A, #n4	2	2	A ← A ∨ n4		
		A, @HL	1	1	A ← A ∨ (HL)	*1	
	XOR	A, #n4	2	2	A ← A ⊻ n4		
		A, @HL	1	1	A ← A ⊻ (HL)	*1	
Note 2	RORC	A	1	1	CY ← A_0, A_3 ← CY, A_{n-1} ← A_n		
	NOT	A	2	2	A ← $\overline{A}$		
Note 3	INCS	reg	1	1 + S	reg ← reg + 1		reg = 0
		@HL	2	2 + S	(HL) ← (HL) + 1	*1	(HL) = 0
		mem	2	2 + S	(mem) ← (mem) + 1	*3	(mem) = 0
	DECS	reg	1	1 + S	reg ← reg – 1		reg = FH
Comparison	SKE	reg, #n4	2	2 + S	Skip if reg = n4		reg = n4
		@HL, #n4	2	2 + S	Skip if (HL) = n4	*1	(HL) = n4
		A, @HL	1	1 + S	Skip if A = (HL)	*1	A = (HL)
		A, reg	2	2 + S	Skip if A = reg		A = reg
Note 4	SET1	CY	1	1	CY ← 1		
	CLR1	CY	1	1	CY ← 0		
	SKT	CY	1	1 + S	Skip if CY = 1		CY = 1
	NOT1	CY	1	1	$\overline{CY}$ ← CY		
Memory bit manipulation	SET1	mem.bit	2	2	(mem.bit) ← 1	*3	
		fmem.bit	2	2	(fmem.bit) ← 1	*4	
		pmem.@L	2	2	(pmem$_{7-2}$ + L$_{3-2}$.bit (L$_{1-0}$)) ← 1	*5	
		@H + mem.bit	2	2	(H + mem$_{3-0}$.bit) ← 1	*1	
	CLR1	mem.bit	2	2	(mem.bit) ← 0	*3	
		fmem.bit	2	2	(fmem.bit) ← 0	*4	
		pmem.@L	2	2	(pmem$_{7-2}$ + L$_{3-2}$.bit (L$_{1-0}$)) ← 0	*5	
		@H + mem.bit	2	2	(H + mem$_{3-0}$.bit) ← 0	*1	
	SKT	mem.bit	2	2 + S	Skip if (mem.bit) = 1	*3	(mem.bit) = 1
		fmem.bit	2	2 + S	Skip if (fmem.bit) = 1	*4	(fmem.bit) = 1
		pmem.@L	2	2 + S	Skip if (pmem$_{7-2}$ + L$_{3-2}$.bit (L$_{1-0}$)) = 1	*5	(pmem.@L) = 1
		@H + mem.bit	2	2 + S	Skip if (H + mem$_{3-0}$.bit) = 1	*1	(@H + mem.bit) = 1
	SKF	mem.bit	2	2 + S	Skip if (mem.bit) = 0	*3	(mem.bit) = 0
		fmem.bit	2	2 + S	Skip if (fmem.bit) = 0	*4	(fmem.bit) = 0
		pmem.@L	2	2 + S	Skip if (pmem$_{7-2}$ + L$_{3-2}$.bit (L$_{1-0}$)) = 0	*5	(pmem.@L) = 0
		@H + mem.bit	2	2 + S	Skip if (H + mem$_{3-0}$.bit) = 0	*1	(@H + mem.bit) = 0

Note **1.** Instruction Group
2. Accumulator operation
3. Increment and decrement
4. Carry flag operation

Note	Mnemonic	Operand	Bytes	Machine Cycles	Operation	Addressing Area	Skip Condition
Memory bit manipulation	SKTCLR	fmem.bit	2	2 + S	Skip if (fmem.bit) = 1 and clear	*4	(fmem.bit) = 1
		pmem.@L	2	2 + S	Skip if ($pmem_{7-2}$ + L_{3-2}.bit (L_{1-0})) = 1 and clear	*5	(pmem.@L) = 1
		@H + mem.bit	2	2 + S	Skip if (H + mem_{3-0}.bit) = 1 and clear	*1	(@H + mem.bit) = 1
	AND1	CY, fmem.bit	2	2	CY ← CY ∧ (fmem.bit)	*4	
		CY, pmem.@L	2	2	CY ← CY ∧ ($pmem_{7-2}$ + L_{3-2}.bit (L_{1-0}))	*5	
		CY, @H + mem.bit	2	2	CY ← CY ∧ (H + mem_{3-0}.bit)	*1	
	OR1	CY, fmem.bit	2	2	CY ← CY ∨ (fmem.bit)	*4	
		CY, pmem.@L	2	2	CY ← CY ∨ ($pmem_{7-2}$ + L_{3-2}.bit (L_{1-0}))	*5	
		CY, @H + mem.bit	2	2	CY ← CY ∨ (H + mem_{3-0}.bit)	*1	
	XOR1	CY, fmem.bit	2	2	CY ← CY ⊻ (fmem.bit)	*4	
		CY, pmem.@L	2	2	CY ← CY ⊻ ($pmem_{7-2}$ + L_{3-2}.bit (L_{1-0}))	*5	
		CY, @H + mem.bit	2	2	CY ← CY ⊻ (H + mem_{3-0}.bit)	*1	
Branch	BR	addr	—	—	● μPD75304B PC_{11-0} ← addr (The assembler selects the optimum instruction from among the BRCB !caddr, and BR $addr instructions.)	*6	
					● μPD75306B, 75308B PC_{12-0} ← addr (The assembler selects the optimum instruction from among the BR !addr, BRCB !caddr, and BR $addr instructions.)		
		!addr	3	3	● μPD75306B, 75308B PC_{12-0} ← addr	*6	
		$addr	1	2	● μPD75304B PC_{11-0} ← addr	*7	
					● μPD75306B, 75308B PC_{12-0} ← addr		
	BRCB	!caddr	2	2	● μPD75304B PC_{11-0} ← $caddr_{11-0}$	*8	
					● μPD75306B, 75308B PC_{12-0} ← PC_{12} + $caddr_{11-0}$		
Subroutine stack control	CALL	!addr	3	3	● μPD75304B (SP – 4) (SP – 1) (SP – 2) ← PC_{11-0} (SP – 3) ← MBE, 0, 0, 0 PC_{11-0} ← addr, SP ← SP – 4	*6	
					● μPD75306B, 75308B (SP – 4) (SP – 1) (SP – 2) ← PC_{11-0} (SP – 3) ← MBE, 0, 0, PC_{12} PC_{12-0} ← addr, SP ← SP – 4		

Note Instruction Group

Note 1	Mnemonic	Operand	Bytes	Machine Cycles	Operation	Addressing Area	Skip Condition
Subroutine stack control	CALLF	!faddr	2	2	● μPD75304B (SP – 4) (SP – 1) (SP – 2) ← PC_{11-0} (SP – 3) ← MBE, 0, 0, 0 PC_{11-0} ← 0, faddr, SP ← SP – 4 ● μPD75306B, 75308B (SP – 4) (SP – 1) (SP – 2) ← PC_{11-0} (SP – 3) ← MBE, 0, 0, PC_{12} PC_{12-0} ← 00, faddr, SP ← SP – 4	*9	
	RET		1	3	● μPD75304B MBE, ×, ×, × ← (SP + 1) PC_{11-0} ← (SP) (SP + 3) (SP + 2) SP ← SP + 4 ● μPD75306B, 75308B MBE, ×, ×, PC_{12} ← (SP + 1) PC_{11-0} ← (SP) (SP + 3) (SP + 2) SP ← SP + 4		
	RETS		1	3+S	● μPD75304B MBE, ×, ×, × ← (SP + 1) PC_{11-0} ← (SP) (SP + 3) (SP + 2) SP ← SP + 4 the skip unconditionally ● μPD75306B, 75308B MBE, ×, ×, PC_{12} ← (SP + 1) PC_{11-0} ← (SP) (SP + 3) (SP + 2) SP ← SP + 4 the skip unconditionally		Unconditional
	RETI		1	3	● μPD75304B MBE, ×, ×, × ← (SP + 1) PC_{11-0} ← (SP) (SP + 3) (SP + 2) PSW ← (SP + 4) (SP + 5), SP ← SP + 6 ● μPD75306B, 75308B MBE, ×, ×, PC_{12} ← (SP + 1) PC_{11-0} ← (SP) (SP + 3) (SP + 2) PSW ← (SP + 4) (SP + 5), SP ← SP + 6		
	PUSH	rp	1	1	(SP – 1) (SP – 2) ← rp, SP ← SP – 2		
		BS	2	2	(SP – 1) ← MBS, (SP – 2) ← 0, SP ← SP – 2		
	POP	rp	1	1	rp ← (SP + 1) (SP), SP ← SP + 2		
		BS	2	2	MBS ← (SP + 1), SP ← SP + 2		
Note 2	EI		2	2	IME ← 1		
		IE×××	2	2	IE××× ← 1		
	DI		2	2	IME ← 0		
		IE×××	2	2	IE××× ← 0		

Note **1.** Instruction Group
2. Interrupt control

Note 1	Mnemonic	Operand	Bytes	Machine Cycles	Operation	Addressing Area	Skip Condition
Input/output	IN*	A, PORTn	2	2	A ← $PORT_n$ (n = 0–7)		
		XA, PORTn	2	2	XA ← $PORT_{n+1}$, $PORT_n$ (n = 4, 6)		
	OUT*	PORTn, A	2	2	$PORT_n$ ← A (n = 2–7)		
		PORTn, XA	2	2	$PORT_{n+1}$, $PORT_n$ ← XA (n =4, 6)		
Note 2	HALT		2	2	Set HALT Mode (PCC.2 ← 1)		
	STOP		2	2	Set STOP Mode (PCC.3 ← 1)		
	NOP		1	1	No Operation		
Special	SEL	MBn	2	2	MBS ← n (n = 0, 1, 15)		
	GETI	taddr	1	3	● μPD75304B • TBR Instruction PC_{11-0} ← (taddr) $_{3-0}$ + (taddr + 1)	*10	
					• TCALL Instruction (SP – 4) (SP – 1) (SP – 2) ← PC_{11-0} (SP – 3) ← MBE, 0, 0, 0 PC_{11-0} ← (taddr) $_{3-0}$ ← (taddr + 1) SP ← SP – 4		
					• Other than TBR and TCALL Instruction Execution of an instruction addressed at (taddr) and (taddr + 1)		Conforms to referenced instruction.
					● μPD75306, 75308BB • TBR Instruction PC_{12-0} ← (taddr) $_{4-0}$ + (taddr + 1)		
					• TCALL Instruction (SP – 4) (SP – 1) (SP – 2) ← PC_{11-0} (SP – 3) ← MBE, 0, 0, PC_{12} PC_{12-0} ← (taddr) $_{4-0}$ ← (taddr + 1) SP ← SP – 4		
					• Other than TBR and TCALL Instruction Execution of an instruction addressed at (taddr) and (taddr + 1)		Conforms to referenced instruction.

* At IN/OUT instruction execution, MBE = 0 or MBE = 1, MBS = 15 must be set in advance.

Note **1.** Instruction Group
2. CPU control

Remarks The TBR and TCALL instructions are assembler pseudo-instructions for GETI instruction table definition.

10. MASK OPTION SELECTION

The following pin mask options are available.

Pin Functions	Mask Options
P40 to P43, P50 to P53	● Pull-up resistor incorporated (specifiable bit-wise) ● No pull-up resistor (specifiable bit-wise)
V_{LC0} to V_{LC2}, BIAS	● LCD drive power supply split resistor incorporated (specifiable as 4-bit unit) ● No LCD drive power supply split resistor (specifiable as 4-bit unit)

11. ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (Ta = 25 °C)

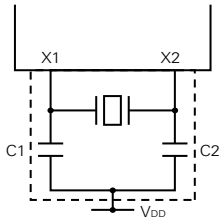
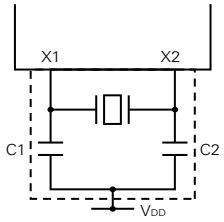
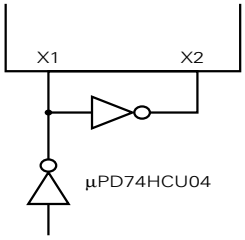
PARAMETER	SYMBOL	TEST CONDITIONS		RATING	UNIT
Power supply voltage	V_{DD}			–0.3 to +7.0	V
Input voltage	V_{I1}	Except ports 4 and 5		–0.3 to V_{DD} +0.3	V
	V_{I2}	Ports 4 and 5	On-chip pull-up resistor	–0.3 to V_{DD} +0.3	V
			Open–drain	–0.3 to +11	V
Output voltage	V_O			–0.3 to V_{DD} +0.3	V
Output current high	I_{OH}	One pin		–15	mA
		All pins		–30	mA
Output current low	I_{OL}*	One pin	Peak value	30	mA
			rms	15	mA
		Total of ports 0, 2, 3 and 5	Peak value	100	mA
			rms	60	mA
		Total of ports 4, 6, and 7	Peak value	100	mA
			rms	60	mA
Operating temperature	T_{opt}			–40 to +85	°C
Storage temperature	T_{stg}			–65 to +150	°C

* Rms is calculated using the following expression: [rms] = [peak value] $\times \sqrt{\text{duty}}$

CAPACITANCE (Ta = 25 °C, V_{DD} = 0 V)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}	f = 1 MHz Unmeasured pins returned to 0 V.			15	pF
Output capacitance	C_{OUT}				15	pF
I/O capacitance	C_{IO}				15	pF

MAIN SYSTEM CLOCK OSCILLATOR CHARACTERISTICS (Ta = –40 to +85 °C, V_{DD} = 2.0 to 6.0 V)

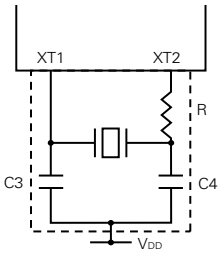
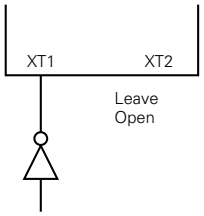
RESONATOR	RECOMMENDED CONSTANT	PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Ceramic resonator***3**		Oscillator frequency (f_X)***1**		1.0		5.0***3**	MHz
		Oscillation stabilization time***2**	After V_{DD} reached the MIN. of the oscillation voltage range			4	ms
Crystal resonator***3**		Oscillator frequency (f_X)***1**		1.0	4.19	5.0***3**	MHz
		Oscillation stabilization time***2**	V_{DD} = 4.5 to 6.0 V			10	ms
						30	ms
External clock		X1 input frequency (f_X)***1**		1.0		5.0***3**	MHz
		X1 input high-/low-level width (t_{XH}, t_{XL})		100		500	ns

***** **1.** The oscillator frequency and X1 input frequency indicate only the oscillator characteristics. For the instruction execution time refer to the AC characteristics.

2. The oscillation stabilization time is necessary for oscillation to stabilize after applying V_{DD} or releasing the STOP mode.

3. When the oscillation frequency is 4.19 MHz < f_X ≤ 5.0 MHz, PCC = 0011 should not be selected as the instruction execution time. If PCC = 0011 is selected, one machine cycle is less than 0.95 s, and the specification MIN. value of 0.95 μs will not be achieved. ★

SUBSYSTEM CLOCK OSCILLATOR CHARACTERISTICS (Ta = –40 to +85 °C, V_{DD} = 2.0 to 6.0 V)

RESONATOR	RECOMMENDED CONSTANT	PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Crystal resonator		Oscillator frequency (f_{XT})		32	32.768	35	kHz
		Oscillation stabilization time*	V_{DD} = 4.5 to 6.0 V		1.0	2	s
						10	s
External clock		XT1 input frequency (f_{XT})		32		100	kHz
		XT1 input high-/low-level width (t_{XTH},t_{XTL})		5		15	μs

* This is the time required for oscillation to stabilize after V_{DD} reaches the MIN. value of the oscillation voltage range.

★ **Note When the main system clock and subsystem clock oscillators are used, the following should be noted concerning wiring in the area in the figure enclosed by a dotted line to prevent the influence of wiring capacitance, etc.**

- **The wiring should be kept as short as possible.**
- **No other signal lines should be crossed. Keep away from lines carrying a high fluctuating current.**
- **The oscillator capacitor grounding point should be at the same potential as V_{DD}. Do not ground to a ground pattern carrying a high current.**
- **A signal should not be taken from the oscillator.**

The subsystem clock oscillator is a low-amplitude circuit in order to achieve a low consumption current, and is more prone to misoperation due to noise than the main system clock oscillator. Particular care is therefore required with the wiring method when the subsystem clock is used.

DC CHARACTERISTICS (Ta = –40 to +85 °C, V_{DD} = 2.7 to 6.0 V) (1/2)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Input voltage high	V_{IH1}	Ports 2 and 3		0.7 V_{DD}		V_{DD}	V
	V_{IH2}	Ports 0,1,6,7, $\overline{RESET}$		0.8 V_{DD}		V_{DD}	V
	V_{IH3}	Ports 4 and 5	On-chip pull-up resistor	0.7 V_{DD}		V_{DD}	V
			Open–drain	0.7 V_{DD}		10	V
	V_{IH4}	X1, X2, XT1		V_{DD} –0.5		V_{DD}	V
Input voltage low	V_{IL1}	Ports 2, 3, 4 and 5		0		0.3 V_{DD}	V
	V_{IL2}	Ports 0, 1, 6, 7 $\overline{RESET}$		0		0.2 V_{DD}	V
	V_{IL3}	X1, X2, XT1		0		0.4	V
Output voltage high	V_{OH1}	Ports 0, 2,3, 6, 7, BIAS	V_{DD} = 4.5 to 6.0 V I_{OH} = –1 mA	V_{DD} –1.0			V
			I_{OH} = -100 μA	V_{DD} –0.5			V
	V_{OH2}	BP0 to BP7 (with 2 I_{OH} outputs)	V_{DD} = 4.5 to 6.0 V I_{OH} = –100 μA	V_{DD} –2.0			V
			I_{OH} = –30 μA	V_{DD} –1.0			V
Output voltage low	V_{OL1}	Ports 0, 2, 3, 4, 5, 6 and 7	Ports 3, 4 and 5 V_{DD} = 4.5 to 6.0 V I_{OL} = 15 mA		0.5	2.0	V
			V_{DD} = 4.5 to 6.0 V I_{OL} = 1.6 mA			0.4	V
			I_{OL} = 400 μA			0.5	V
		SB0, 1	Open–drain pull-up resistor ≥ 1 kΩ			0.2 V_{DD}	V
	V_{OL2}	BP0 to BP7 (with 2 I_{OL} outputs)	V_{DD} = 4.5 to 6.0 V I_{OL} = 100 μA			1.0	V
			I_{OL} = 50 μA			1.0	V
Input leakage current high	I_{LIH1}	V_{IN} = V_{DD}	Other than below			3	μA
	I_{LIH2}		X1, X2, XT1			20	μA
	I_{LIH3}	V_{IN} = 10 V	Ports 4 and 5 (when open–drain)			20	μA
Input leakage current low	I_{LIL1}	V_{IN} = 0 V	Other than below			–3	μA
	I_{LIL2}		X1, X2, XT1			–20	μA
Output leakage current high	I_{LOH1}	V_{OUT} = V_{DD}	Other than below			3	μA
	I_{LOH2}	V_{OUT} = 10 V	Ports 4 and 5 (when open–drain)			20	μA
Output leakage current low	I_{LOL}	V_{OUT} = 0 V				–3	μA

DC CHARACTERISTICS (Ta = –40 to +85 °C, V_{DD} = 2.7 to 6.0 V) (2/2)

PARAMETER	SYMBOL	TEST CONDITIONS			MIN.	TYP.	MAX.	UNIT
On-chip pull-up resistor	R_{L1}	Ports 0, 1, 2, 3, 6 and 7 (Except P00) V_{IN} = 0 V	V_{DD} = 5.0 V ±10%		15	40	80	kΩ
			V_{DD} = 3.0 V ±10%		30		300	kΩ
	R_{L2}	Ports 4 and 5 V_{OUT} = V_{DD} –2.0 V	V_{DD} = 5.0 V ±10%		15	40	70	kΩ
			V_{DD} = 3.0 V ±10%		10		60	kΩ
LCD drive voltage	V_{LCD}				2.0		V_{DD}	V
LCD split resistor	R_{LCD}				60	100	150	kΩ
LCD output voltage deviation***1** (common)	V_{ODC}	I_O = ±5 μA	V_{LCD0} = V_{LCD} V_{LCD1} = V_{LCD} × 2/3 V_{LCD2} = V_{LCD} × 1/3 2.7 V ≤ V_{LCD} ≤ V_{DD}		0		±0.2	V
LCD output voltage deviation (segment)	V_{ODS}	I_O = ±1 μA			0		±0.2	V
Supply current***2**	I_{DD1}	4.19 MHz***3** crystal oscillation C1 = C2 = 22 pF	V_{DD} = 5 V ±10%***4**			3.0	9	mA
			V_{DD} = 3 V ±10%***5**			0.4	1.2	mA
	I_{DD2}		HALT mode	V_{DD} = 5 V ±10%		600	1800	μA
				V_{DD} = 3 V ±10%		180	540	μA
	I_{DD3}	32 kHz***6** crystal oscillation	V_{DD} = 3 V ±10%			40	120	μA
	I_{DD4}		HALT mode	V_{DD} = 3 V ±10%		12	36	μA
	I_{DD5}	XT1 = 0 V STOP mode	V_{DD} = 5 V ±10%			1	25	μA
			V_{DD} = 3 V ±10%			0.5	15	μA
				Ta = 25 °C		0.5	5	μA

***** **1.** The voltage deviation is the difference between the output voltage and the segment or common output desired value (V_{LCDn} ; n= 0, 1, 2).

2. Current which flows in the on-chip pull-up resistor or LCD split resistor is not included.

3. Including oscillation of the subsystem clock.

4. When the processor clock control register (PCC) is set to 0011 and the device is operated in the high-speed mode.

5. When PCC is set to 0000 and the device is operated in the low-speed mode.

6. When the system clock control register (SCC) is set to 1001 and the device is operated on the subsystem clock, with main system clock oscillation stopped.

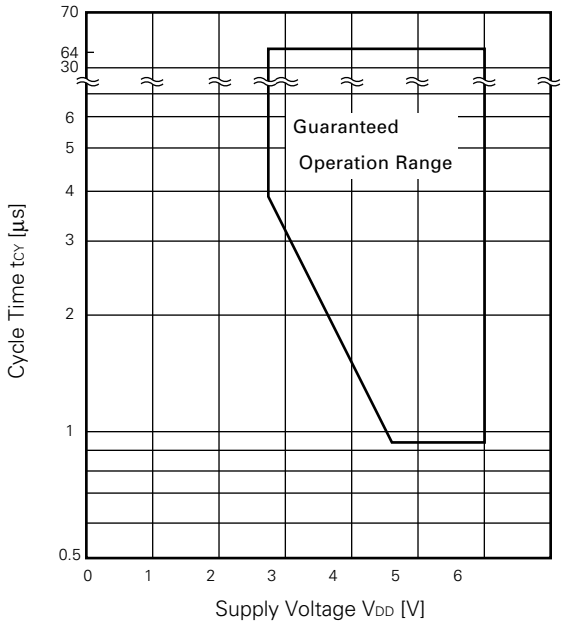
AC CHARACTERISTICS (Ta = –40 to +85 °C, V_{DD} = 2.7 to 6.0 V)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
CPU clock cycle time (minimum instruction execution time)***1**	t_{CY}	Operating on main system clock	V_{DD} = 4.5 to 6.0 V	0.95		64	μs
				3.8		64	μs
		Operating on subsystem clock		114	122	125	μs
TI0 input frequency	f_{TI}	V_{DD} = 4.5 to 6.0 V		0		1	MHz
				0		275	kHz
TI0 input width high/low	t_{TIH}, t_{TIL}	V_{DD} = 4.5 to 6.0 V		0.48			μs
				1.8			μs
Interrupt input width high/low	t_{INTH}, t_{INTL}	INT0		***2**			μs
		INT1, 2, 4		10			μs
		KR0 to KR7		10			μs
$\overline{\text{RESET}}$ width low	t_{RSL}			10			μs

***** **1.** The CPU clock (Φ) cycle time (minimum instruction execution time) is determined by the oscillatior frequency of the connected resonator, the system clock control register (SCC) and the processor clock control register (PCC). The figure at the right indicates the cycle time t_{CY} versus supply voltage V_{DD} characteristic with the main system clock operating.

2. $2t_{CY}$ or $128/f_X$ is set by setting the interrupt mode register (IM0).

t_{CY} vs V_{DD}
(Operating on Main System Clock)



SERIAL TRANSFER OPERATION

2-Wired and 3-Wired Serial I/O Modes ($\overline{SCK}$ ... Internal clock output): (Ta = –40 to +85 °C, V_{DD} = 2.7 to 6.0 V)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
$\overline{SCK}$ cycle time	t_{KCY1}	V_{DD} = 4.5 to 6.0 V		1600			ns
				3800			ns
$\overline{SCK}$ width high/low	t_{KL1}, t_{KH1}	V_{DD} = 4.5 to 6.0 V		t_{KCY1}/2-50			ns
				t_{KCY1}/2-150			ns
SI setup time (to $\overline{SCK}$↑)	t_{SIK1}			150			ns
SI hold time (from $\overline{SCK}$↑)	t_{KSI1}			400			ns
SO output delay time from $\overline{SCK}$↓	t_{KSO1}	R_L = 1 kΩ, C_L = 100 pF*	V_{DD} = 4.5 to 6.0 V			250	ns
						1000	ns

2-Wired and 3-Wired Serial I/O Modes ($\overline{SCK}$ ... External clock input): (Ta = -40 to +85 °C, V_{DD} = 2.7 to 6.0 V)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
$\overline{SCK}$ cycle time	t_{KCY2}	V_{DD} = 4.5 to 6.0 V		800			ns
				3200			ns
$\overline{SCK}$ width high/low	t_{KL2}, t_{KH2}	V_{DD} = 4.5 to 6.0 V		400			ns
				1600			ns
SI setup time (to $\overline{SCK}$↑)	t_{SIK2}			100			ns
SI hold time (from $\overline{SCK}$ ↑)	t_{KSI2}			400			ns
SO output delay time from $\overline{SCK}$↓	t_{KSO2}	R_L = 1 kΩ, C_L = 100 pF*	V_{DD} = 4.5 to 6.0 V			300	ns
						1000	ns

* R_L and C_L are load resistor and load capacitance of the SO output line.

SBI Mode ($\overline{SCK}$ ... Internal clock output (Master)): (Ta = –40 to +85 °C, V_{DD} = 2.7 to 6.0 V)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
$\overline{SCK}$ cycle time	t_{KCY3}	V_{DD} = 4.5 to 6.0 V		1600			ns
				3800			ns
$\overline{SCK}$ width high/low	t_{KL3} t_{KH3}	V_{DD} = 4.5 to 6.0 V		t_{KCY3}/2-50			ns
				t_{KCY3}/2-150			ns
SB0, 1 setup time (to $\overline{SCK}$ ↑)	t_{SIK3}			150			ns
SB0, 1 hold time (from $\overline{SCK}$ ↑)	t_{KSI3}			t_{KCY3}/2			ns
SB0, 1 output delay time from $\overline{SCK}$ ↓	t_{KSO3}	R_L = 1 kΩ, C_L = 100 pF*	V_{DD} = 4.5 to 6.0 V	0		250	ns
				0		1000	ns
SB0, 1 ↓ from $\overline{SCK}$ ↑	t_{KSB}			t_{KCY3}			ns
$\overline{SCK}$ from SB0, 1 ↓	t_{SBK}			t_{KCY3}			ns
SB0, 1 width low	t_{SBL}			t_{KCY3}			ns
SB0, 1 width high	t_{SBH}			t_{KCY3}			ns

SBI Mode ($\overline{SCK}$ ... External clock input (Slave)): (Ta = –40 to +85 °C, V_{DD} = 2.7 to 6.0 V)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
$\overline{SCK}$ cycle time	t_{KCY4}	V_{DD} = 4.5 to 6.0 V		800			ns
				3200			ns
$\overline{SCK}$ width high/low	t_{KL4} t_{KH4}	V_{DD} = 4.5 to 6.0 V		400			ns
				1600			ns
SB0, 1 setup time (to $\overline{SCK}$ ↑)	t_{SIK4}			100			ns
SB0, 1 hold time (from $\overline{SCK}$ ↑)	t_{KSI4}			t_{KCY4}/2			ns
SB0, 1 output delay time from $\overline{SCK}$ ↓	t_{KSO4}	R_L = 1 kΩ, C_L = 100 pF*	V_{DD} = 4.5 to 6.0 V	0		300	ns
				0		1000	ns
SB0, 1 ↓ from $\overline{SCK}$ ↑	t_{KSB}			t_{KCY4}			ns
$\overline{SCK}$ ↓ from SB0, 1 ↓	t_{SBK}			t_{KCY4}			ns
SB0, 1 width low	t_{SBL}			t_{KCY4}			ns
SB0, 1 width high	t_{SBH}			t_{KCY4}			ns

* R_L and C_L are load resistor and load capacitance of the SB0, 1 output lines.

DC CHARACTERISTICS (Ta = –40 to +85 °C, V_{DD} = 2.0 to 6.0 V) (1/2)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Input voltage high	V_{IH1}	Ports 2 and 3		0.8 V_{DD}		V_{DD}	V
	V_{IH2}	Ports 0, 1, 6, 7, $\overline{\text{RESET}}$		0.8 V_{DD}		V_{DD}	V
	V_{IH3}	Ports 4 and 5	On-chip pull-up resistor	0.8 V_{DD}		V_{DD}	V
			Open–drain	0.8 V_{DD}		10	V
	V_{IH4}	X1, X2, XT1		V_{DD} –0.3		V_{DD}	V
Input voltage low	V_{IL1}	Ports 2, 3, 4 and 5		0		0.2 V_{DD}	V
	V_{IL2}	Ports 0, 1, 6, 7, $\overline{\text{RESET}}$		0		0.2 V_{DD}	V
	V_{IL3}	X1, X2, XT1		0		0.3	V
Output voltage high	V_{OH1}	Ports 0, 2, 3, 6, 7, BIAS	I_{OH} = –100 μA	V_{DD} –0.5			V
	V_{OH2}	BP0 to BP7 (with 2 I_{OH} outputs)	I_{OH} = –10 μA	V_{DD} –0.4			V
Output voltage low	V_{OL1}	Ports 0, 2, 3, 4, 5 6, and 7	I_{OL} = 400 μA			0.5	V
		SB0, 1	Open–drain, pull-up resistor ≥ 1 kΩ			0.2 V_{DD}	V
	V_{OL2}	BP0 to BP7 (with 2 I_{OL} outputs)	I_{OL} = 10 μA			0.4	V
Input leakage current high	I_{LIH1}	V_{IN} = V_{DD}	Other than below			3	μA
	I_{LIH2}		X1, X2, XT1			20	μA
	I_{LIH3}	V_{IN} = 10 V	Ports 4 and 5 (with open–drain)			20	μA
Input leakage current low	I_{LIL1}	V_{IN} = 0 V	Other than below			–3	μA
	I_{LIL2}		X1, X2, XT1			–20	μA
Output leakage current high	I_{LOH1}	V_{OUT} = V_{DD}	Other than below			3	μA
	I_{LOH2}	V_{OUT} = 10 V	Ports 4 and 5 (with open–drain)			20	μA
Output leakage current low	I_{LOL}	V_{OUT} = 0 V				–3	μA

DC CHARACTERISTICS (Ta = –40 to +85 °C, V_{DD} = 2.0 to 6.0 V) (2/2)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
On-chip pull-up resistor	R_{L1}	Ports 0, 1, 2, 3, 6 and 7 (Except P00) V_{IN} = 0 V	V_{DD} = 2.5 V ±10%	50		600	kΩ
	R_{L2}	Ports 4 and 5 V_{OUT} = V_{DD} –1.0 V	V_{DD} = 2.5 V ±10%	10		60	kΩ
LCD drive voltage	V_{LCD}			2.0		V_{DD}	V
LCD split resistor	R_{LCD}			60	100	150	kΩ
LCD output voltage deviation ***1** (common)	V_{ODC}	I_O = ±5 μA	V_{LCD0} = V_{LCD} V_{LCD1} = V_{LCD} × 2/3 V_{LCD2} = V_{LCD} × 1/3 2.0 V ≤ V_{LCD} ≤ V_{DD}	0		±0.2	V
LCD output voltage deviation (segment)	V_{ODS}	I_O = ±1 μA		0		±0.2	V
Supply current***2**	I_{DD1}	4.19 MHz***3** crystal oscillation C1 = C2 = 22 pF low-speed mode	V_{DD} = 3 V ±10%***4**		0.4	1.2	mA
			V_{DD} = 2.5 V ±10%***4**		0.3	0.9	mA
	I_{DD2}		HALT mode: V_{DD} = 3 V ±10%		180	540	μA
			HALT mode: V_{DD} = 2.5 V ±10%		120	360	μA
	I_{DD3}	32 kHz***5** crystal oscillation	V_{DD} = 3 V ±10%		40	120	μA
			V_{DD} = 2.5 V ±10%		25	75	μA
	I_{DD4}		HALT mode: V_{DD} = 3 V ±10%		12	36	μA
			HALT mode: V_{DD} = 2.5 V ±10%		9	27	μA
	I_{DD5}	XT1 = 0 V STOP mode	V_{DD} = 3 V ±10%		0.5	15	μA
			V_{DD} = 3 V ±10%, Ta = 25 °C		0.5	5	μA
			V_{DD} = 2.5 V ±10%		0.4	15	μA
			V_{DD} = 2.5 V ±10%, Ta = 25°C		0.4	5	μA

***** **1.** The voltage deviation is the difference between the output voltage and the segment or common output desired value (V_{LCDn}; n = 0, 1, 2).

2. Current which flows in the on-chip pull-up resistor or LCD split resistor is not included.

3. Including oscillation of the subsystem clock.

4. When PCC is set to 0000 and the device is operated in the low-speed mode.

5. When the system clock control register (SCC) is set to 1001 and the device is operated on the subsystem clock, with main system clock oscillation stopped.

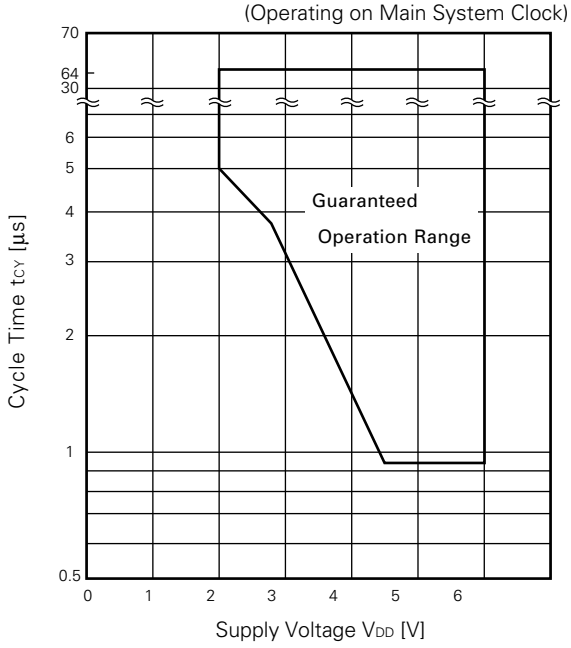
AC CHARACTERISTICS (Ta = –40 to +85 °C, V_{DD} = 2.0 to 6.0 V)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
CPU clock cycle time (minimum instruction execution time)***1**	t_{CY}	Operation on main system clock	V_{DD} = 2.7 to 6.0 V	3.8		64	μs
			V_{DD} = 2.0 to 6.0 V	5		64	μs
			Ta = –40 to + 60 °C V_{DD} = 2.2 to 6.0 V	3.4		64	μs
		Operation on subsystem clock		114	122	125	μs
TI0 input frequency	f_{TI}			0		275	kHz
TI0 input width high/low	t_{TIH}, t_{TIL}			1.8			μs
Interrupt input width high/low	t_{INTH}, t_{INTL}	INT0		***2**			μs
		INT1, 2, 4		10			μs
		KR0 to KR7		10			μs
$\overline{\text{RESET}}$ width low	t_{RSL}			10			μs

***** **1.** The CPU clock (Φ) cycle time (minimum instruction execution time) is determined by the oscillatior frequency of the connected resonator, the system clock control register (SCC) and the processor clock control register (PCC). The figure at the right indicates the cycle time t_{CY} versus supply voltage V_{DD} characteristic with the main system clock operating.

2. $2t_{CY}$ or $128/f_X$ is set by setting the interrupt mode register (IM0).

t_{CY} vs V_{DD}
(Operating on Main System Clock)



SERIAL TRANSFER OPERATION

2-Wired and 3-Wired Serial I/O Mode ($\overline{SCK}$ ... Internal clock output): (Ta = –40 to +85 °C, V_{DD} = 2.0 to 6.0 V)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
$\overline{SCK}$ cycle time	t_{KCY1}	V_{DD} = 4.5 to 6.0 V		1600			ns
				3800			ns
$\overline{SCK}$ width high/low	t_{KL1}, t_{KH1}	V_{DD} = 4.5 to 6.0 V		t_{KCY1}/2-50			ns
				t_{KCY1}/2-150			ns
SI setup time (to $\overline{SCK}$ ↑)	t_{SIK1}			250			ns
SI hold time (from $\overline{SCK}$ ↑)	t_{KSI1}			400			ns
SO output delay time from $\overline{SCK}$ ↓	t_{KSO1}	R_L = 1 kΩ, C_L = 100 pF*	V_{DD} = 4.5 to 6.0 V			250	ns
						1000	ns

2-Wired and 3-Wired Serial I/O Mode ($\overline{SCK}$ ... External clock input): (Ta = –40 to +85 °C, V_{DD} = 2.0 to 6.0 V)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
$\overline{SCK}$ cycle time	t_{KCY2}	V_{DD} = 4.5 to 6.0 V		800			ns
				3200			ns
$\overline{SCK}$ width high/low	t_{KL2}, t_{KH2}	V_{DD} = 4.5 to 6.0 V		400			ns
				1600			ns
SI setup time (to $\overline{SCK}$↑)	t_{SIK2}			100			ns
SI hold time (from $\overline{SCK}$↑)	t_{KSI2}			400			ns
SO output delay time from $\overline{SCK}$↓	t_{KSO2}	R_L = 1 kΩ, C_L = 100 pF*	V_{DD} = 4.5 to 6.0 V			300	ns
						1000	ns

* R_L and C_L are load resistor and load capacitance of the SO output line.

SBI Mode ($\overline{SCK}$ ... Internal clock output (Master)): (Ta = –40 to +85 °C, V_{DD} = 2.0 to 6.0 V)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
$\overline{SCK}$ cycle time	t_{KCY3}	V_{DD} = 4.5 to 6.0 V		1600			ns
				3800			ns
$\overline{SCK}$ width high/low	t_{KL3} t_{KH3}	V_{DD} = 4.5 to 6.0 V		t_{KCY3}/2-50			ns
				t_{KCY3}/2-150			ns
SB0, 1 setup time (to $\overline{SCK}$↑)	t_{SIK3}			250			ns
SB0, 1 hold time (from $\overline{SCK}$↑)	t_{KSI3}			t_{KCY3}/2			ns
SB0, 1 output delay time from $\overline{SCK}$↓	t_{KSO3}	R_L = 1 kΩ, C_L = 100 pF*	V_{DD} = 4.5 to 6.0 V	0		250	ns
				0		1000	ns
SB0, 1 ↓ from $\overline{SCK}$↑	t_{KSB}			t_{KCY3}			ns
$\overline{SCK}$ from SB0, 1 ↓	t_{SBK}			t_{KCY3}			ns
SB0, 1 width low	t_{SBL}			t_{KCY3}			ns
SB0, 1 width high	t_{SBH}			t_{KCY3}			ns

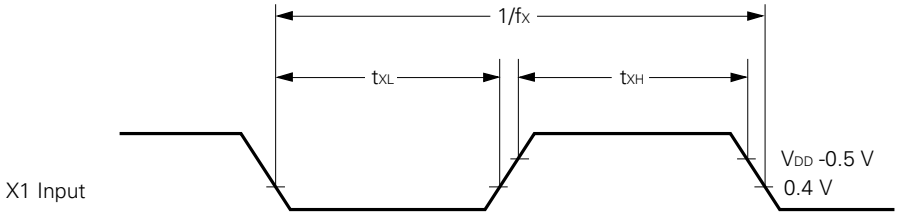
SBI Mode ($\overline{SCK}$ ... External clock input (Slave)): (Ta = –40 to +85 °C, V_{DD} = 2.0 to 6.0 V)

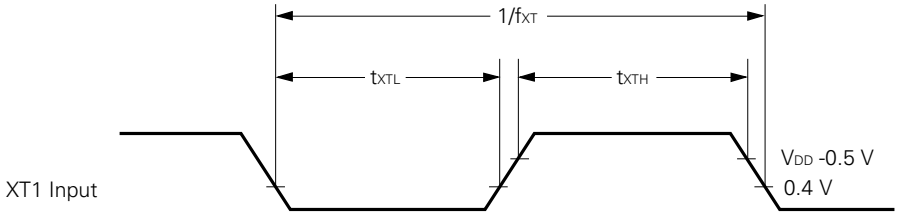
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
$\overline{SCK}$ cycle time	t_{KCY4}	V_{DD} = 4.5 to 6.0 V		800			ns
				3200			ns
$\overline{SCK}$ width high/low	t_{KL4} t_{KH4}	V_{DD} = 4.5 to 6.0 V		400			ns
				1600			ns
SB0, 1 setup time (to $\overline{SCK}$ ↑)	t_{SIK4}			100			ns
SB0, 1 hold time (from $\overline{SCK}$ ↑)	t_{KSI4}			t_{KCY4}/2			ns
SB0, 1 output delay time from $\overline{SCK}$ ↓	t_{KSO4}	R_L = 1 kΩ, C_L = 100 pF*	V_{DD} = 4.5 to 6.0 V	0		300	ns
				0		1000	ns
SB0, 1 ↓ from $\overline{SCK}$ ↑	t_{KSB}			t_{KCY4}			ns
$\overline{SCK}$↓ from SB0, 1 ↓	t_{SBK}			t_{KCY4}			ns
SB0, 1 width low	t_{SBL}			t_{KCY4}			ns
SB0, 1 width high	t_{SBH}			t_{KCY4}			ns

* R_L and C_L are load resistor and load capacitance of the SB0, 1 output lines.

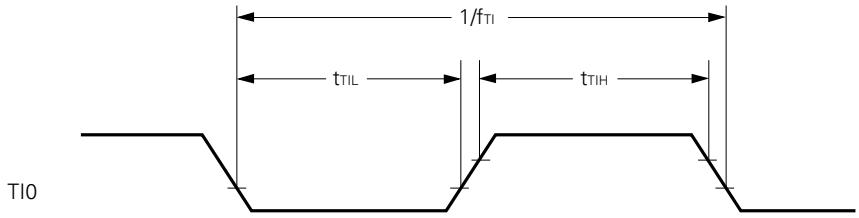
AC Timing Test Point (Excluding X1 and XT1 inputs)

Clock Timings



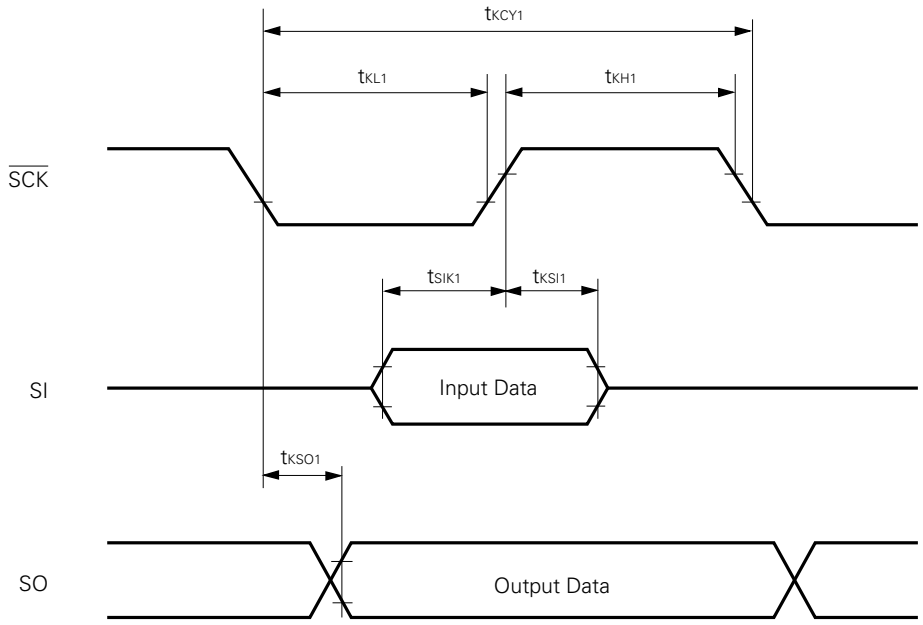


TI0 Timing

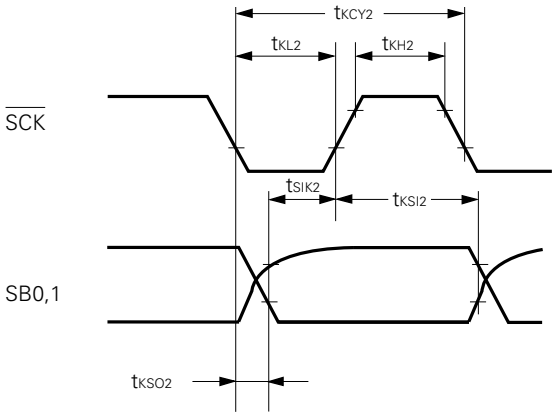


Serial Transfer Timing

3-wired serial I/O mode:

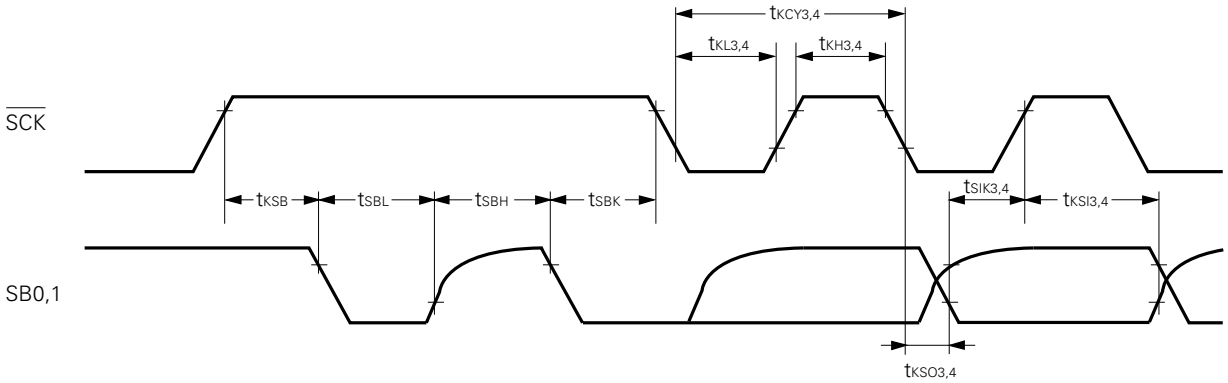


2-wired serial I/O mode:

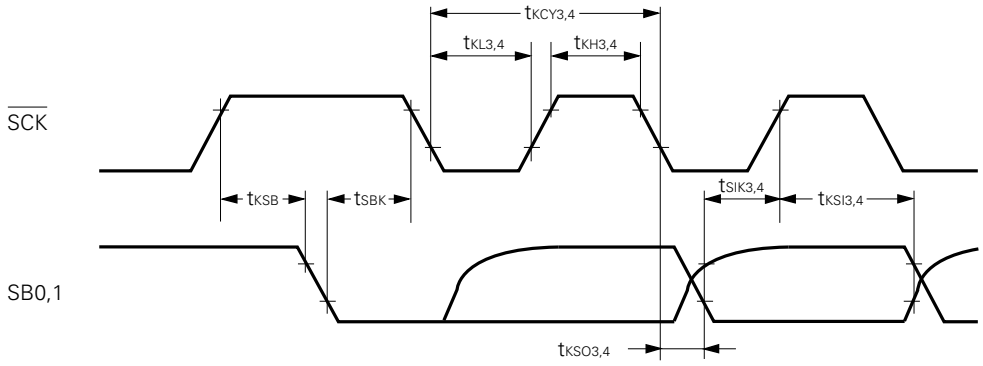


Serial Transfer Timing

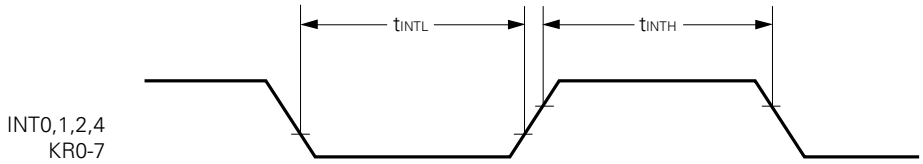
Bus release signal transfer:



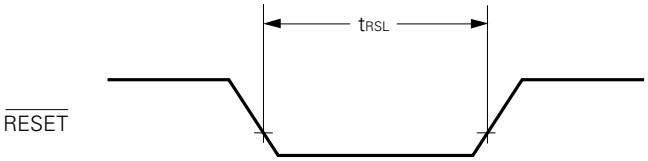
Command signal transfer:



Interrupt Input Timing



$\overline{\text{RESET}}$ Input Timing



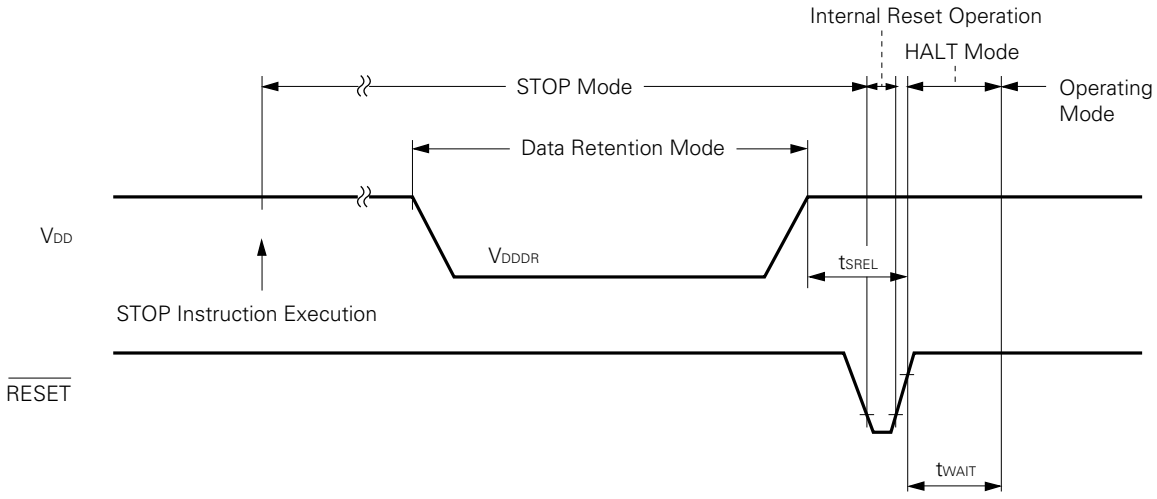
DATA MEMORY STOP MODE LOW SUPPLY VOLTAGE DATA RETENTION CHARACTERISTICS (Ta = –40 to 85 °C)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Data retention supply voltage	V_{DDDR}		2.0		6.0	V
Data retention supply current*1	I_{DDDR}	V_{DDDR} = 2.0 V		0.3	15	μA
Release signal setup time	t_{SREL}		0			μs
Oscillation stabilization wait time*2	t_{WAIT}	Release by $\overline{\text{RESET}}$		2^{17}/fx		ms
		Release by interrupt request		*3		ms

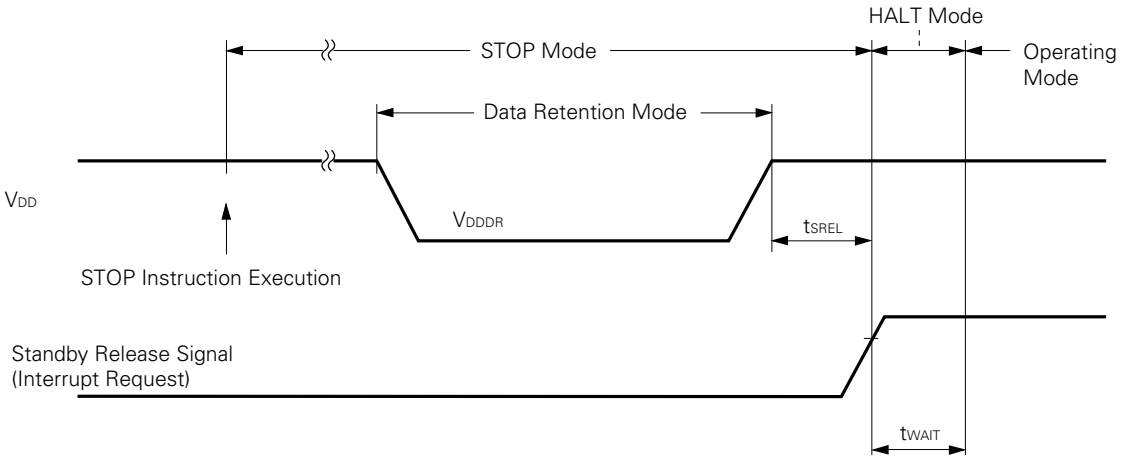
* **1.** Current which flows in the on-chip pull-up resistor is not included.
2. The oscillation stabilization wait time is the time during which the CPU operation is stopped to prevent unstable operation at the oscillation start.
3. Depends on the basic interval timer mode register (BTM) setting (table below).

BTM3	BTM2	BTM1	BTM0	WAIT TIME (Figures in parentheses are for operation at fx = 4.19 MHz)
—	0	0	0	2^{20}/fx (approx. 250 ms)
—	0	1	1	2^{17}/fx (approx. 31.3 ms)
—	1	0	1	2^{15}/fx (approx. 7.82 ms)
—	1	1	1	2^{13}/fx (approx. 1.95 ms)

Data Retention Timing (STOP mode release by $\overline{\text{RESET}}$)

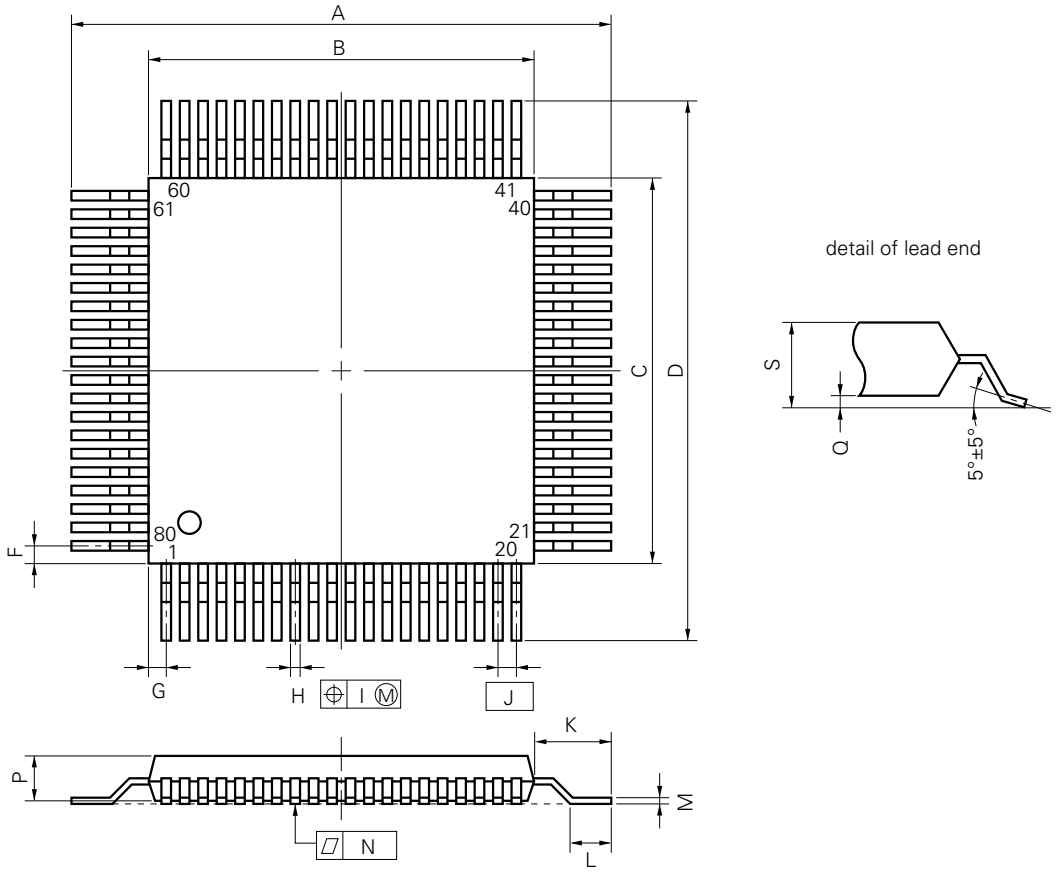


Data Retention Timing (Standby release signal: STOP mode release by interrupt signal)



12. PACKAGE INFORMATION

80 PIN PLASTIC QFP (□14)



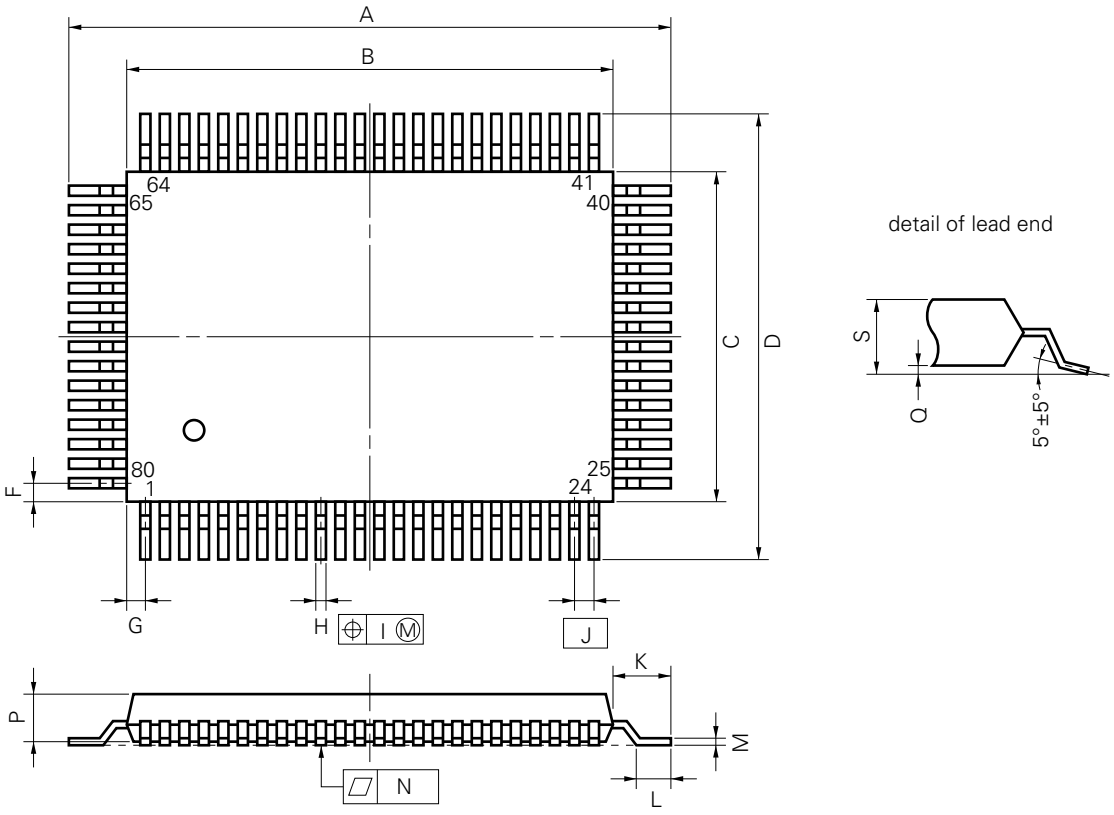
S80GC-65-3B9-3

NOTE

Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	17.2±0.4	0.677±0.016
B	14.0±0.2	$0.551^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.2±0.4	0.677±0.016
F	0.8	0.031
G	0.8	0.031
H	0.30±0.10	$0.012^{+0.004}_{-0.005}$
I	0.13	0.005
J	0.65 (T.P.)	0.026 (T.P.)
K	1.6±0.2	0.063±0.008
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.10	0.004
P	2.7	0.106
Q	0.1±0.1	0.004±0.004
S	3.0 MAX.	0.119 MAX.

80 PIN PLASTIC QFP (14×20)



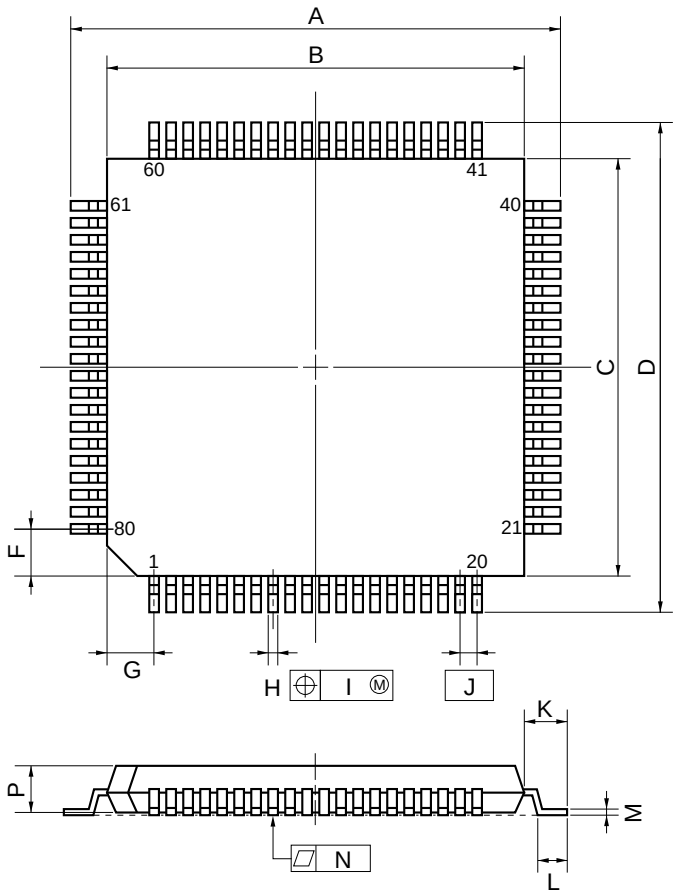
P80GF-80-3B9-2

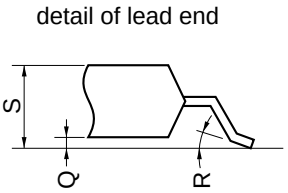
NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	23.6±0.4	0.929±0.016
B	20.0±0.2	$0.795^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.6±0.4	0.693±0.016
F	1.0	0.039
G	0.8	0.031
H	0.35±0.10	$0.014^{+0.004}_{-0.005}$
I	0.15	0.006
J	0.8 (T.P.)	0.031 (T.P.)
K	1.8±0.2	$0.071^{+0.008}_{-0.009}$
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.15	0.006
P	2.7	0.106
Q	0.1±0.1	0.004±0.004
S	3.0 MAX.	0.119 MAX.

80 PIN PLASTIC TQFP (FINE PITCH) (□12)





NOTE

Each lead centerline is located within 0.10 mm (0.004 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	14.0±0.2	$0.551^{+0.009}_{-0.008}$
B	12.0±0.2	$0.472^{+0.009}_{-0.008}$
C	12.0±0.2	$0.472^{+0.009}_{-0.008}$
D	14.0±0.2	$0.551^{+0.009}_{-0.008}$
F	1.25	0.049
G	1.25	0.049
H	$0.22^{+0.05}_{-0.04}$	0.009±0.002
I	0.10	0.004
J	0.5 (T.P.)	0.020 (T.P.)
K	1.0±0.2	$0.039^{+0.009}_{-0.008}$
L	0.5±0.2	$0.020^{+0.008}_{-0.009}$
M	$0.145^{+0.055}_{-0.045}$	0.006±0.002
N	0.10	0.004
P	1.05	0.041
Q	0.05±0.05	0.002±0.002
R	5°±5°	5°±5°
S	1.27 MAX.	0.050 MAX.

P80GK-50-BE9-4

13. RECOMMENDED SOLDERING CONDITIONS ★

These products should be soldered and mounted under the conditions recommended below.

For details of recommended soldering conditions, refer to the information document **"Surface Mount Technology Manual (IEI 1207)"**.

For soldering methods and conditions other than those recommended, please contact our salesman.

Table 13-1 Surface Mount Type Soldering Conditions

(1) μPD75304BGC-×××-3B9: 80-Pin Plastic QFP (□14 mm)
μPD75306BGC-×××-3B9: 80-Pin Plastic QFP (□14 mm)
μPD75308BGC-×××-3B9: 80-Pin Plastic QFP (□14 mm)

Soldering Method	Soldering ConditionsRecommended	Condition Symbol
Infrared reflow	Package peak temperature: 230°C Duration: 30 sec. max. (210°C or above) Number of applications: one Time limit: 7 days* (thereafter 20 hours 125°C prebaking required)	IR30-207-1
VPS	Package peak temperature: 215°C Duration: 40 sec. max. (200°C or above) Number of applications: one Time limit: 7 days* (thereafter 20 hours 125°C prebaking required)	VP15-207-1
Pin part heating	Pin part temperature: 300°C or less Duration: 3 sec. max. (per side of device)	—

(2) μPD75304BGF-×××-3B9: 80-Pin Plastic QFP (14 × 20 mm)
μPD75306BGF-×××-3B9: 80-Pin Plastic QFP (14 × 20 mm)
μPD75308BGF-×××-3B9: 80-Pin Plastic QFP (14 × 20 mm)

Soldering Method	Soldering ConditionsRecommended	Condition Symbol
Infrared reflow	Package peak temperature: 230°C Duration: 30 sec. max. (210°C or above) Number of applications: one	IR30-00-1
VPS	Package peak temperature: 215°C Duration: 40 sec. max. (200°C or above) Number of applications: one	VP15-00-1
Wave soldering	Solder bath temperature: 260°C or less Duration: 10 sec. max. Number of applications: one Preparatory heating temperature: 120°C max. (package surface temperature)	WS60-00-1
Pin part heating	Pin part temperature: 300°C or less Duration: 3 sec. max. (per side of device)	—

***** For the storage period after dry-pack decapsulation, storage conditions are max. 25°C, 65% RH.

Note Use of more than one soldering method should be avoided (except in the case of pin part heating).

(3) μPD75304BGK-×××-3B9: 80-Pin Plastic TQFP (□12 mm)
μPD75306BGK-×××-3B9: 80-Pin Plastic TQFP (□12 mm)
μPD75308BGK-×××-3B9: 80-Pin Plastic TQFP (□12 mm)

Soldering Method	Soldering ConditionsRecommended	Condition Symbol
Infrared reflow	Package peak temperature: 230°C Duration: 30 sec. max. (210°C or above) Number of applications: one Time limit: 1 day* (thereafter 16 hours 125°C prebaking required)	IR30-161-1
VPS	Package peak temperature: 215°C Duration: 40 sec. max. (200°C or above) Number of applications: one Time limit: 1 day* (thereafter 16 hours 125°C prebaking required)	VP15-161-1
Pin part heating	Pin part temperature: 300°C or less Duration: 3 sec. max. (per side of device)	—

* For the storage period after dry-pack decapsulation, storage conditions are max. 25°C, 65% RH.

Note Use of more than one soldering method should be avoided (except in the case of pin part heating).

NOTICE

Recommended soldering conditions have been improved for some of these products.
(Improvements: Relaxation of infrared reflow peak temperature (235°C, number of applications (two), time limit, etc.)
Please contact your NEC sales representative for details.

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★ APPENDIX A. DIFFERENCES AMONG SERIES PRODUCTS

Item \ Product Name		μPD75304/75306/75308		μPD75312/75316	μPD75P308	μPD75P316
Supply voltage range		2.0 to 6.0 V			5V±5%	
ROM configuration		Mask ROM			EPROM/One-time	One-time PROM
Program memory (bytes)		4096/6016/8064		12160/16256	8064	16256
Data memory (× 4 bits)		512				
Instruction cycle		0.95 μs, 1.91 μs, 15.3 μs (main system clock: 4.19 MHz operation) 122 μs (subsystem clock: 32.768 kHz operation)				
Input/output ports	CMOS input	40	8	Pull-up resistor incorporation spesifiable by software: 23		
	CMOS input/output		16			
	CMOS output		8	Used with segment pin		
	N-ch open–drain input/output		8	10 V withstand voltage. Pull-up resistor incorporation spesifiable by mask option	10 V withstand voltage. Pull-up resistor incorporation spesifiable by mask option. (without pull-up resistor)	
LCD controller/driver		• Common output: Static – 1/4 duty selected • Segment output: Max. 32				
		LCD drive split resistor can be incorporated by mask option.			No LCD drive split resistor.	
LCD drive voltage		2.0 to V_{DD}				
Timer/counter		• 8-bit timer/event counter • 8-bit basic interval timer • Watch timer				
Serial interface		• NEC standard serial bus interface (SBI) • Clock synchronous serial interface				
Vectored interrupt		• External: 3 • Internal: 3				
Test input		• External: 1 • Internal: 1				
Clock output (PCL)		Φ, 524 kHz, 262 kHz, 65.5 kHz (main system clock: 4.19 MHz operation)				
Buzzer output (BUZ)		2 kHz (Main system clock: in 4.19 MHz operation or subsystem clock: in 32.768 kHz operation)				
Package		80-pin plastic QFP (14 × 20 mm)			80-pin plastic QFP (14 × 20 mm) 80-pin ceramic WQFN (LCC with window)	80-pin plastic QFP (14 × 20 mm)
On-chip PROM product		μPD75P308		μPD75P316 μPD75P316A	—	—

Item \ Product Name	μPD75304B/75306B/75308B	μPD75312B	μPD75316B	μPD75P316B*	μPD75P316A
Supply voltage range	2.0 to 6.0 V				
ROM configuration	Mask ROM			One-time PROM	EPROM/One-time
Program memory (bytes)	4096/6016/8064	12160	16256		
Data memory (× 4 bits)	512	1024			
Instruction cycle	0.95 μs, 1.91 μs, 15.3 μs (main system clock: 4.19 MHz operation) 122 μs (subsystem clock: 32.768 kHz operation)				
Input/output ports: CMOS input	40	8	Pull-up resistor incorporation spesifiable by software: 23		
Input/output ports: CMOS input/output		16			
Input/output ports: CMOS output		8	Used with segment pin		
Input/output ports: N-ch open–drain input/output		8	10 V withstand voltage. Pull-up resistor incorporation spesifiable by mask option	10 V withstand voltage. Pull-up resistor incorporation spesifiable by mask option. (without pull-up resistor)	
LCD controller/driver	• Common output: Static – 1/4 duty selected • Segment output: Max. 32				
	LCD drive split resistor can be incorporated by mask option.		No LCD drive split resistor.		
LCD drive voltage	2.0 to V_{DD}				
Timer/counter	• 8-bit timer/event counter • 8-bit basic interval timer • Watch timer				
Serial interface	• NEC standard serial bus interface (SBI) • Clock synchronous serial interface				
Vectored interrupt	• External: 3 • Internal: 3				
Test input	• External: 1 • Internal: 1				
Clock output (PCL)	Φ, 524 kHz, 262 kHz, 65.5 kHz (main system clock: 4.19 MHz operation)				
Buzzer output (BUZ)	2 kHz (Main system clock: in 4.19 MHz operation or subsystem clock: in 32.768 kHz operation)				
Package	80-pin plastic QFP • (14 × 20 mm) • (□14mm) 80-pin plastic TQFP(□12mm)	80-pin plastic QFP (□14mm) 80-pin plastic TQFP(□12mm)			80-pin ceramic WQFN 80-pin plastic QFP (14 × 20 mm)
On-chip PROM product	GF package: μPD75P316A GC/GK package: μPD75P316B	μPD75P316B		—	—

* Under development

APPENDIX B. DEVELOPMENT TOOLS

The following development tools are available for system development using the μPD75304B/75306B/75308B.

Hardware	IE-75000-R***1** IE-75001-R		75X series in-circuit emulator
	IE-75000-R-EM***2**		Emulation board for the IE-75000-R or IE-75001-R
	EP-75308GF-R	EV-9200G-80	Emulation probe for the μPD75304BGF, 75306BGF and 75308BGF. An 80-pin conversion socket (EV-9200G-80) is also provided.
	EP-75308BGC-R	EV-9200GC-80	Emulation probe for the μPD75304BGC, 75306BGC and 75308BGC. An 80-pin conversion socket (EV-9200GC-80) is also provided.
	EP-75308BGK-R	EV-9500GK-80	Emulation probe for the μPD75304BGK, 75306BGK and 75308BGK. An 80-pin conversion adapter (EV-9200GK-80) is also provided.
	PG-1500		PROM programmer
	PA-75P308GF		PROM programmer adapter for the μPD75P316AGF, connected to the PG-1500.
	PA-75P316BGC		PROM programmer adapter for the μPD75P316BGC, connected to the PG-1500.
	PA-75P316BGK		PROM programmer adapter for the μPD75P316BGK, connected to the PG-1500.
Software	IE Control Program		Host machines PC-9800 series (MS-DOS™ Ver. 3.30 to Ver. 5.00A***3**) IBM PC/AT™(PC DOS™ Ver. 3.1)
	PG-1500 Controller		
	RA75X Relocatable Assembler		

* **1.** Maintenance product
2. Not incorporated in the IE-75001-R.
3. A task swapping function is provided in Ver. 5.00/5.00A, but this function cannot be used with this software.

Remarks Please refer to the 75X Series Selection Guide (IF-151) for third party development tools.

APPENDIX C. RELATED DOCUMENTS

Device Related Documents

Document Name	Document Number
User's Manual	IEM-5016
Instruction Application Table	IEM-994
Application Note	IEM-5035
	IEM-5041
75X Series Selection Guide	IF-151

Development Tools Documents

	Document Name		Document Number
Hardware	IE-75000-R/IE-75001-R User's Manual		EEU-846
	IE-75000-R-EM User's Manual		EEU-673
	EP-75308GF-R User's Manual		EEU-689
	EP-75308BGC-R User's Manual		EEU-825
	EP-75308BGK-R User's Manual		EEU-838
	PG-1500 User's Manual		EEU-651
Software	RA75X Assembler Package User's Manual	Operation	EEU-731
		Language	EEU-730
	PG-1500 Controller User's Manual		EEU-704

Other Documents

Document Name	Document Number
Package Manual	IEI-635
Surface Mount Technology Manual	IEI-1207
Quality Grande on NEC Semiconductor Device	IEI-1209
NEC Semiconductor Device Reliability & Quality Control	IEM-5068
Electrostatic Discharge(ESD) Test	MEM-539
Semiconductor Devices Quality Guarantee Guide	MEI-603
Microcomputer Related Products Guide Other Manufacturers Volume	MEI-604

* The contents of the above related documents are subject to change without notice. The latest documents should be used for design, etc.

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