

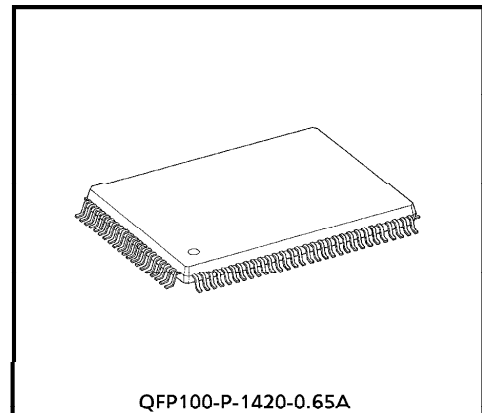
TENTATIVE TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

# TC9432F

## DIGITAL SERVO SINGLE CHIP PROCESSOR BUILT IN 1 BIT DA CONVERTER

The TC9432F is a single chip processor which incorporates the following function : synchronous separation protection and interpolation, EFM demodulation, Error correction, microcontroller interface, digital equalizer for use in servo LSI and servo control circuit.

In addition, the TC9432F incorporates a 1 bit DA converter. In combination with the head amplifier TA2109F for digital servo, the TC9432F allow simplified, adjustment-free structuring of CD player system.



QFP100-P-1420-0.65A

Weight : 1.6g (Typ.)

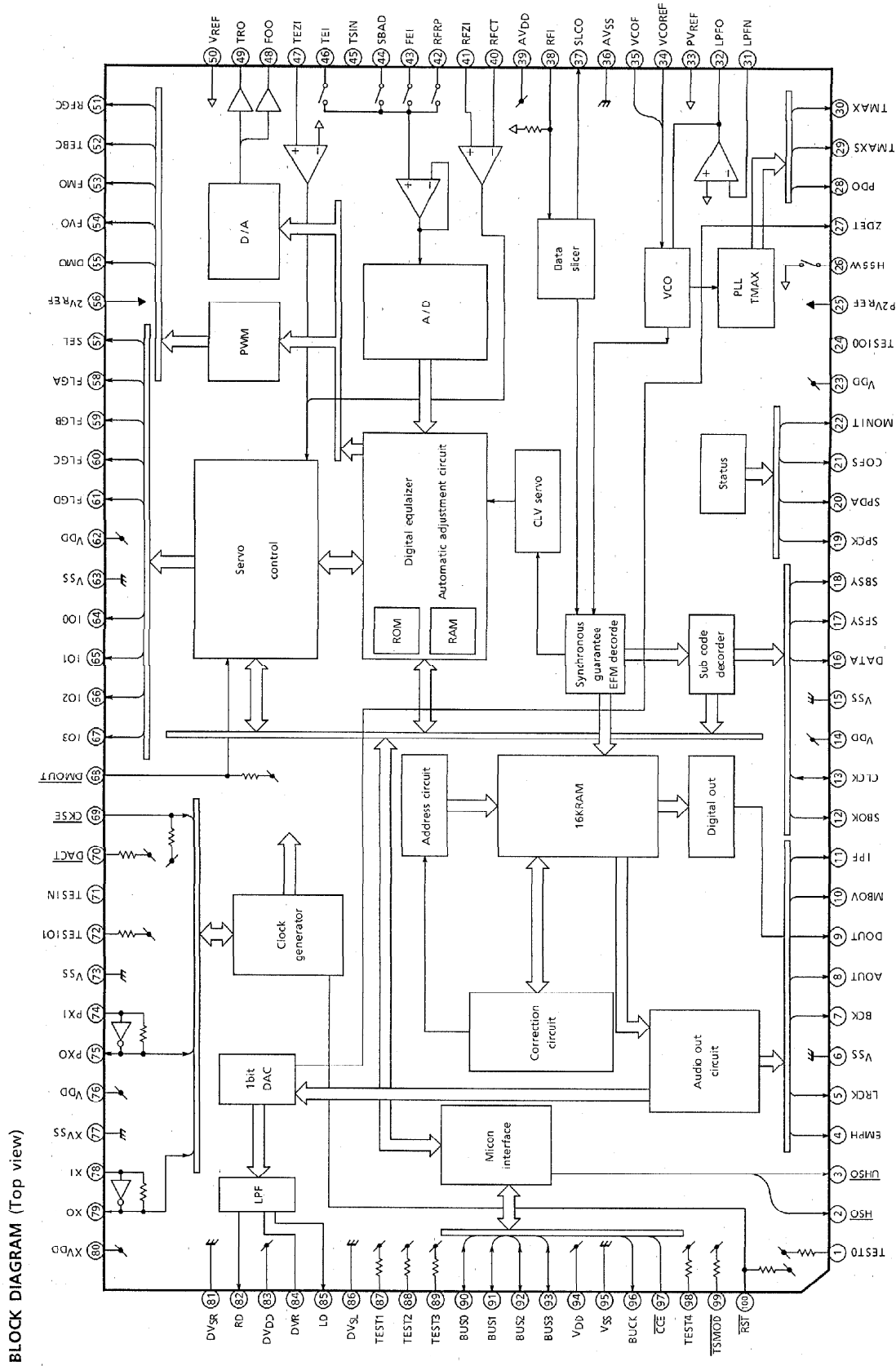
### FEATURES

- Sync pattern detection, sync signal protection and synchronization can be made correctly.
- Built in EFM demodulation circuit, subcode demodulation circuit.
- Capable of correcting dual C1 correction and quadruple C2 correction using the CIRC correction theoretical format.
- The TC9432F respond to variable playback system.
- Jitter absorbing capacity of  $\pm 6$  frames.
- Built in 16KRAM.
- Built in digital out circuit.
- Built in L/R independent digital attenuator.
- Audio output responds to bilingual function.
- Reed timing free subcode Q data and capable of synchronous output with audio data.

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- Built in data slicer and analog PLL (free-adjustment VCO).
- Capable of automatic adjustment function of focus servo and tracking servo, for loop gain, offset and balance.
- Built in RF gain automatic adjustment circuit.
- Built in digital equalizer for phase compensation.
- Built in RAM for digital equalizer for coefficient, and capable of variable pickup.
- Built in focus, tracking servo control circuit.
- Search control corresponds to every mode and can realize high speed and stable search.
- Lens-kick are using speed controlled form.
- Built in AFC circuit and APC circuit for CLV servo of disc motor.
- Built in anti-defect and anti-shock circuit.
- Built in 8 times oversampling 1bit DA converter.
- Built in analog filter for 1bit DA converter.
- Built in zero data detect output circuit.
- The TC9432F capable of 4 times speed operation.
- Built in microcontroller interface circuit.
- CMOS silicon structure and high speed, low power consumption.
- 100 pin flat package.



**PIN FUNCTION**

PIN No.	SYMBOL	I/O	FUNCTIONAL DESCRIPTION	REMARKS															
1	TEST0	I	Test mode terminal. Normally, keep at open.	With pull-up resistor.															
2	$\overline{\text{HSO}}$	O	Playback speed mode flag output terminal. <table border="1" style="margin: 10px auto;"> <thead> <tr> <th><math>\overline{\text{UHSO}}</math></th> <th><math>\overline{\text{HSO}}</math></th> <th>PLAYBACK SPEED</th> </tr> </thead> <tbody> <tr> <td>H</td> <td>H</td> <td>Nomal</td> </tr> <tr> <td>H</td> <td>L</td> <td>2 times</td> </tr> <tr> <td>L</td> <td>H</td> <td>4 times</td> </tr> <tr> <td>L</td> <td>L</td> <td>—</td> </tr> </tbody> </table>	$\overline{\text{UHSO}}$	$\overline{\text{HSO}}$	PLAYBACK SPEED	H	H	Nomal	H	L	2 times	L	H	4 times	L	L	—	—
$\overline{\text{UHSO}}$	$\overline{\text{HSO}}$	PLAYBACK SPEED																	
H	H	Nomal																	
H	L	2 times																	
L	H	4 times																	
L	L	—																	
3	$\overline{\text{UHSO}}$	O																	
4	EMPH	O	Subcode Q data emphasis flag output terminal. Emphasis ON at "H" level and OFF at "L" level. The output polarity can invert by command.	—															
5	LRCK	O	Channel clock output terminal. (44.1kHz) L-ch at "L" level and R-ch at "H" level. The output polarity can invert by command.	—															
6	V <sub>SS</sub>	—	Digital GND terminal.	—															
7	BCK	O	Bit clock output terminal. (1.4122MHz)	—															
8	AOUT	O	Audio data output terminal.	—															
9	DOUT	O	Digital data output terminal.	—															
10	MBOV	O	Buffer memory over signal output terminal. Over at "H" level.	—															
11	IPF	O	Correction flag output terminal. At "H" level, AOUT output is made to correction impossibility by C <sub>2</sub> correction processing.	—															
12	SBOK	O	Subcode Q data CRCC check adjusting result output terminal. The adjusting result is OK at "H" level.	—															
13	CLCK	I/O	Subcode P~W data readout clock input/output terminal. This terminal can select by command bit.	—															
14	V <sub>DD</sub>	—	Digital power supply voltage terminal.	—															
15	V <sub>SS</sub>	—	Digital GND terminal.	—															
16	DATA	O	Subcode P~W data output terminal.	—															
17	SFSY	O	Play-back frame sync signal output terminal.	—															
18	SBSY	O	Subcode block sync signal output terminal.	—															
19	SPCK	O	Processor status signal readout clock output terminal.	—															
20	SPDA	O	Processor status signal output terminal.	—															
21	COFS	O	Correction frame clock output terminal. (7.35kHz)	—															
22	MONIT	O	Internal signal (DSP internal flag and PLL clock) output terminal. Selected by command.	—															
23	V <sub>DD</sub>	—	Digital power supply voltage terminal.	—															

PIN No.	SYMBOL	I/O	FUNCTIONAL DESCRIPTION	REMARKS								
24	TESIO0	I	Test input/output terminal. Normally, keep at "L" level.	—								
25	P2VREF	—	PLL double reference voltage supply terminal.	—								
26	HSSW	O	2/4 times speed at "VREF" voltage.	2-state output. (PVREF, HiZ)								
27	ZDET	O	1bit DA converter zero detect flag output terminal.	—								
28	PDO	O	Phase difference signal output terminal of EFM signal and PLCK signal.	3-state output. (P2VREF, PVREF, VSS)								
29	TMAXS	O	TMAX detection result output terminal. Selected by command bit (TMPS).	3-state output. (P2VREF, PVREF, VSS)								
30	TMAX	O	TMAX detection result output terminal. Selected by command bit (TMPS). <table border="1" style="margin: 10px auto; border-collapse: collapse;"> <thead> <tr> <th>DIFFERENCE RESULT</th> <th>TMAX OUTPUT</th> </tr> </thead> <tbody> <tr> <td>Longer than fixed freq.</td> <td>"P2VREF"</td> </tr> <tr> <td>Shorter than fixed freq.</td> <td>"VSS"</td> </tr> <tr> <td>Within the fixed freq.</td> <td>"HiZ"</td> </tr> </tbody> </table>	DIFFERENCE RESULT	TMAX OUTPUT	Longer than fixed freq.	"P2VREF"	Shorter than fixed freq.	"VSS"	Within the fixed freq.	"HiZ"	3-state output. (P2VREF, HiZ, VSS)
DIFFERENCE RESULT	TMAX OUTPUT											
Longer than fixed freq.	"P2VREF"											
Shorter than fixed freq.	"VSS"											
Within the fixed freq.	"HiZ"											
31	LPFN	I	LPF amplifier inverting input terminal for PLL.	Analog input.								
32	LPFO	O	LPF amplifier output terminal for PLL.	Analog output.								
33	PVREF	—	PLL reference voltage supply terminal.	—								
34	VCOREF	I	VCO center frequency reference level terminal. Normally, keep at "PVREF" level.	—								
35	VCOF	O	VCO filter terminal.	Analog output.								
36	AVSS	—	Analog GND terminal.	—								
37	SLCO	O	Data slice level output terminal.	Analog output.								
38	RFI	I	RF signal input terminal.	Analog input. (Z <sub>in</sub> : selected by command)								
39	AVDD	—	Analog power supply voltage terminal.	—								
40	RFCT	I	RFRP signal center level input terminal.	Analog input. (Z <sub>in</sub> : 50kΩ)								
41	RFZI	I	RFRP zero cross input terminal.	Analog input.								
42	RFRP	I	RF ripple signal input terminal.	Analog input.								
43	FEI	I	Focus error signal input terminal.	Analog input.								
44	SBAD	I	Sub-beam adder signal input terminal.	Analog input.								
45	TSIN	I	Test input terminal. Normally, keep at "VREF" level.	Analog input.								
46	TEI	I	Tracking error signal input terminal. Take in at tracking servo on.	Analog input.								
47	TEZI	I	Tracking error zero cross input terminal.	Analog input. (Z <sub>in</sub> : 10kΩ)								
48	FOO	O	Focus servo equalizer output terminal.	Analog output.								
49	TRO	O	Tracking servo equalizer output terminal.	(2VREF~AVSS)								
50	VREF	—	Analog reference voltage supply terminal.	—								

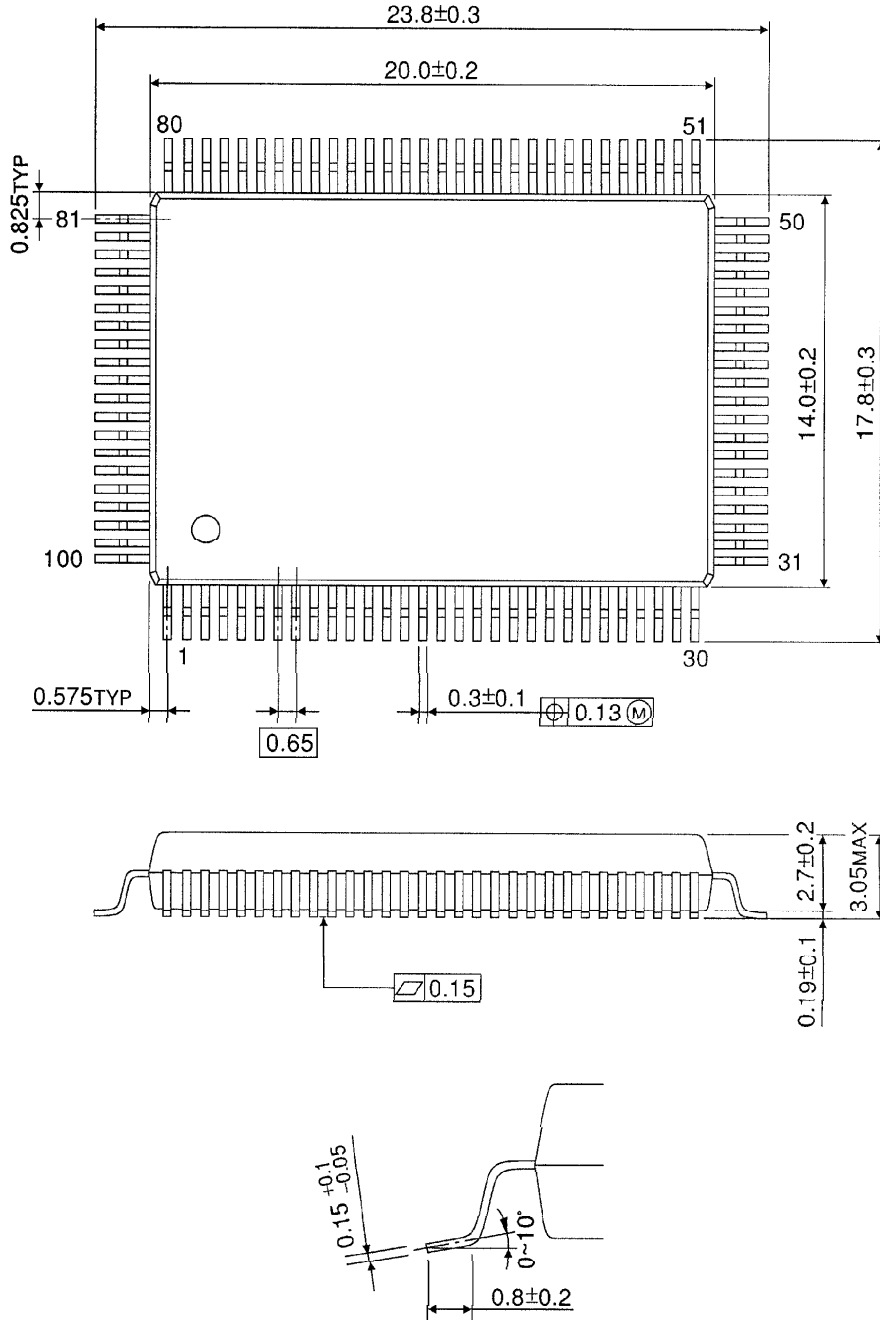
PIN No.	SYMBOL	I/O	FUNCTIONAL DESCRIPTION	REMARKS
51	RFGC	O	RF amplitude adjustment control signal output terminal.	3-state PWM signal output. (2V <sub>REF</sub> , V <sub>REF</sub> , V <sub>SS</sub> ) (PWM carrier = 88.2kHz)
52	TEBC	O	Tracking balance control signal output terminal.	
53	TEBC	O	Feed equalizer output terminal.	
54	TEBC	O	Speed error signal or feed search equalizer output terminal.	
55	DMO	O	Disk equalizer output terminal. (PWM carrier = 88.2kHz for DSP, Synchronize to PXO)	3-state output. (2V <sub>REF</sub> , V <sub>REF</sub> , V <sub>SS</sub> )
56	2V <sub>REF</sub>	—	Analog double reference voltage supply terminal.	—
57	SEL	O	APC circuit ON/OFF indication signal output terminal. At the laser on time, UHF = L at "Hi-Z" level and UHF = H at "H" level.	—
58	FLGA	O	External flag output terminal for internal signal. Can select signal from TEZC, FOON, FOK and RFZC by command.	—
59	FLGB	O	External flag output terminal for internal signal. Can select signal from DFCT, FOON, FMON and RFZC by command.	—
60	FLGC	O	External flag output terminal for internal signal. Can select signal from TRON, TRSR, FOK and SRCH by command.	—
61	FLGD	O	External flag output terminal for internal signal. Can select signal from TRON, DMON, HYS and SHC by command.	—
62	V <sub>DD</sub>	—	Digital power supply voltage terminal.	—
63	V <sub>SS</sub>	—	Digital GND terminal.	—
64	IO0	I/O	General I/O terminal. Can change over input port or output port by command. At the input mode time can readout a state of terminal (H/L) by read command. At the output mode time can control a state of terminal (H/L/HiZ) by command.	—
65	IO1			
66	IO2			
67	IO3			
68	DMOUT	I	This terminal controls IO0~IO3 terminal. At "L" level time, IO0, 1 out feed equalizer signal of 2-state PWM, IO2, 3 out disk equalizer signal of 2-state PWM.	With pull-up resistor.
69	CKSE	I	Normally, keep at open.	With pull-up resistor.
70	DACT	I	DAC test mode terminal. Normally, keep at open.	With pull-up resistor.
71	TESIN	I	Test input terminal. Normally, keep at "L" level.	Analog input.
72	TESIO1	I	Test input/output terminal. Normally, keep at "L" level.	Analog input.
73	V <sub>SS</sub>	—	Digital GND terminal.	—

PIN No.	SYMBOL	I/O	FUNCTIONAL DESCRIPTION	REMARKS
74	PXI	I	Crystal oscillator connecting input terminal for DSP. Normally, keep at "L" level.	—
75	PXO	O	Crystal oscillator connecting output terminal for DSP.	
76	V <sub>DD</sub>	—	Digital power supply voltage terminal.	—
77	XV <sub>SS</sub>	—	Oscillator GND terminal for system clock.	—
78	XI	I	Crystal oscillator connecting input terminal for system clock.	—
79	XO	O	Crystal oscillator connecting output terminal for system clock.	—
80	XV <sub>DD</sub>	—	Oscillator power supply voltage terminal for system clock.	—
81	DV <sub>SR</sub>	—	Analog GND terminal for DA converter. (R-ch)	—
82	RO	O	R channel data forward output terminal.	—
83	DV <sub>DD</sub>	—	Analog supply voltage terminal for DA converter.	—
84	DVR	—	Reference voltage terminal for DA converter.	—
85	LO	O	L channel data forward output terminal.	—
86	DV <sub>SL</sub>	—	Analog GND terminal for DA converter. (L-ch)	—
87	TEST1	I	Test mode terminal. Normal, keep at open.	With pull-up resistor.
88	TEST2	I	Test mode terminal. Normal, keep at open.	With pull-up resistor.
89	TEST3	I	Test mode terminal. Normal, keep at open.	With pull-up resistor.
90	BUS0	I/O	Micon interface data input/output terminal.	Schmit input. With pull-up resistor.
91	BUS1	I/O		
92	BUS2	I/O		
93	BUS3	I/O		
94	V <sub>DD</sub>	—	Digital power supply voltage terminal.	—
95	V <sub>SS</sub>	—	Digital GND terminal.	—
96	BUCK	I	Micon interface clock input terminal.	Schmit input.
97	$\overline{\text{CCE}}$	I	Command and data sending/receiving chip enable signal input terminal. The bus line becomes active at "L" level.	Schmit input.
98	TEST4	I	Test mode terminal. Normal, keep at open.	With pull-up resistor.
99	$\overline{\text{TSMOD}}$	I	Local test mode selection terminal.	With pull-up resistor.
100	$\overline{\text{RST}}$	I	Reset signal input terminal. Reset at "L" level.	With pull-up resistor.

OUTLINE DRAWING

QFP100-P-1420-0.65A

Unit : mm



Weight : 1.6g (Typ.)