OKI Semiconductor

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MSM63238

4-Bit Microcontroller with Built-in POCSAG Decoder and Melody Circuit, Operating at 0.9 V (Min.)

GENERAL DESCRIPTION

The MSM63238 is a CMOS 4-bit microcontroller with a built-in POCSAG (Post Office Code Standardization Advisory Group) decoder.
The MSM63238 employs Oki's original nX-4/250 CPU core and is suitable for pager applications.
The MSM63P238 is a one-time-programmable ROM-version product having one-time PROM (OTP) as internal program memory.
The specifications of the MSM63P238 are equal to those of the MSM63238 except for electrical characteristics, packaging (only 80-pin flat package is available for the MSM63P238), and some functions.

FEATURES

- Rich instruction set
  439 instructions
  Transfer, rotate, increment/decrement, arithmetic operations, comparison, logic operations, mask operations, bit operations, ROM table reference, external memory transfer, stack operations, flag operations, branch, conditional branch, call/return, control.

- Rich selection of addressing modes
  Indirect addressing of four data memory types, with current bank register, extra bank register, HL register and XY register.
  Data memory bank internal direct addressing mode.

- Processing speed
  Two clocks per machine cycle, with most instructions executed in one machine cycle.
  Minimum instruction execution time : 61 µs (@ 32.768 kHz system clock)
  1 µs (@ 2 MHz system clock)

- Clock generation circuit
  Low-speed clock : 32.768 kHz/38.4 kHz/76.8 kHz crystal oscillator
  High-speed clock : 2 MHz (Max.) RC or ceramic oscillator select

- Program memory space
  16K words
  Basic instruction length is 16 bits/1 word

- Data memory space
  1K nibbles

- External data memory space
  64 Kbytes (expandable by using an I/O port)

- Stack level
  - Call stack level : 16 levels
  - Register stack level : 16 levels

- POCSAG decoder
  - Data rate : 512 bps/1200 bps/2400 bps
  - User frame : 3 types
  - User address : 6 types
  - Battery saving mode (for controlling intermittent operations of RF receiver)

- I/O ports
  - Input ports: Selectable as input with pull-up resistance/input with pull-down resistance/high-impedance input
  - Output ports: Selectable as P-channel open drain output/N-channel open drain output/CMOS output/high-impedance output
  - Input-output ports: Selectable as input with pull-up resistance/input with pull-down resistance/high-impedance input
    Selectable as P-channel open drain output/N-channel open drain output/CMOS output/high-impedance output
  - Can be interfaced with external peripherals that use a different power supply than this device uses.
  - Number of ports:
    - Input port : 1 port × 4 bits
    - Output port : 6 ports × 4 bits
    - Input-output port : 5 ports × 4 bits
      1 port × 2 bits

- Melody output function
  - Melody sound frequency : 529 to 2979 Hz
  - Tone length : 63 types
  - Tempo : 15 types
  - Note data : Resides in the program memory
  - Buzzer drive signal output : 4 kHz

- Reset function
  - Reset through RESET pin
  - Power-on reset
  - Reset by low-speed oscillation halt

- Battery check
  - Low-voltage supply check
  - Criterion voltage : Can be selected as 1.05 ±0.10 V, 1.30 ±0.15 V, 2.20 ±0.20 V or 2.80 ±0.30 V

- Power supply backup
  - Backup circuit (voltage multiplier) enables operation at 0.9 V minimum

- Timers and counter
  8-bit timer × 4
  Selectable as auto-reload mode/capture mode/clock frequency measurement mode
  Watchdog timer × 1
  15-bit time base counter × 1
  1, 2, 4, 8, 16, 32, 64, and 128 Hz signals can be read

- Serial port

Mode	:	UART mode, synchronous mode
UART communication speed	:	1200 bps, 2400 bps, 4800 bps, 9600 bps
Clock frequency in synchronous mode	:	32.768 kHz (internal clock mode), external clock frequency
Data length	:	5 to 8 bits

- Interrupt sources

External interrupt	:	3
Internal interrupt	:	15 (watchdog timer interrupt is a nonmaskable interrupt)

- Operating voltage

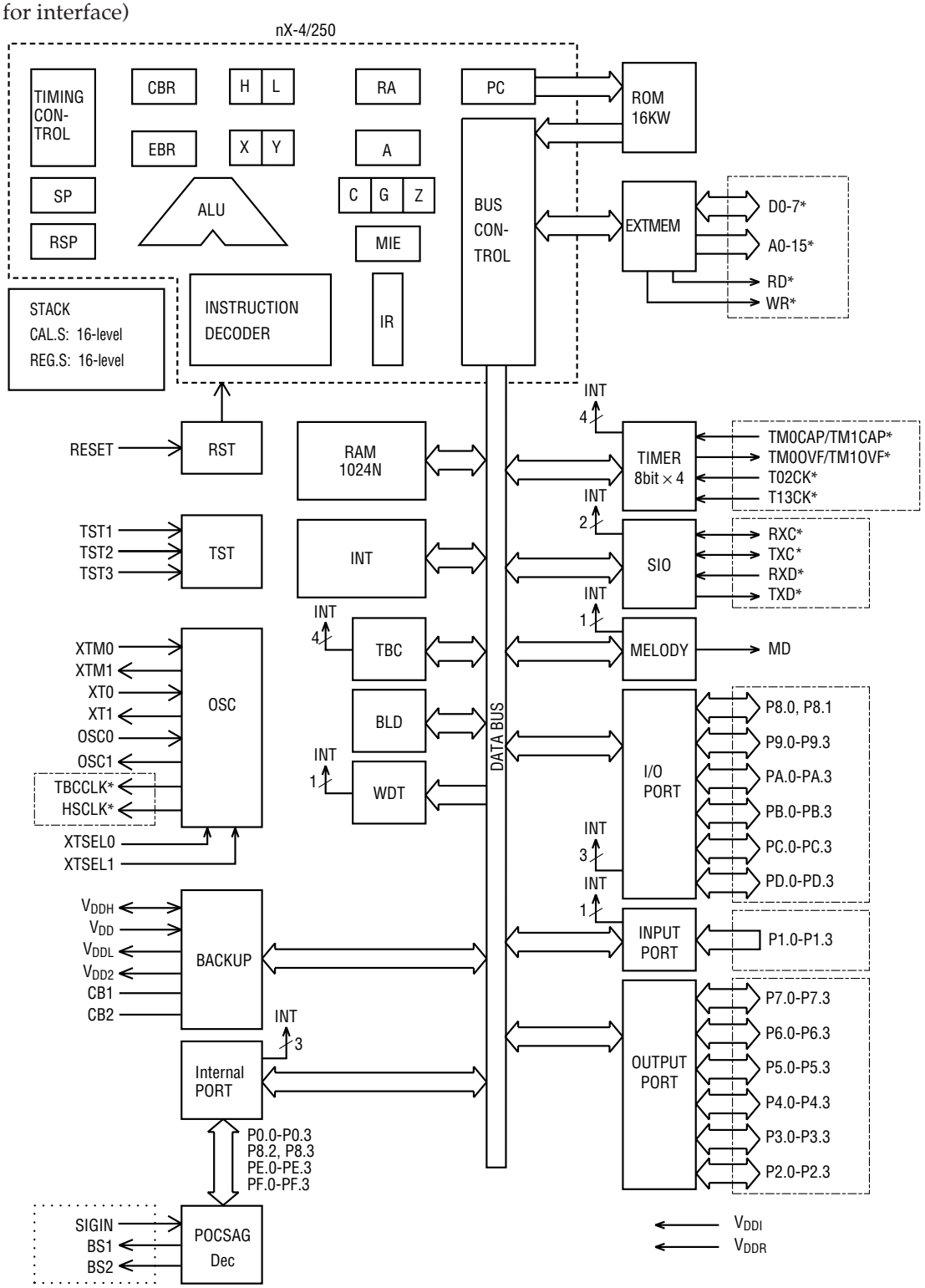
When backup used	:	0.9 to 2.7 V (Low-speed clock operating) 1.2 to 2.7 V (Operating frequency: 300 to 500 kHz) 1.5 to 2.7 V (Operating frequency: 200 kHz to 1 MHz)
When backup not used	:	1.8 to 5.5 V (Operating frequency: 300 to 500 kHz) 2.2 to 5.5 V (Operating frequency: 300 kHz to 1 MHz) 2.7 to 5.5 V (Operating frequency: 200 kHz to 2 MHz)

- Package options:

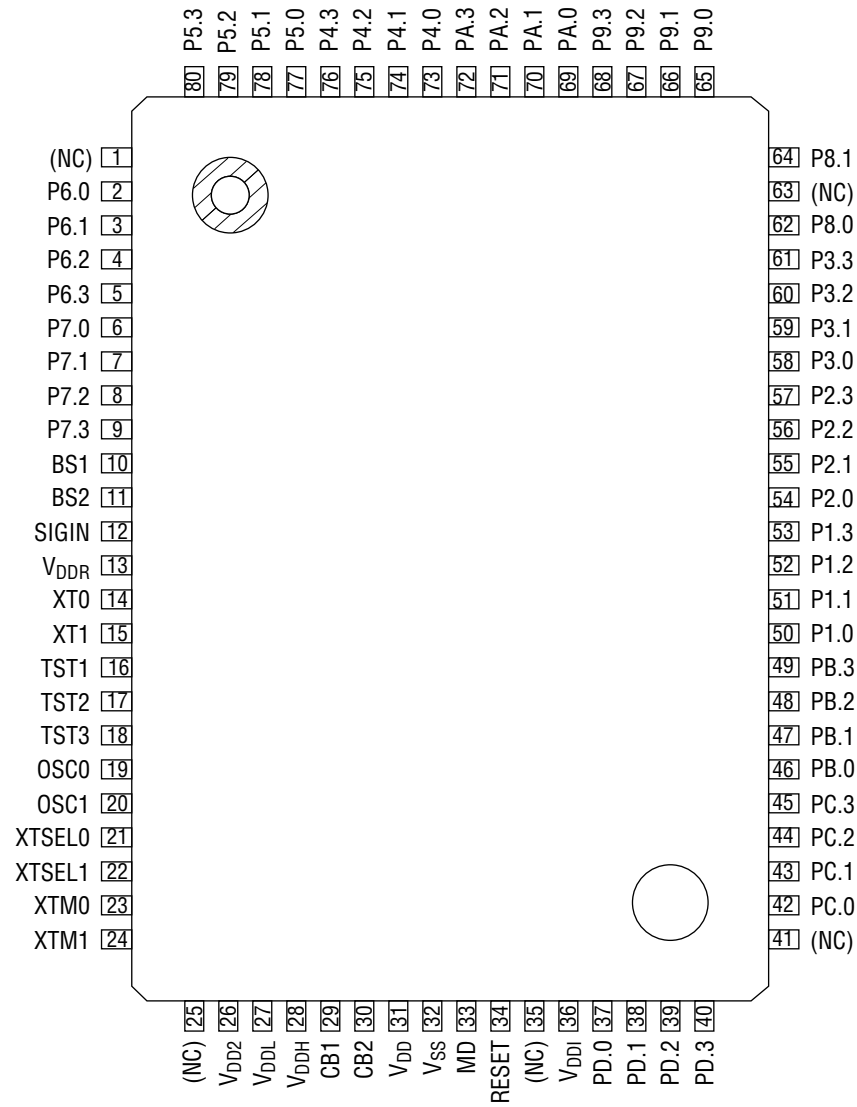
80-pin plastic QFP (QFP80-P-1420-0.80-BK)	:	(Product name: MSM63238-xxxGS-BK)
100-pin plastic TQFP (TQFP100-P-1414-0.50-K)	:	(Product name: MSM63238-xxxTS-K)
Chip	:	MSM63238-xxx xxx indicates a code number.

BLOCK DIAGRAM

An asterisk (*) indicates the port secondary function. ⬚ and ⬚ indicate that the power is supplied from V_{DDI} to the circuits corresponding to the signal names inside ⬚, and from V_{DDR} to the circuits corresponding to signal names inside ⬚. (V_{DDI} and V_{DDR}: power supply for interface)



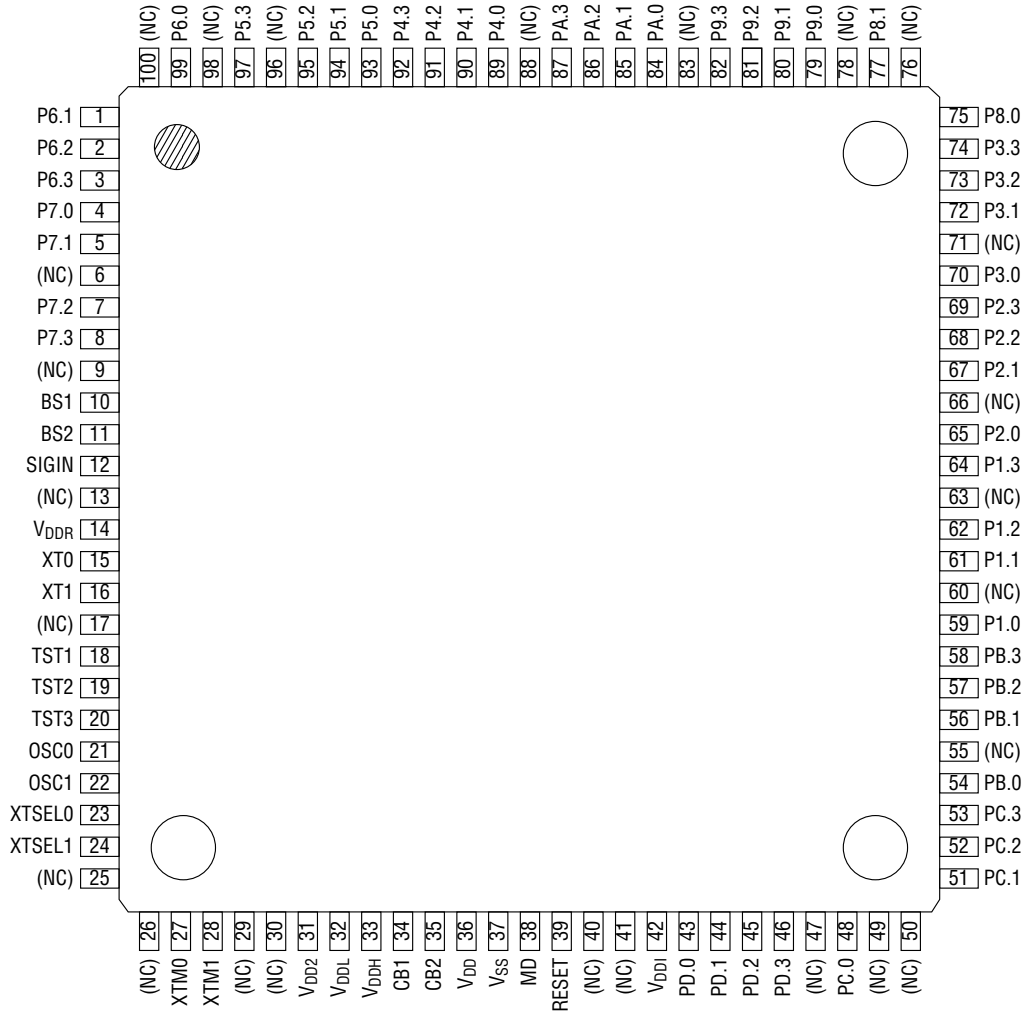
PIN CONFIGURATION (TOP VIEW)



80-Pin Plastic QFP

Note: Pins marked as (NC) are no-connection pins which are left open.

PIN CONFIGURATION (TOP VIEW) (continued)

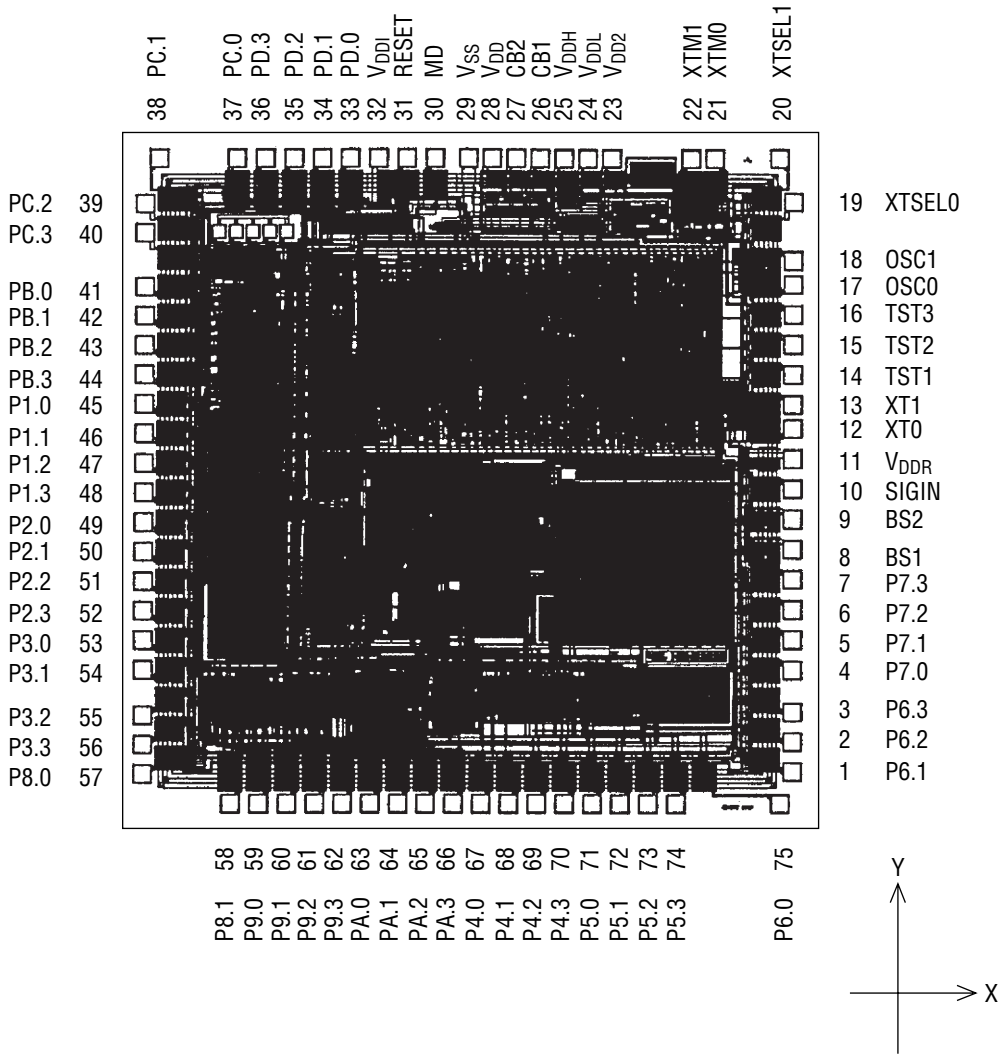


100-Pin Plastic TQFP

Note: Pins marked as (NC) are no-connection pins which are left open.

PAD CONFIGURATION

Pad Layout



Chip Size	: 4.55 mm × 4.55 mm
Chip Thickness	: 350 µm (typ.)
Coordinate Origin	: Chip center
Pad Hole Size	: 110 µm × 110 µm
Pad Size	: 120 µm × 120 µm
Minimum Pad Pitch	: 150 µm

Note: The chip substrate voltage is V_{SS}.

Pad Coordinates

Pad No.	Pad Name	X (µm)	Y (µm)	Pad No.	Pad Name	X (µm)	Y (µm)
1	P6.1	2123.6	–1897.7	39	PC.2	–2123.6	1810.6
2	P6.2	2123.6	–1701.4	40	PC.3	–2123.6	1618.5
3	P6.3	2123.6	–1505.4	41	PB.0	–2123.6	1264.2
4	P7.0	2123.6	–1231.1	42	PB.1	–2123.6	1072.2
5	P7.1	2123.6	–1034.8	43	PB.2	–2123.6	880.1
6	P7.2	2123.6	–838.8	44	PB.3	–2123.6	688.0
7	P7.3	2123.6	–642.5	45	P1.0	–2123.6	496.0
8	BS1	2123.6	–446.2	46	P1.1	–2123.6	303.9
9	BS2	2123.6	–250.2	47	P1.2	–2123.6	111.8
10	SIGIN	2123.6	–54.0	48	P1.3	–2123.6	–80.6
11	V_{DDR}	2123.6	142.0	49	P2.0	–2123.6	–272.7
12	XT0	2123.6	338.3	50	P2.1	–2123.6	–464.8
13	XT1	2123.6	495.0	51	P2.2	–2123.6	–656.8
14	TST1	2123.6	691.3	52	P2.3	–2123.6	–848.9
15	TST2	2123.6	887.2	53	P3.0	–2123.6	–1041.0
16	TST3	2123.6	1083.6	54	P3.1	–2123.6	–1233.1
17	OSC0	2123.6	1279.8	55	P3.2	–2123.6	–1529.1
18	OSC1	2123.6	1436.5	56	P3.3	–2123.6	–1721.2
19	XTSEL0	2123.6	1819.3	57	P8.0	–2123.6	–1913.3
20	XTSEL1	2031.2	2107.3	58	P8.1	–1552.5	–2107.3
21	XTM0	1609.4	2107.3	59	P9.0	–1370.2	–2107.3
22	XTM1	1452.8	2107.3	60	P9.1	–1187.6	–2107.3
23	V_{DD2}	938.6	2107.3	61	P9.2	–1005.2	–2107.3
24	V_{DDL}	782.0	2107.3	62	P9.3	–822.9	–2107.3
25	V_{DDH}	625.3	2107.3	63	PA.0	–640.6	–2107.3
26	CB1	468.6	2107.3	64	PA.1	–458.2	–2107.3
27	CB2	312.0	2107.3	65	PA.2	–275.9	–2107.3
28	V_{DD}	155.4	2107.3	66	PA.3	–93.6	–2107.3
29	V_{SS}	–1.3	2107.3	67	P4.0	88.7	–2107.3
30	MD	–219.4	2107.3	68	P4.1	271.0	–2107.3
31	RESET	–405.6	2107.3	69	P4.2	453.4	–2107.3
32	V_{DDI}	–592.2	2107.3	70	P4.3	635.7	–2107.3
33	PD.0	–778.4	2107.3	71	P5.0	818.0	–2107.3
34	PD.1	–964.9	2107.3	72	P5.1	1000.3	–2107.3
35	PD.2	–1151.2	2107.3	73	P5.2	1182.7	–2107.3
36	PD.3	–1337.7	2107.3	74	P5.3	1365.0	–2107.3
37	PC.0	–1523.9	2107.3	75	P6.0	2042.0	–2107.3
38	PC.1	–2031.2	2107.3				

PIN DESCRIPTIONS

The basic functions of each pin of the MSM63238 are described in Table 1.
A symbol with a slash (/) denotes a pin that has a secondary function.
Refer to Table 2 for secondary functions.
For type, "—" denotes a power supply pin, "I" an input pin, "O" an output pin, and "I/O" an input-output pin.
For pin, "GS-BK" denotes an 80-pin flat package (80QFP) and "TS-K" a 100-pin flat package (100TQFP).

Table 1 Pin Descriptions (Basic Functions)

Function	Symbol	Pin		Type	Description
		GS-BK	TS-K		
Power Supply	V_{DD}	31	36	—	Positive power supply
	V_{SS}	32	37	—	Negative power supply
	V_{DDR}	13	14	—	Interface power supply for SIGIN, BS1, BS2
	V_{DDI}	36	42	—	Positive power supply pin for external interface (power supply for input, output, and I/O ports)
	V_{DDL}	27	32	—	Positive power supply pin for internal logic (internally generated). A capacitor (0.1 μF) should be connected between this pin and V_{SS}.
	V_{DD2}	26	31	—	Positive power supply pin for low-speed clock (internally generated)
	V_{DDH}	28	33	—	Voltage multiplier pin for power supply backup (internally generated). A capacitor (1.0 μF) should be connected between this pin and V_{SS}.
	CB1	29	34	—	Pins to connect a capacitor for voltage multiplier. A capacitor (1.0 μF) should be connected between CB1 and CB2.
	CB2	30	35	—	
Oscillation	XT0	14	15	I	Clock oscillation pins for POCSAG decoder. A 32.768 kHz, 38.4 kHz, or 76.8 kHz crystal and capacitor (C_G) should be connected to these pins.
	XT1	15	16	O	
	XTM0	23	27	I	Low-speed clock oscillation pins for CPU. A 32.768 kHz crystal and capacitor (C_{GM}) should be connected to these pins.
	XTM1	24	28	O	
	OSC0	19	21	I	High-speed clock oscillation pins. A ceramic resonator and capacitors (C_{L0}, C_{L1}) or external oscillation resistor (R_{OS}) should be connected to these pins.
	OSC1	20	22	O	
	XTSEL0	21	23	I	Low-speed CPU clock select pins. These pins are used to select a low-speed CPU clock. Because these are high impedance inputs, be sure to tie these pins to V_{DD} or V_{SS}.
	XTSEL1	22	24		
Test	TST1	16	18	I	Input pins for testing. Pull-down resistors are internally connected to these pins. The user cannot use these pins.
	TST2	17	19		
	TST3	18	20		

Table 1 Pin Descriptions (Basic Functions) (continued)

Function	Symbol	Pin		Type	Description
		GS-BK	TS-K		
Reset	RESET	34	39	I	Reset input pin. Setting this pin to "H" level puts this device into a reset state. Then, setting this pin to "L" level starts executing an instruction from address 0000H. A pull-down resistor is internally connected to this pin.
Melody	MD	33	38	O	Melody output pin (normal phase)
POCSAG Decoder	BS1	10	10	O	Battery saving outputs. Signals to control intermittent operations of RF receiver.
	BS2	11	11		
	SIGIN	12	12	I	Receive data input pin. Input pin for receive data from RF receiver.
Port	P1.0/INT5	50	59	I	4-bit input port. Pull-up resistor input, pull-down resistor input, or high-impedance input is selectable for each bit.
	P1.1/INT5	51	61		
	P1.2/INT5	52	62		
	P1.3/INT5	53	64		
	P2.0	54	65	O	4-bit output ports. P-channel open drain output, N-channel open drain output, CMOS output, or high-impedance output is selectable for each bit.
	P2.1	55	67		
	P2.2	56	68		
	P2.3	57	69		
	P3.0	58	70	O	
	P3.1	59	72		
	P3.2	60	73		
	P3.3	61	74		
	P4.0/A0	73	89	O	
	P4.1/A1	74	90		
	P4.2/A2	75	91		
	P4.3/A3	76	92		
	P5.0/A4	77	93	O	
	P5.1/A5	78	94		
	P5.2/A6	79	95		
	P5.3/A7	80	97		
	P6.0/A8	2	99	O	
	P6.1/A9	3	1		
	P6.2/A10	4	2		
	P6.3/A11	5	3		
	P7.0/A12	6	4	O	
	P7.1/A13	7	5		
	P7.2/A14	8	7		
	P7.3/A15	9	8		

Table 1 Pin Descriptions (Basic Functions) (continued)

Function	Symbol	Pin		Type	Description
		GS-BK	TS-K		
Port	P8.0/$\overline{RD}$	62	75	I/O	2-bit input-output port and 4-bit input-output ports. In input mode, pull-up resistor input, pull-down resistor input, or high-impedance input is selectable for each bit. In output mode, P-channel open drain output, N-channel open drain output, CMOS output, or high-impedance output is selectable for each bit.
	P8.1/$\overline{WR}$	64	77		
	P9.0/D0	65	79	I/O	
	P9.1/D1	66	80		
	P9.2/D2	67	81		
	P9.3/D3	68	82		
	PA.0/D4	69	84	I/O	
	PA.1/D5	70	85		
	PA.2/D6	71	86		
	PA.3/D7	72	87		
	PB.0/INT0/ TM0CAP/ TM0OVF	46	54	I/O	
	PB.1/INT0/ TM1CAP/ TM1OVF	47	56		
	PB.2/INT0/ T02CK	48	57		
	PB.3/INT0/ T13CK	49	58		
	PC.0/INT1/ RXD	42	48	I/O	
	PC.1/INT1/ TXC	43	51		
	PC.2/INT1/ RXC	44	52		
	PC.3/INT1/ TXD	45	53		
	PD.0	37	43	I/O	
	PD.1	38	44		
	PD.2	39	45		
	PD.3	40	46		

Table 2 shows the secondary functions of each pin of the MSM63238.

Table 2 Pin Descriptions (Secondary Functions)

Function	Symbol	Pin		Type	Description
		GS-BK	TS-K		
External Interrupt	PB.0/INT0	46	54	I	External 0 interrupt input pins. The change of input signal level causes an interrupt to occur. The Port B Interrupt Enable register (PBIE) enables or disables an interrupt for each bit.
	PB.1/INT0	47	56		
	PB.2/INT0	48	57		
	PB.3/INT0	49	58		
	PC.0/INT1	42	48	I	External 1 interrupt input pins. The change of input signal level causes an interrupt to occur. The Port C Interrupt Enable register (PCIE) enables or disables an interrupt for each bit.
	PC.1/INT1	43	51		
	PC.2/INT1	44	52		
	PC.3/INT1	45	53		
	P1.0/INT5	50	59	I	External 5 interrupt input pins. The change of input signal level causes an interrupt to occur. The Port 1 Interrupt Enable register (P1IE) enables or disables an interrupt for each bit.
	P1.1/INT5	51	61		
	P1.2/INT5	52	62		
	P1.3/INT5	53	64		
Capture	PB.0/TM0CAP	46	54	I	Timer 0 capture trigger input pin.
	PB.1/TM1CAP	47	56	I	Timer 1 capture trigger input pin.

Table 2 Pin Descriptions (Secondary Functions) (continued)

Function	Symbol	Pin		Type	Description
		GS-BK	TS-K		
Timer	PB.0/TM0OVF	46	54	O	Timer 0 overflow flag output pin.
	PB.1/TM1OVF	47	56	O	Timer 1 overflow flag output pin.
	PB.2/T02CK	48	57	I	External clock input pin for timer 0 and timer 2.
	PB.3/T13CK	49	58	I	External clock input pin for timer 1 and timer 3.
Oscillation Output	PD.2/TBCCLK	39	45	O	Low-speed oscillation clock output pin
	PD.3/HSCLK	40	46	O	High-speed oscillation clock output pin
Serial Port	PC.0/RXD	42	48	I	Serial port receive data input pin
	PC.1/TXC	43	51	I/O	Sync serial port clock input-output pin. Transmit clock output when this device is used as a master processor. Transmit clock input when this device is used as a slave processor.
	PC.2/RXC	44	52	I/O	Sync serial port clock input-output pin. Receive clock output when this device is used as a master processor. Receive clock input when this device is used as a slave processor.
	PC.3/TXD	45	53	O	Serial port transmit data output pin.

Table 2 Pin Descriptions (Secondary Functions) (continued)

Function	Symbol	Pin		Type	Description
		GS-BK	TS-K		
External Memory	P4.0/A0	73	89	O	Address output bus for external memory
	P4.1/A1	74	90		
	P4.2/A2	75	91		
	P4.3/A3	76	92		
	P5.0/A4	77	93		
	P5.1/A5	78	94		
	P5.2/A6	79	95		
	P5.3/A7	80	97		
	P6.0/A8	2	99		
	P6.1/A9	3	1		
	P6.2/A10	4	2		
	P6.3/A11	5	3		
	P7.0/A12	6	4		
	P7.1/A13	7	5		
	P7.2/A14	8	7		
	P7.3/A15	9	8		
	P9.0/D0	65	79	I/O	Data bus for external memory
	P9.1/D1	66	80		
	P9.2/D2	67	81		
	P9.3/D3	68	82		
	PA.0/D4	69	84		
	PA.1/D5	70	85		
	PA.2/D6	71	86		
	PA.3/D7	72	87		
	P8.0/$\overline{RD}$	62	75	O	Read signal output pin for external memory (negative logic)
	P8.1/$\overline{WR}$	64	77	O	Write signal output pin for external memory (negative logic)

ABSOLUTE MAXIMUM RATINGS

(V_{SS} = 0 V)

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage 1	V_{DD}	Backup used, Ta = 25°C	–0.3 to +3.0	V
		Backup not used, Ta = 25°C	–0.3 to +6.0	
Power Supply Voltage 2	V_{DDI}	Ta = 25°C	–0.3 to +6.0	V
Power Supply Voltage 3	V_{DDR}	Ta = 25°C	–0.3 to +6.0	V
Power Supply Voltage 4	V_{DDH}	Ta = 25°C	–0.3 to +6.0	V
Power Supply Voltage 5	V_{DDL}	Ta = 25°C	–0.3 to +6.0	V
Input Voltage 1	V_{IN1}	V_{DD} Input, Ta = 25°C	–0.3 to V_{DD} + 0.3	V
Input Voltage 2	V_{IN2}	V_{DDI} Input, Ta = 25°C	–0.3 to V_{DDI} + 0.3	V
Input Voltage 3	V_{IN3}	V_{DDR} Input, Ta = 25°C	–0.3 to V_{DDR} + 0.3	V
Output Voltage 1	V_{OUT1}	V_{DD} output, Ta = 25°C	–0.3 to V_{DD} + 0.3	V
Output Voltage 2	V_{OUT2}	V_{DDI} output, Ta = 25°C	–0.3 to V_{DDI} + 0.3	V
Output Voltage 3	V_{OUT3}	V_{DDR} output, Ta = 25°C	–0.3 to V_{DDR} + 0.3	V
Output Voltage 4	V_{OUT4}	V_{DDH} output, Ta = 25°C	–0.3 to V_{DDH} + 0.3	V
Storage Temperature	T_{STG}	—	–55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

• When backup is used

(V_{SS} = 0 V)

Parameter	Symbol	Condition	Range	Unit
Operating Temperature	T_{op}	—	–20 to +70	°C
Operating Voltage	V_{DD}	—	0.9 to 2.7	V
	V_{DDI}	—	0.9 to 5.5	V
	V_{DDR}	—	0.9 to 5.5	V
Crystal Oscillation Frequency	f_{XT}	—	30 to 80	kHz
	f_{XTM}	—	30 to 35	kHz
Ceramic Oscillation Frequency	f_{CM}	V_{DD} = 1.2 to 2.7 V	300k to 500k	Hz
		V_{DD} = 1.5 to 2.7 V	200k to 1M	
External RC Oscillator Resistance	R_{OS}	V_{DD} = 1.2 to 2.7 V	100 to 300	kΩ
		V_{DD} = 1.5 to 2.7 V	50 to 300	

• When backup is not used

(V_{SS} = 0 V)

Parameter	Symbol	Condition	Range	Unit
Operating Temperature	T_{op}	—	–20 to +70	°C
Operating Voltage	V_{DD}	—	1.8 to 5.5	V
	V_{DDI}	—	1.8 to 5.5	V
	V_{DDR}	—	1.8 to 5.5	V
Crystal Oscillation Frequency	f_{XT}	—	30 to 80	kHz
	f_{XTM}	—	30 to 35	kHz
Ceramic Oscillation Frequency	f_{CM}	V_{DD} = 1.8 to 5.5 V	300k to 500k	Hz
		V_{DD} = 2.2 to 5.5 V	300k to 1M	
		V_{DD} = 2.7 to 5.5 V	200k to 2M	
External RC Oscillator Resistance	R_{OS}	V_{DD} = 1.8 to 5.5 V	100 to 300	kΩ
		V_{DD} = 2.2 to 5.5 V	50 to 300	
		V_{DD} = 2.7 to 5.5 V	30 to 300	

ELECTRICAL CHARACTERISTICS

DC Characteristics

(V_{DD} = V_{DDI} = V_{DDR} = 0.9 to 5.5 V, V_{SS} = 0 V, Ta = –20 to +70°C unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring Circuit
V_{DDH} Voltage (Backup used)	V_{DDH}	High speed clock stop V_{DD} = 1.5 V C_h, C_{12} = 1 µF	2.8	—	3.0	V	
		High speed clock oscillation (Ceramic oscillation, 1 MHz) V_{DD} = 1.5 V C_h, C_{12} = 1 µF	2.0	—	2.7	V	
V_{DDL} Voltage	V_{DDL}	High speed clock stop	1.0	1.5	2.0	V	
		High speed clock oscillation (V_{DD} = 1.2 to 5.5 V)	1.2	—	5.5	V	
V_{DD2} Voltage	V_{DD2}	—	1.0	1.5	2.0	V	
Crystal Oscillation Start Voltage	V_{STA}	Oscillation start time: within 5 seconds	1.2	—	—	V	
Crystal Oscillation Hold Voltage	V_{HOLD}	Backup used (Ta = 25°C)	0.9	—	—	V	1
		Backup used	1.0	—	—	V	
		Backup not used	1.7	—	—	V	
Crystal Oscillation Stop Detect Time	T_{STOP}	—	0.1	—	5.0	ms	
External Crystal Oscillator Capacitance	C_G, C_{GM}	—	5	—	25	pF	
Internal Crystal Oscillator Capacitance	C_D, C_{DM}	—	20	25	30	pF	
Internal RC Oscillator Capacitance	C_{OS}	—	8	12	16	pF	
POR Voltage	V_{POR1}	V_{DD} = 1.5 V	0.0	—	0.4	V	
		V_{DD} = 3.0 V	0.0	—	0.7	V	
Non-POR Voltage	V_{POR2}	V_{DD} = 1.5 V	1.2	—	1.5	V	
		V_{DD} = 3.0 V	2.0	—	3.0	V	

Notes: 1. "T_{STOP}" indicates that if the crystal oscillator stops over the value of T_{STOP}, the system reset occurs.
2. "POR" denotes Power On Reset.
3. "V_{POR1}" indicates that POR occurs when V_{DD} falls from V_{DD} to V_{POR1} and again rises up to V_{DD}.
4. "V_{POR2}" indicates that POR does not occur when V_{DD} falls from V_{DD} to V_{POR2} and again rises up to V_{DD}.

DC Characteristics (continued)

• When backup is used

(V_{DD} = V_{DDI} = 1.5 V, V_{SS} = 0 V, Ta = –20 to +70°C unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring Circuit
Supply Current 1	I_{DD1}	CPU in HALT mode. (High-speed clock oscillation stop) Decoder in HALT mode. (Decoder oscillation stop)	—	6.0	35	µA	1
Supply Current 2	I_{DD2}	CPU in HALT mode. (High-speed clock oscillation stop) Decoder in carrier on state. (76.8 kHz operation)	—	35	80	µA	
Supply Current 3	I_{DD3}	CPU in HALT mode. (High-speed clock oscillation stop) Decoder in data receiving state. (76.8 kHz operation)	—	85	200	µA	
Supply Current 4	I_{DD4}	CPU in operation at 32 kHz. (High-speed clock oscillation stop) Decoder in HALT mode. (Decoder oscillation stop)	—	22	40	µA	
Supply Current 5	I_{DD5}	CPU in operation at high speed. (RC oscillation, R_{OS} = 51 kΩ) Decoder in HALT mode. (Decoder oscillation stop)	—	600	800	µA	
Supply Current 6	I_{DD6}	CPU in operation at high speed. (Ceramic oscillation, 1 MHz) Decoder in HALT mode. (Decoder oscillaiton stop)	—	700	900	µA	

DC Characteristics (continued)

• When backup is not used

(V_{DD} = V_{DDI} = 3.0 V, V_{SS} = 0 V, Ta = –20 to +70°C unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring Circuit
Supply Current 1	I_{DD1}	CPU in HALT mode. (High-speed clock oscillation stop) Decoder in HALT mode. (Decoder oscillation stop)	—	3.0	20	µA	1
Supply Current 2	I_{DD2}	CPU in HALT mode. (High-speed clock oscillation stop) Decoder in carrier on state. (76.8 kHz operation)	—	17	40	µA	
Supply Current 3	I_{DD3}	CPU in HALT mode. (High-speed clock oscillation stop) Decoder in data receiving state. (76.8 kHz operation)	—	42	100	µA	
Supply Current 4	I_{DD4}	CPU in operation at 32 kHz. (High-speed clock oscillation stop) Decoder in HALT mode. (Decoder oscillation stop)	—	10	25	µA	
Supply Current 5	I_{DD5}	CPU in operation at high speed. (RC oscillation, R_{OS} = 51 kΩ) Decoder in HALT mode. (Decoder oscillation stop)	—	450	600	µA	
Supply Current 6	I_{DD6}	CPU in operation at high speed. (Ceramic oscillation, 2 MHz) Decoder in HALT mode. (Decoder oscillation stop)	—	800	1000	µA	

DC Characteristics (continued)

(V_{DD} = V_{DDI} = V_{DDH} = V_{DDR} = 3.0 V, V_{SS} = 0 V, Ta = –20 to +70°C unless otherwise specified)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit	Measuring Circuit
Output Current 1 (P2.0 to P2.3) (P3.0 to P3.3) (P4.0 to P4.3) ⋮ (PC.0 to PC.3) (PD.0 to PD.3)	I_{OH1}	V_{OH1} = V_{DDI} – 0.5 V	V_{DDI} = 1.5 V	–2.5	–1.4	–0.4	mA	
			V_{DDI} = 3.0 V	–6.0	–3.5	–1.0	mA	
			V_{DDI} = 5.0 V	–8.5	–5.0	–1.5	mA	
	I_{OL1}	V_{OL1} = 0.5 V	V_{DDI} = 1.5 V	0.4	1.4	2.5	mA	
			V_{DDI} = 3.0 V	1.0	3.0	6.0	mA	
			V_{DDI} = 5.0 V	1.5	3.7	8.5	mA	
Output Current 2 (MD)	I_{OH2}	V_{OH2} = V_{DD} – 0.7 V	V_{DD} = 1.5 V	–4.0	–2.0	–0.5	mA	
			V_{DD} = 3.0 V	–11.0	–6.0	–2.0	mA	
			V_{DD} = V_{DDH} = 5.0 V	–14.0	–9.0	–4.0	mA	
	I_{OL2}	V_{OL2} = 0.7 V	V_{DD} = 1.5 V	0.5	2.0	4.0	mA	
			V_{DD} = 3.0 V	2.0	5.5	11.0	mA	
			V_{DD} = V_{DDH} = 5.0 V	4.0	7.0	14.0	mA	
Output Current 3 (BS1, BS2)	I_{OH3}	V_{OH3} = V_{DDR} – 0.5 V	V_{DDR} = 1.5 V	–7.0	–4.5	–1.0	mA	
			V_{DDR} = 3.0 V	–16.0	–10.0	–2.0	mA	
			V_{DDR} = 5.0 V	–24.0	–14.0	–3.0	mA	
	I_{OL3}	V_{OL3} = 0.5 V	V_{DDR} = 1.5 V	1.0	4.0	7.0	mA	2
			V_{DDR} = 3.0 V	2.0	8.0	16.0	mA	
			V_{DDR} = 5.0 V	3.0	9.5	24.0	mA	
Output Current 4 (OSC1)	I_{OH4R}	V_{OH4R} = V_{DDH} – 0.5 V (RC oscillation)	V_{DD} = V_{DDH} = 3.0 V	–2.5	–1.3	–0.25	mA	
			V_{DD} = V_{DDH} = 5.0 V	–3.5	–1.7	–0.5	mA	
	I_{OL4R}	V_{OL4R} = 0.5 V (RC oscillation)	V_{DD} = V_{DDH} = 3.0 V	0.25	1.5	2.5	mA	
			V_{DD} = V_{DDH} = 5.0 V	0.5	1.8	3.5	mA	
	I_{OH4C}	V_{OH4C} = V_{DDH} – 0.5 V (ceramic oscillation)	V_{DD} = V_{DDH} = 3.0 V	–300	–160	–60	µA	
			V_{DD} = V_{DDH} = 5.0 V	–400	–240	–100	µA	
	I_{OL4C}	V_{OL4C} = 0.5 V (ceramic oscillation)	V_{DD} = V_{DDH} = 3.0 V	60	170	300	µA	
			V_{DD} = V_{DDH} = 5.0 V	100	210	400	µA	
Output Leakage (P2.0 to P2.3) (P3.0 to P3.3) (P4.0 to P4.3) ⋮ (PD.0 to PD.3)	I_{OOH}	V_{OH} = V_{DDI}		—	—	1.0	µA	
	I_{OOL}	V_{OL} = V_{SS}		–1.0	—	—	µA	

DC Characteristics (continued)

(V_{DD} = V_{DDI} = V_{DDH} = V_{DDR} = 3.0 V, V_{SS} = 0 V, Ta = –20 to +70°C unless otherwise specified)

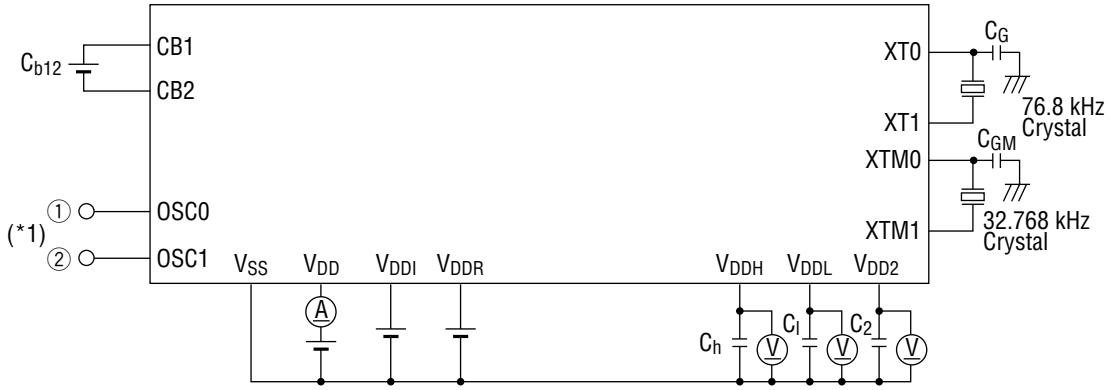
Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit	Measuring Circuit
Input Current 1 (P1.0 to P1.3) (P8.0, P8.1) (P9.0 to P9.3) ⋮ (PD.0 to PD.3)	I_{IH1}	V_{IH1} = V_{DDI} (when pulled down)	V_{DDI} = 1.5 V	2	20	45	µA	3
			V_{DDI} = 3.0 V	30	120	260	µA	
			V_{DDI} = 5.0 V	70	350	650	µA	
	I_{IL1}	V_{IL1} = V_{SS} (when pulled up)	V_{DDI} = 1.5 V	–45	–20	–2	µA	
			V_{DDI} = 3.0 V	–260	–120	–30	µA	
			V_{DDI} = 5.0 V	–650	–350	–70	µA	
	I_{IH1Z}	V_{IH1} = V_{DDI} (in a high impedance state)		0.0	—	1.0	µA	
	I_{IL1Z}	V_{IL1} = V_{SS} (in a high impedance state)		–1.0	—	0.0	µA	
Input Current 2 (SIGIN)	I_{IH2Z}	V_{IH2} = V_{DDR}		0.0	—	1.0	µA	
	I_{IL2Z}	V_{IL2} = V_{SS}		–1.0	—	0.0	µA	
Input Current 3 (OSC0)	I_{IL3}	V_{IL3} = V_{SS} (when pulled up)	V_{DD} = V_{DDH} = 3.0 V	–350	–170	–30	µA	
			V_{DD} = V_{DDH} = 5.0 V	–750	–450	–200	µA	
	I_{IH3R}	V_{IH3} = V_{DDH} (RC oscillation)		0.0	—	1.0	µA	
	I_{IL3R}	V_{IL3} = V_{SS} (RC oscillation)		–1.0	—	0.0	µA	
	I_{IH3C}	V_{IH3} = V_{DDH} (ceramic oscillation)	V_{DD} = V_{DDH} = 3.0 V	0.1	0.5	1.0	µA	
			V_{DD} = V_{DDH} = 5.0 V	0.75	1.5	3.0	µA	
	I_{IL3C}	V_{IL3} = V_{SS} (ceramic oscillation)	V_{DD} = V_{DDH} = 3.0 V	–1.0	–0.5	–0.1	µA	
			V_{DD} = V_{DDH} = 5.0 V	–3.0	–1.5	–0.75	µA	
Input Current 4 (RESET)	I_{IH4}	V_{IH4} = V_{DD}	V_{DD} = 1.5 V	10	180	350	µA	
			V_{DD} = 3.0 V	150	1100	2400	µA	
			V_{DD} = V_{DDH} = 5.0 V	0.5	2.7	5.0	mA	
	I_{IL4}	V_{IL4} = V_{SS}		–1.0	—	0.0	µA	
Input Current 5 (TST1, TST2, TST3)	I_{IH5}	V_{IH5} = V_{DD}	V_{DD} = 1.5 V	50	750	1500	µA	
			V_{DD} = 3.0 V	0.5	3.0	5.5	mA	
			V_{DD} = V_{DDH} = 5.0 V	0.25	6.5	11.0	mA	
	I_{IL5}	V_{IL5} = V_{SS}		–1.0	—	0.0	µA	
Input Current 6 (XTSEL0, XTSEL1)	I_{IH6Z}	V_{IH6} = V_{DD}		0.0	—	1.0	µA	
	I_{IL6Z}	V_{IL6} = V_{SS}		–1.0	—	0.0	µA	

DC Characteristics (continued)

(V_{DD} = V_{DDI} = V_{DDH} = V_{DDR} = 3.0 V, V_{SS} = 0 V, Ta = –20 to +70°C unless otherwise specified)

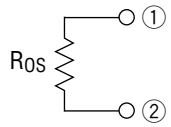
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring Circuit
Input Voltage 1 (P1.0 to P1.3) (P8.0, P8.1) (P9.0 to P9.3) ⋮ (PD.0 to PD.3)	V_{IH1}	V_{DDI} = 1.5 V	1.2	—	1.5	V	
		V_{DDI} = 3.0 V	2.4	—	3.0	V	
		V_{DDI} = 5.0 V	4.0	—	5.0	V	
	V_{IL1}	V_{DDI} = 1.5 V	0.0	—	0.3	V	
		V_{DDI} = 3.0 V	0.0	—	0.6	V	
		V_{DDI} = 5.0 V	0.0	—	1.0	V	
Input Voltage 2 (SIGIN)	V_{IH2}	V_{DDR} = 1.5 V	1.2	—	1.5	V	
		V_{DDR} = 3.0 V	2.4	—	3.0	V	
		V_{DDR} = 5.0 V	4.0	—	5.0	V	
	V_{IL2}	V_{DDR} = 1.5 V	0.0	—	0.3	V	
		V_{DDR} = 3.0 V	0.0	—	0.6	V	
		V_{DDR} = 5.0 V	0.0	—	1.0	V	
Input Voltage 3 (OSC0)	V_{IH3}	V_{DD} = V_{DDH} = 3.0 V	2.4	—	3.0	V	
		V_{DD} = V_{DDH} = 5.0 V	4.0	—	5.0	V	
	V_{IL3}	V_{DD} = V_{DDH} = 3.0 V	0.0	—	0.6	V	4
		V_{DD} = V_{DDH} = 5.0 V	0.0	—	1.0	V	
Input Voltage 4 (RESET, TST1, TST2, TST3, XTSEL0, XTSEL1)	V_{IH4}	V_{DD} = 1.5 V	1.35	—	1.5	V	
		V_{DD} = 3.0 V	2.4	—	3.0	V	
		V_{DD} = V_{DDH} = 5.0 V	4.0	—	5.0	V	
	V_{IL4}	V_{DD} = 1.5 V	0.0	—	0.15	V	
		V_{DD} = 3.0 V	0.0	—	0.6	V	
		V_{DD} = V_{DDH} = 5.0 V	0.0	—	1.0	V	
Hysteresis Width 1 (P1.0 to P1.3) (P8.0, P8.1) ⋮ (PD.0 to PD.3)	ΔV_{T1}	V_{DDI} = 1.5 V	0.05	0.1	0.3	V	
		V_{DDI} = 3.0 V	0.2	0.5	1.0	V	
		V_{DDI} = 5.0 V	0.25	1.0	1.5	V	
Hysteresis Width 2 (RESET, TST1, TST2, TST3, XTSEL0, XTSEL1)	ΔV_{T2}	V_{DD} = 1.5 V	0.05	0.1	0.3	V	
		V_{DD} = 3.0 V	0.2	0.5	1.0	V	
		V_{DD} = V_{DDH} = 5.0 V	0.25	1.0	1.5	V	
Input Pin Capacitance (P1.0 to P1.3) (P8.0, P8.1) (P9.0 to P9.3) ⋮ (PD.0 to PD.3)	C_{IN}	—	—	—	5	pF	1

Measuring circuit 1

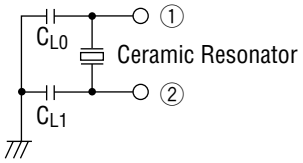


C_l, C_2	: 0.1 µF
C_h, C_{b12}	: 1 µF
C_G, C_{GM}	: 15 pF
C_{L0}	: 30 pF
C_{L1}	: 30 pF
Ceramic Resonator	: CSB1000J (1 MHz) CSA2.00MG (2 MHz) (Murata MFG.-make)

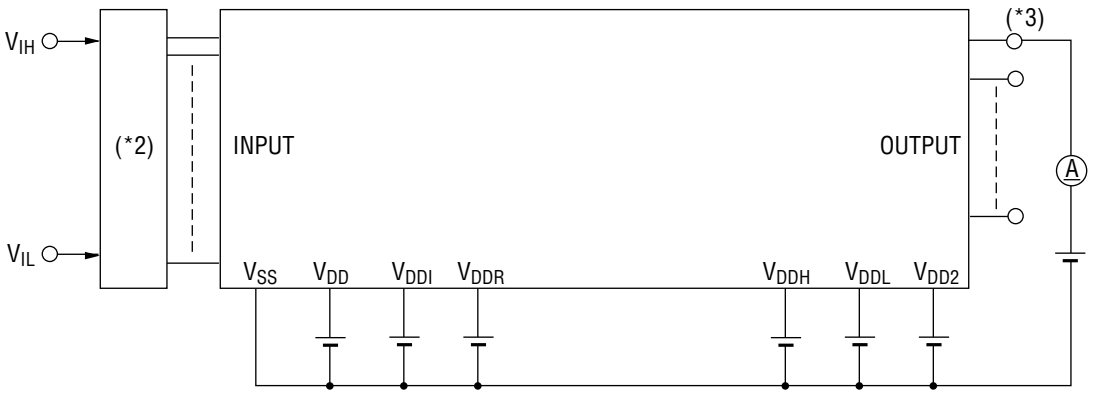
*1 RC Oscillator



Ceramic Oscillator

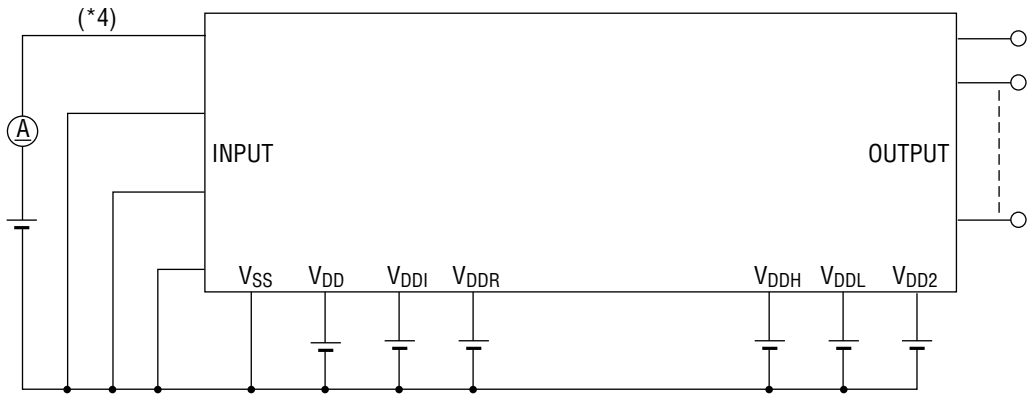


Measuring circuit 2

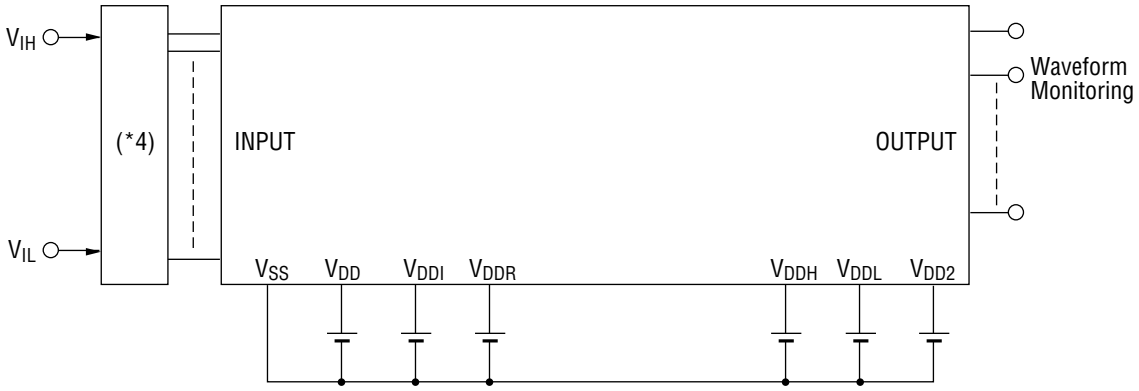


*2 Input logic circuit to determine the specified measuring conditions.
*3 Measured at the specified output pins.

Measuring circuit 3



Measuring circuit 4



*4 Measured at the specified input pins.

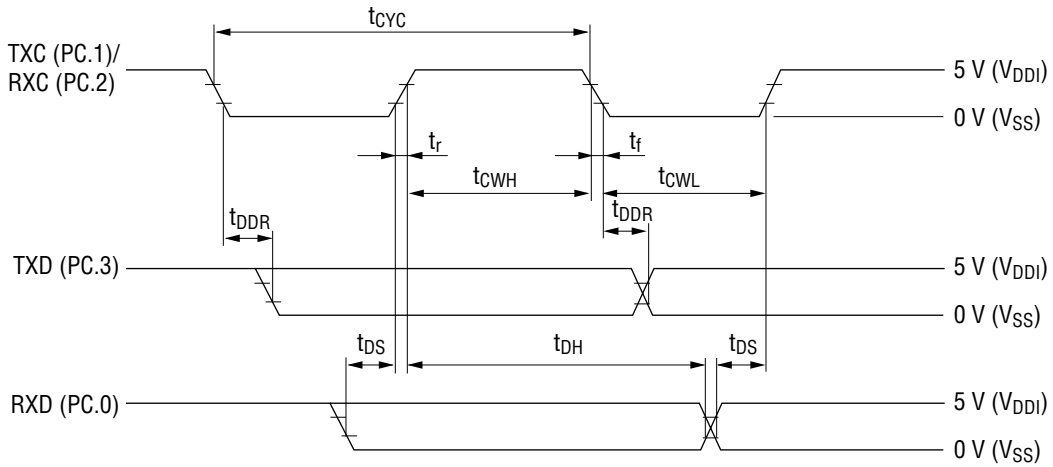
AC Characteristics (Serial Interface, Serial Port)

(V_{DD} = V_{DDR} = 0.9 to 5.5 V, V_{DDH} = 1.8 to 5.5 V, V_{SS} = 0 V, V_{DDI} = 5.0 V, Ta = –20 to +70°C unless otherwise specified)

(1) Synchronous Communication

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
TXC/RXC Input Fall Time	t_f	—	—	—	1.0	µs
TXC/RXC Input Rise Time	t_r	—	—	—	1.0	µs
TXC/RXC Input "L" Level Pulse Width	t_{CWL}	—	0.8	—	—	µs
TXC/RXC Input "H" Level Pulse Width	t_{CWH}	—	0.8	—	—	µs
TXC/RXC Input Cycle Time	t_{CYC}	—	2.0	—	—	µs
TXC/RXC Output Cycle Time	$t_{CYC1(O)}$	CPU in operation state at 32 kHz	—	30.5	—	µs
	$t_{CYC2(O)}$	CPU in operation at 2 MHz V_{DD} = V_{DDH} = 2.7 V to 5.5 V	—	0.5	—	µs
TXD Output Delay Time	t_{DDR}	Output load capacitance 10 pF	—	—	0.4	µs
RXD Input Setup Time	t_{DS}	—	0.5	—	—	µs
RXD Input Hold Time	t_{DH}	—	0.8	—	—	µs

Synchronous communication timing
("H" level = 4.0 V, "L" level = 1.0 V)

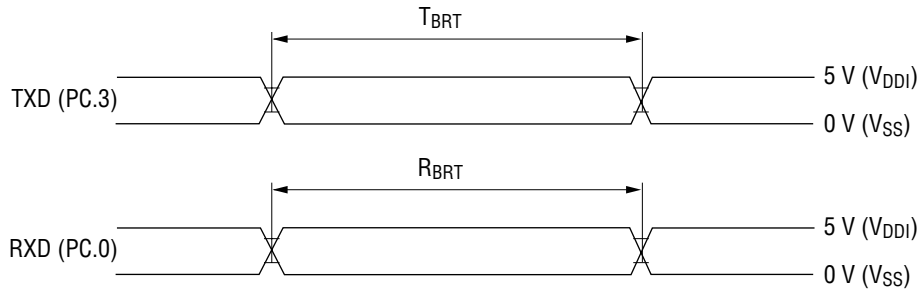


(2) UART Communication

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Transmit Baud Rate	T_{BRT}	$T_{BRT} = 1/f_{BRT}$ $T_{CR} = 1/f_{OSC}$	$T_{BRT}-T_{CR}$	T_{BRT}	$T_{BRT}+T_{CR}$	s
Receive Baud Rate	R_{BRT}	$R_{BRT} = 1/f_{BRT}$	$R_{BRT}\times0.97$	R_{BRT}	$R_{BRT}\times1.03$	s

f_{BRT}: Baud rates (1200, 2400, 4800, 9600 bps)

UART communication timing
("H" level = 4.0 V, "L" level = 1.0 V)



AC Characteristics (External Memory Interface)

(V_{DD} = V_{DDR} = 0.9 to 5.5 V, V_{DDH} = 1.8 to 5.5 V, V_{SS} = 0 V, V_{DDI} = 5.0 V, Ta = –20 to +70°C unless otherwise specified)

(1) Reading from External Memory

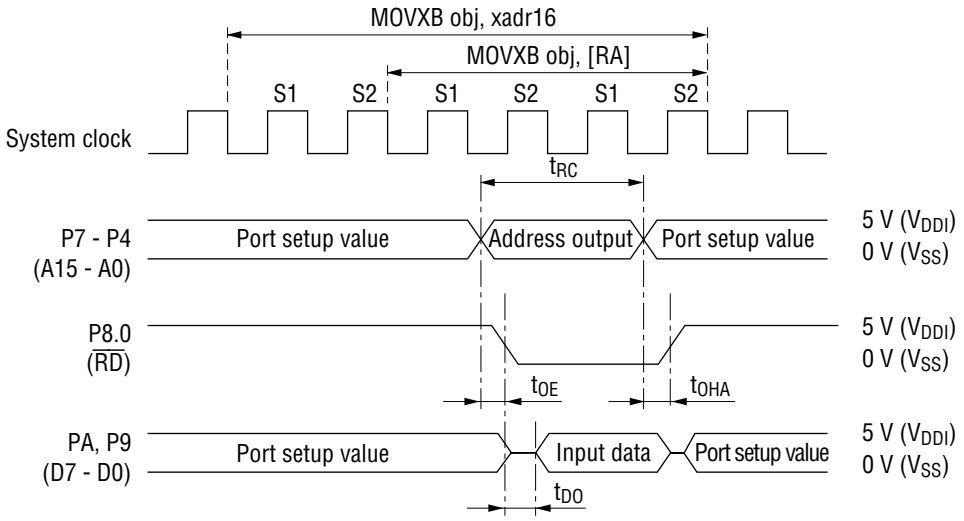
(a) When CPU operates at 32.768 kHz

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Read Cycle Time	t_{RC}	—	—	61.0	—	µs
$\overline{RD}$ Output Delay Time	t_{OE}	—	—	—	5.0	µs
Output Valid Time	t_{OHA}	—	—	—	5.0	µs
External Memory Output Delay Time	t_{DO}	—	—	—	5.0	µs

(b) When CPU operates at 2 MHz (V_{DDH} = 2.7 to 5.5 V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Read Cycle Time	t_{RC}	—	1.0	—	—	µs
$\overline{RD}$ Output Delay Time	t_{OE}	—	—	—	100	ns
Output Valid Time	t_{OHA}	—	—	—	100	ns
External Memory Output Delay Time	t_{DO}	—	—	—	150	ns

AC characteristics timing
("H" level = 4.0 V, "L" level = 1.0 V)



(2) Writing to External Memory

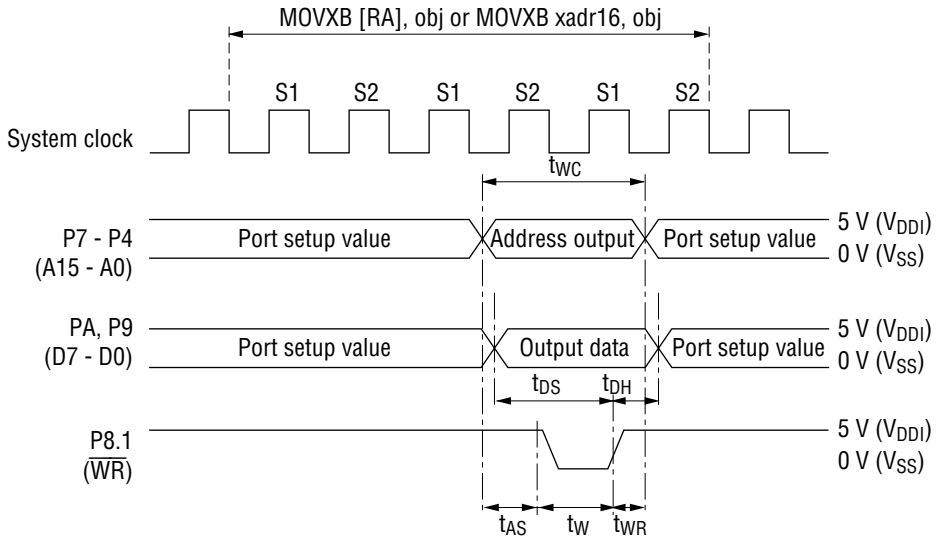
(a) When CPU operates at 32.768 kHz

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Write Cycle Time	t_{WC}	—	—	61.0	—	µs
Address Setup Time	t_{AS}	—	—	30.5	—	µs
Write Time	t_{W}	—	—	15.3	—	µs
Write Recovery Time	t_{WR}	—	—	15.3	—	µs
Data Setup Time	t_{DS}	—	—	45.8	—	µs
Data Hold Time	t_{DH}	—	—	15.3	—	µs

(b) When CPU operates at 2 MHz (V_{DDH} = 2.7 to 5.5 V)

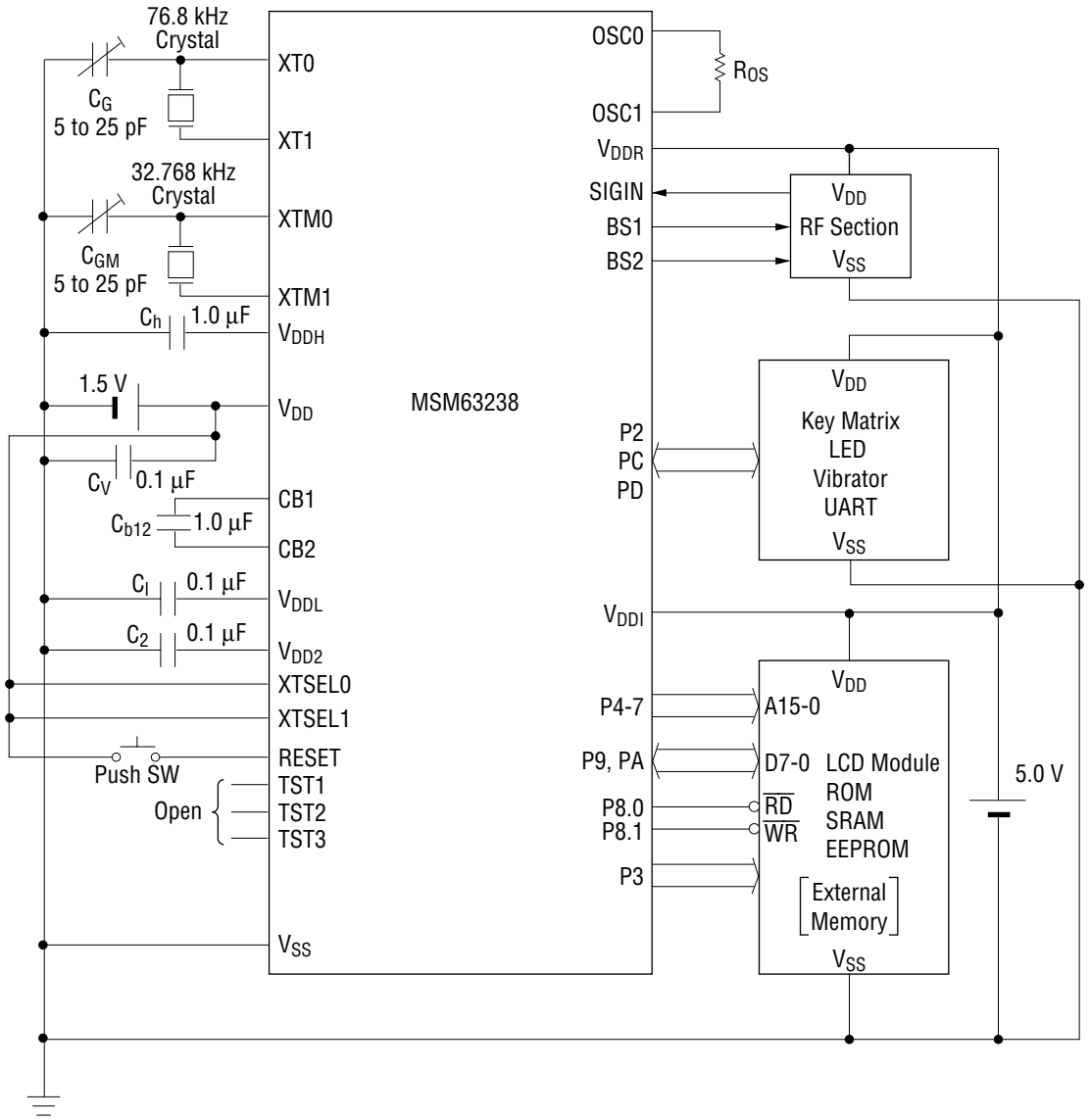
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Write Cycle Time	t_{WC}	—	1.0	—	—	µs
Address Setup Time	t_{AS}	—	0.4	—	—	µs
Write Time	t_{W}	—	0.2	—	—	µs
Write Recovery Time	t_{WR}	—	0.2	—	—	µs
Data Setup Time	t_{DS}	—	0.7	—	—	µs
Data Hold Time	t_{DH}	—	0.2	—	—	µs

AC characteristics timing
("H" level = 4.0 V, "L" level = 1.0 V)



APPLICATION CIRCUITS

- RC oscillation is selected as high-speed oscillation.
- Ports and RF section are powered from external memory power source.
- C_V is an IC power supply bypass capacitor.
- Values of C_I, C_2, C_G, C_{GM}, C_h, C_{b12}, and C_V are for reference only.

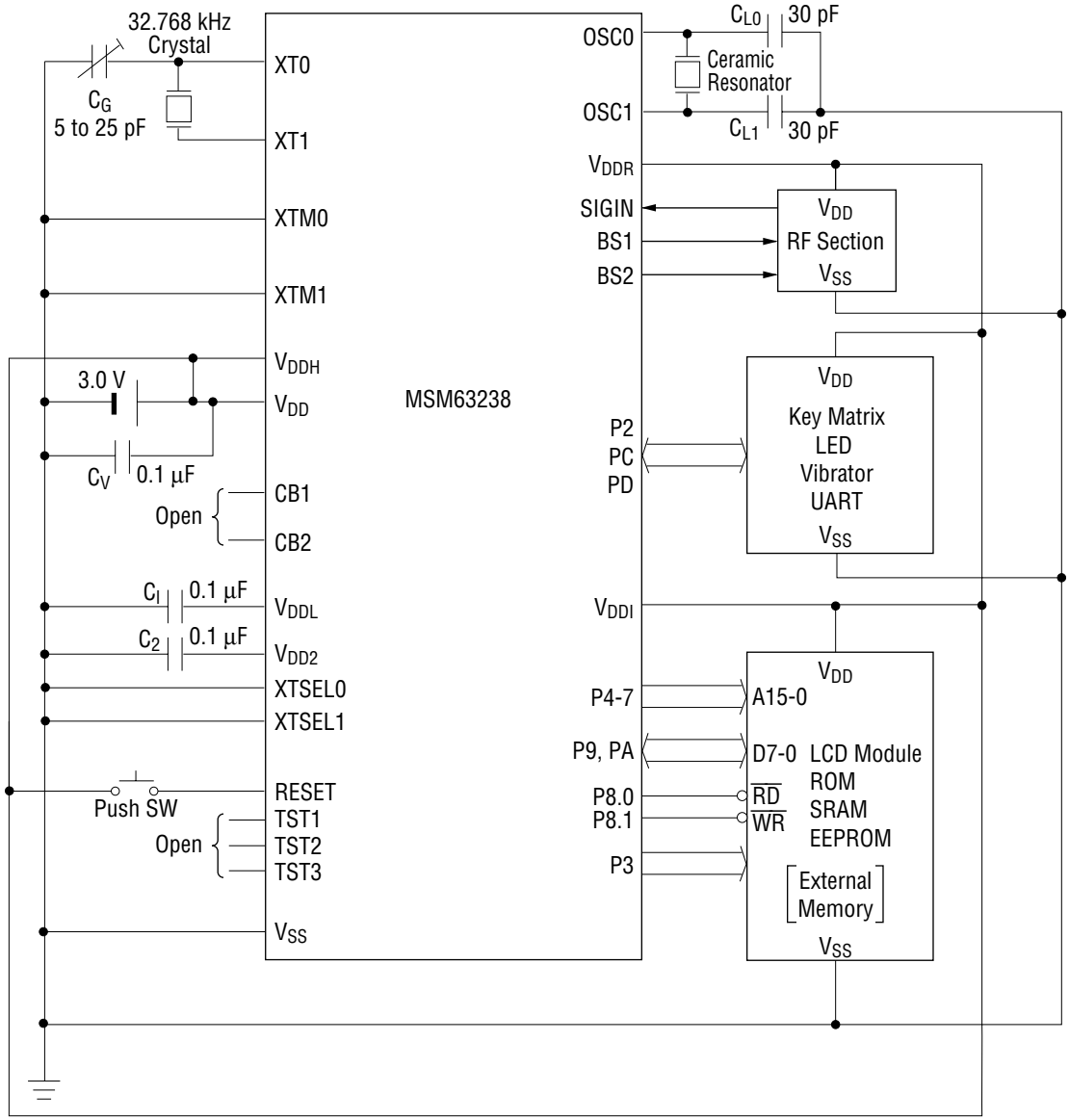


Note: V_{DDI} is the power supply pin for the input, output, and input-output ports. V_{DDR} is the interface power supply pin for SIGIN, BS1, and BS2.
Be sure to connect the V_{DDI} and V_{DDR} pins either to the positive power supply pin (V_{DD}) of this device or to the positive power supply pin of the external memory.

Application Circuit Example with Power Supply Backup

APPLICATION CIRCUITS (continued)

- Ceramic oscillation is selected as high-speed oscillation.
- Ports and RF section are powered from external memory power source.
- C_V is an IC power supply bypass capacitor.
- Values of C_I, C_2, C_G, C_V, C_{L0}, and C_{L1} are for reference only.



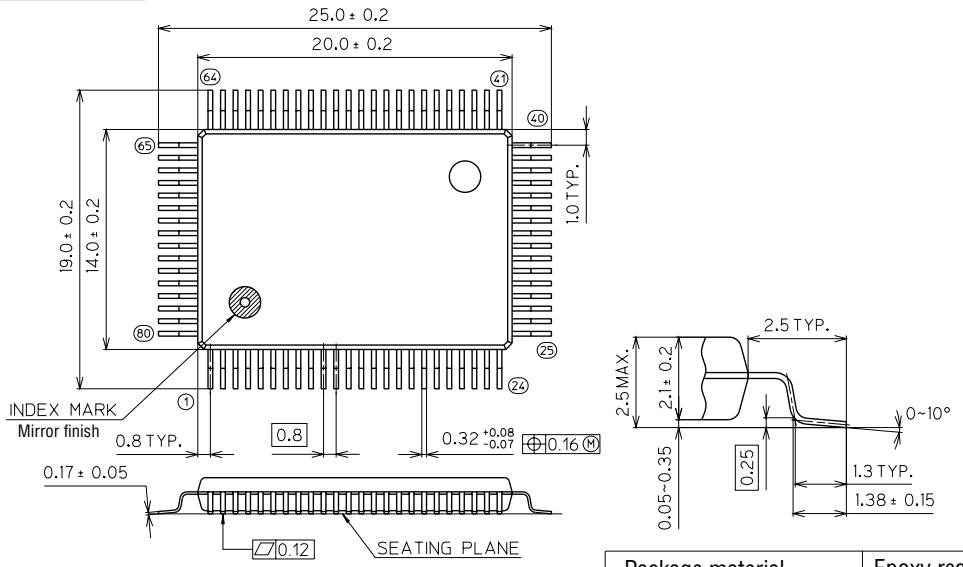
Note: V_{DDI} is the power supply pin for the input, output, and input-output ports. V_{DDR} is the interface power supply pin for SIGIN, BS1, and BS2.
Be sure to connect the V_{DDI} and V_{DDR} pins either to the positive power supply pin (V_{DD}) of this device or to the positive power supply pin of the external memory.

Application Circuit Example with No Power Supply Backup

PACKAGE DIMENSIONS

(Unit : mm)

QFP80-P-1420-0.80-BK



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	1.27 TYP.

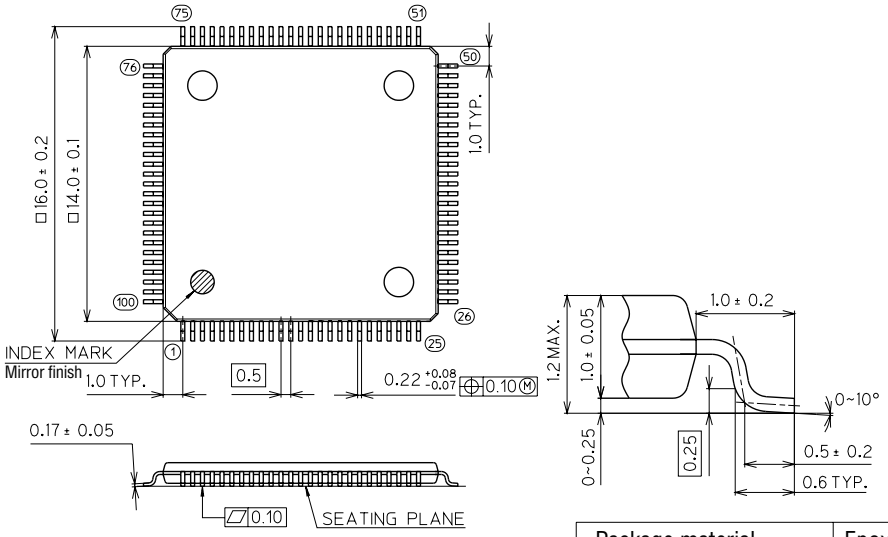
Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

PACKAGE DIMENSIONS

(Unit : mm)

TQFP100-P-1414-0.50-K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	0.55 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).