FAIRCHILD SEMICONDUCTOR™

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MM74C905
12-Bit Successive Approximation Register

General Description

The MM74C905 CMOS 12-bit successive approximation register contains all the digit control and storage necessary for successive approximation analog-to-digital conversion. Because of the unique capability of CMOS to switch to each supply rail without any offset voltage, it can also be used in digital systems as the control and storage element in repetitive routines.

Features

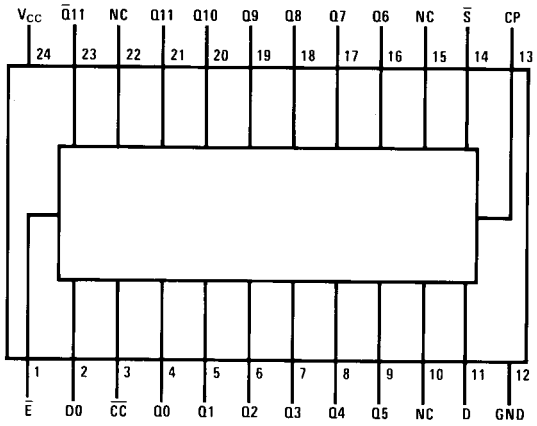
- Wide supply voltage range: 3.0V to 15V
- Guaranteed noise margin: 1.0V
- High noise immunity: 0.45 V_{CC} (typ)
- Low power TTL compatibility: Fan out of 2 driving 74L
- Provision for register extension or truncation
- Operates in START/STOP or continuous conversion mode
- Drive ladder switches directly. For 10 bits or less with 50k/100k R/2R ladder network

Ordering Code:

Order Number	Package Number	Package Description
MM74C905N	N24A	24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-010, 0.600" Wide

Connection Diagram

Pin Assignments for DIP



Truth Table

Time	Inputs			Outputs													
t_n	D	$\overline{S}$	$\overline{E}$	D0	Q11	Q10	Q9	Q8	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	$\overline{CC}$
0	X	L	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X
1	D11	H	L	X	L	H	H	H	H	H	H	H	H	H	H	H	H
2	D10	H	L	D11	D11	L	H	H	H	H	H	H	H	H	H	H	H
3	D9	H	L	D10	D11	D10	L	H	H	H	H	H	H	H	H	H	H
4	D8	H	L	D9	D11	D10	D9	L	H	H	H	H	H	H	H	H	H
5	D7	H	L	D8	D11	D10	D9	D8	L	H	H	H	H	H	H	H	H
6	D6	H	L	D7	D11	D10	D9	D8	D7	L	H	H	H	H	H	H	H
7	D5	H	L	D6	D11	D10	D9	D8	D7	D6	L	H	H	H	H	H	H
8	D4	H	L	D5	D11	D10	D9	D8	D7	D6	D5	L	H	H	H	H	H
9	D3	H	L	D4	D11	D10	D9	D8	D7	D6	D5	D4	L	H	H	H	H
10	D2	H	L	D3	D11	D10	D9	D8	D7	D6	D5	D4	D3	L	H	H	H
11	D1	H	L	D2	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	L	H	H
12	D0	H	L	D1	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	L	H
13	X	H	L	D0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	L
14	X	X	L	X	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	L
	X	X	H	X	H	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC

H = HIGH Level
L = LOW Level
X = Don't Care
NC = No Change

Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	−0.3V to V_{CC}+0.3V
Operating Temperature Range (T_A)	−40°C to +85°C
Storage Temperature Range (T_S)	−65°C to +150°C
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Operating V_{CC} Range	3.0V to 15V
Absolute Maximum V_{CC}	16V
Lead Temperature (T_L)	
(Soldering, 10 seconds)	260°C

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

DC Electrical Characteristics

Min/Max limits apply across temperature range unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS TO CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	V_{CC} = 5.0V	3.5			V
		V_{CC} = 10V	8.0			V
$V_{IN(0)}$	Logical "0" Input Voltage	V_{CC} = 5.0V			1.5	V
		V_{CC} = 10V			2.0	V
$V_{OUT(1)}$	Logical "1" Output Voltage	V_{CC} = 5.0V, I_O = −10 µA	4.5			V
		V_{CC} = 10V, I_O = −10 µA	9.0			V
$V_{OUT(0)}$	Logical "0" Output Voltage	V_{CC} = 5.0V, I_O = 10 µA			0.5	V
		V_{CC} = 10V, I_O = 10 µA			1.0	V
$I_{IN(1)}$	Logical "1" Input Current	V_{CC} = 15V, V_{IN} = 15V		0.005	1.0	µA
$I_{IN(0)}$	Logical "0" Input Current	V_{CC} = 15V, V_{IN} = 0V	−1.0	−0.005		µA
I_{CC}	Supply Current	V_{CC} = 15V		0.05	300	µA
CMOS/LPTTL INTERFACE						
$V_{IN(1)}$	Logical "1" Input Voltage	V_{CC} = 4.75V	V_{CC} − 1.5			V
$V_{IN(0)}$	Logical "0" Input Voltage	V_{CC} = 4.75V			0.8	V
$V_{OUT(1)}$	Logical "1" Output Voltage	V_{CC} = 4.75V, I_O = −360 µA	2.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage	V_{CC} = 4.75V, I_O = 360 µA			0.4	V
OUTPUT DRIVE (See Family Characteristics Data Sheet)						
I_{SOURCE}	Output Source Current (P-Channel)	V_{CC} = 5.0V, V_{OUT} = 0V T_A = 25°C	−1.75	−3.3		mA
I_{SOURCE}	Output Source Current (P-Channel)	V_{CC} = 10V, V_{OUT} = 0V T_A = 25°C	−8.0	−15		mA
I_{SINK}	Output Sink Current (N-Channel)	V_{CC} = 5.0V, V_{OUT} = V_{CC} T_A = 25°C	1.75	3.6		mA
I_{SINK}	Output Sink Current (N-Channel)	V_{CC} = 10V, V_{OUT} = V_{CC} T_A = 25°C V_{CC} = 10V ±5%	8.0	16		mA
R_{SOURCE}	Q11–Q0 Outputs	V_{OUT} = V_{CC} − 0.3V T_A = 25°C	150		350	Ω
R_{SINK}	Q11–Q0 Outputs	V_{CC} = 10V ±5% V_{OUT} = 0.3V T_A = 25°C	80		230	Ω

AC Electrical Characteristics (Note 2)

$T_A = 25°C$, $C_L = 50$ pF, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd}	Propagation Delay Time from Clock Input to Outputs (Q0–Q11) ($t_{pd(Q)}$)	$V_{CC} = 5.0V$		200	350	ns
		$V_{CC} = 10V$		80	150	ns
t_{pd}	Propagation Delay Time from Clock Input to D0 ($t_{pd(D0)}$)	$V_{CC} = 5.0V$		180	325	ns
		$V_{CC} = 10V$		70	125	ns
t_{pd}	Propagation Delay Time from Register Enable (E) to Output (Q11) ($t_{pd(E)}$)	$V_{CC} = 5.0V$		190	350	ns
		$V_{CC} = 10V$		75	150	ns
t_{pd}	Propagation Delay Time from Clock to CC ($t_{pd(CC)}$)	$V_{CC} = 5.0V$		190	350	ns
		$V_{CC} = 10V$		75	0.50	ns
t_S	Data Input Set-Up Time	$V_{CC} = 5.0V$	80			ns
		$V_{CC} = 10V$	30			ns
t_S	Start Input Set-Up Time	$V_{CC} = 5.0V$	80			ns
		$V_{CC} = 10V$	30			ns
t_W	Minimum Clock Pulse Width	$V_{CC} = 5.0V$	250	125		ns
		$V_{CC} = 10V$	100	50		ns
t_r, t_f	Maximum Clock Rise and Fall Time	$V_{CC} = 5.0V$			15	µs
		$V_{CC} = 10V$			5.0	µs
f_{MAX}	Maximum Clock Frequency	$V_{CC} = 5.0V$	2.0	4.0		MHz
		$V_{CC} = 10V$	5.0	10		MHz
C_{CK}	Clock Input Capacitance	Clock Input (Note 3)		10		pF
C_{IN}	Input Capacitance	Any other Input (Note 3)		5		pF
C_{PD}	Power Dissipation Capacitance	(Note 4)		100		pF

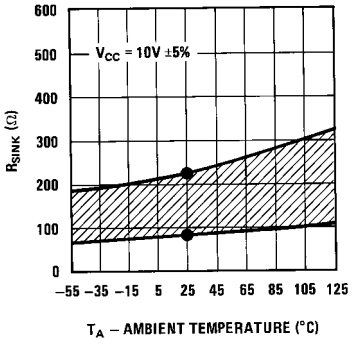
Note 2: AC Parameters are guaranteed by DC correlated testing.

Note 3: Capacitance is guaranteed by periodic testing.

Note 4: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation, see Family Characteristics Application Note—AN-90.

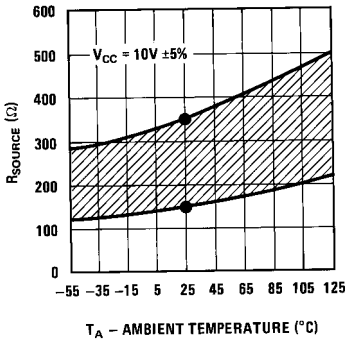
Typical Performance Characteristics

R_{SINK} vs Temperature



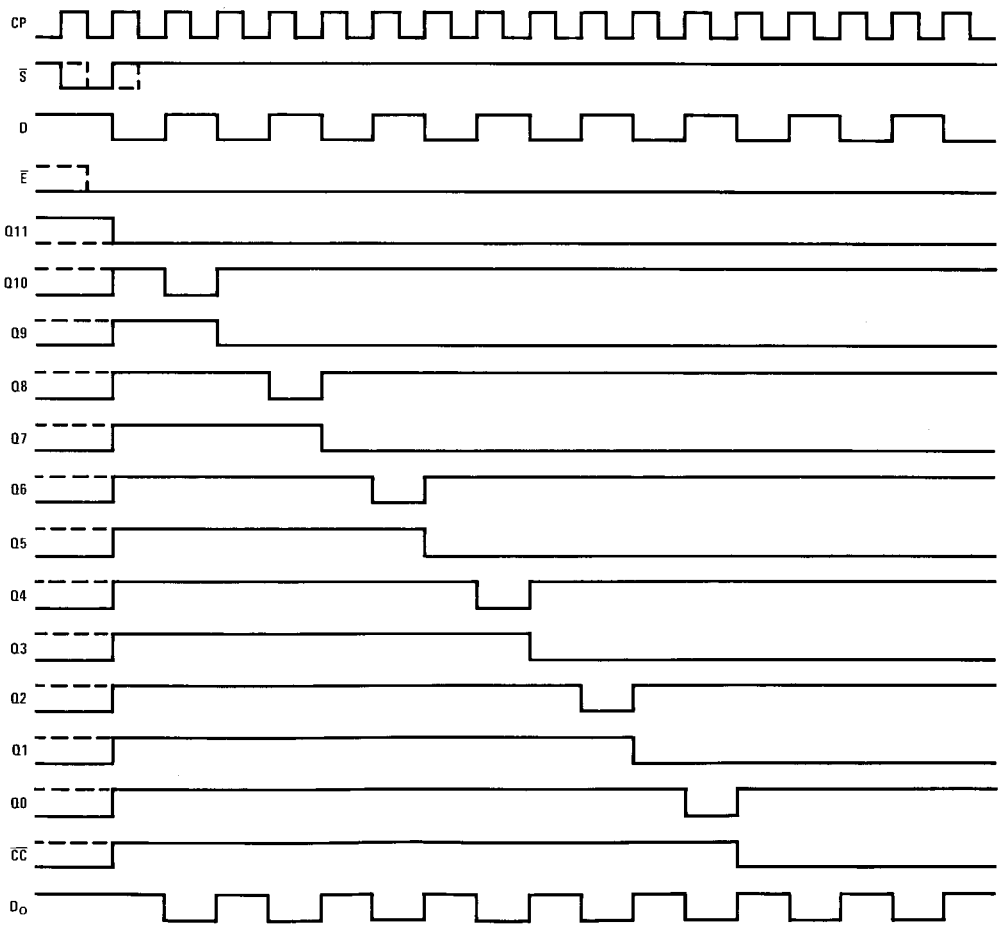
•These points are guaranteed by automatic testing.

R_{SOURCE} vs Temperature

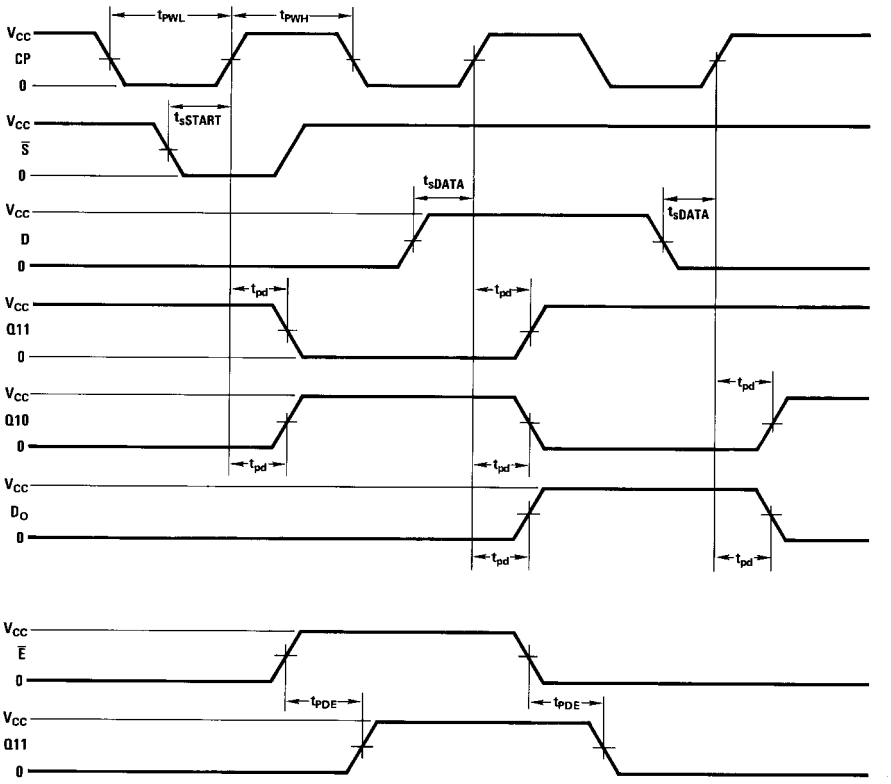


•These points are guaranteed by automatic testing.

Timing Diagram



Switching Time Waveforms



USER NOTES FOR A/D CONVERSION

The register can be used with either current switches that require a low voltage level to turn the switch ON or current switches that require a high voltage level to turn the switch ON. If current switches are used which turn ON with a low logic level, the resulting digit output from the register is active low. That is, a logic "1" is represented as a low voltage level. If current switches are used which turn ON with a high logic level, the resulting digit output is active high. A logic "1" is represented as a high voltage level.

For a maximum error of ±½ LSB, the comparator must be biased. If current switches that require a high voltage level to turn ON are used, the comparator should be biased +½ LSB and if the current switches require a low logic level to turn ON, then the comparator must be biased –½ LSB.

The register can be used to perform 2's complement conversion by offsetting the comparator one half full range +½ LSB and using the complement of the MSB Q11 as the sign bit.

If the register is truncated and operated in the continuous conversion mode, a lock-up condition may occur on power-ON. This situation can be overcome by making the START input the "OR" function of $\overline{CC}$ and the appropriate register output.

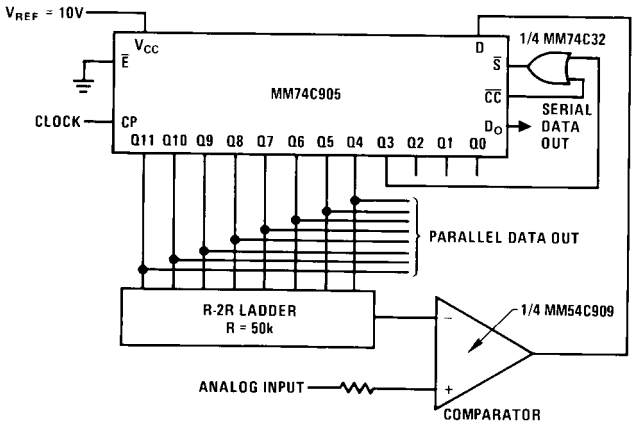
The register, by suitable selection of register ladder network, can be used to perform either binary or BCD conversion.

The register outputs can drive the 10 bits or less with 50k/100k R/2R ladder network directly for V_{CC} = 10V or higher.

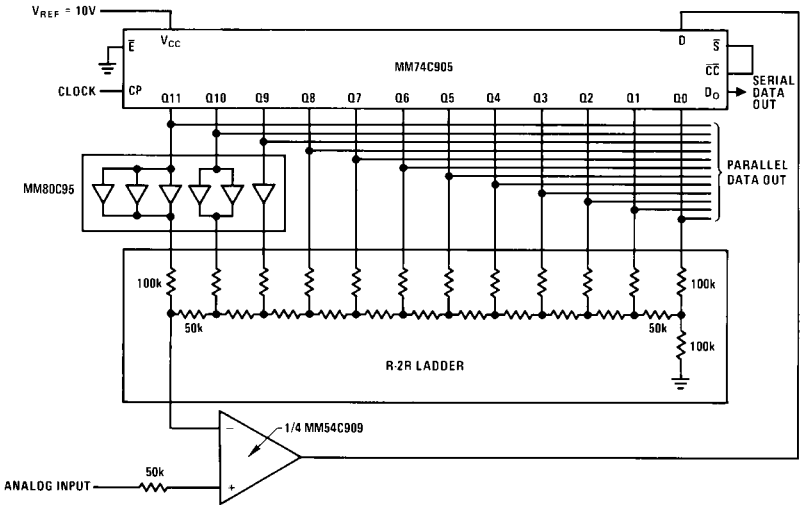
In order to drive the 12-bit 50k/100k ladder network and have the ±½ LSB resolution, the MM74C902 or MM74C904 is used as buffers, three buffers for MSB (Q11), two buffers for Q10, and one buffer for Q9.

Typical Applications

12-Bit Successive Approximation A-to-D Converter, Operating in Continuous 8–Bit Truncated Mode



12-Bit Successive Approximation A-to-D Converter, Operating in Continuous Mode, Drives the 50k/100k Ladder Network Directly



Definition of Terms

CP: Register *clock* input.

CC: *Conversion complete*—this output remains at $V_{OUT(1)}$ during a conversion and goes to $V_{OUT(0)}$ when conversion is complete.

D: Serial *data* input—connected to comparator output in A-to-D applications.

$\overline{E}$: *Register enable* —this input is used to expand the length of the register. When $\overline{E}$ is at $V_{IN(1)}$ Q11 is forced to $V_{OUT(1)}$ and inhibits conversion. When not used for expansion $\overline{E}$ must be connected to $V_{IN(0)}$ (GND).

Q11: True register MSB output.

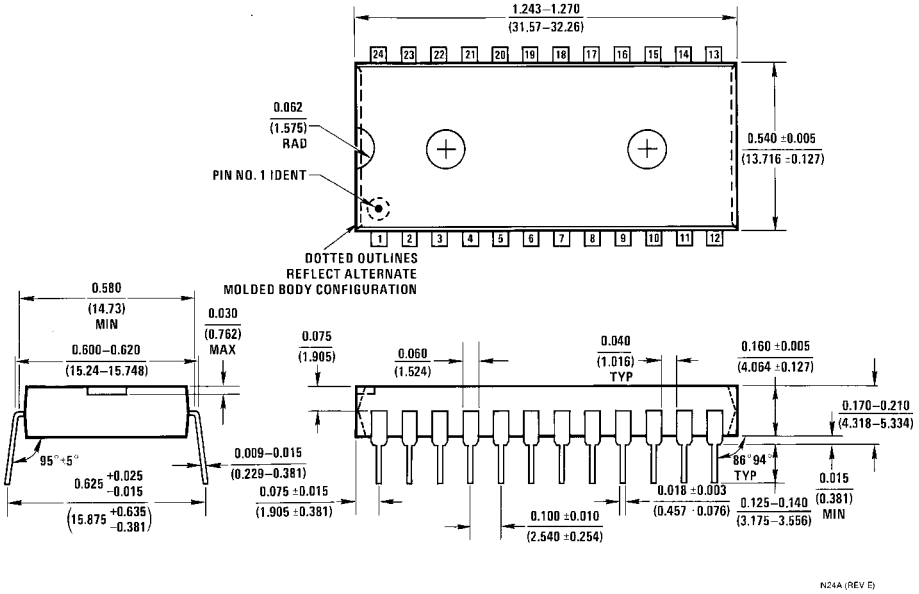
$\overline{Q}$11: Complement of register MSB output.

Qi (i = 0 to 11): Register outputs.

$\overline{S}$: *Start input*—holding start input at $V_{IN(0)}$ for at least one clock period will initiate a conversion by setting MSB (Q11) at $V_{OUT(0)}$ and all other output (Q10–Q0) at $V_{OUT(1)}$. If set-up time requirements are met, a conversion may be initiated by holding start input at $V_{IN(0)}$ for less than one clock period.

DO: *Serial data output*—D input delayed by one clock period.

Physical Dimensions inches (millimeters) unless otherwise noted



24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-010, 0.600" Wide
Package Number N24A

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