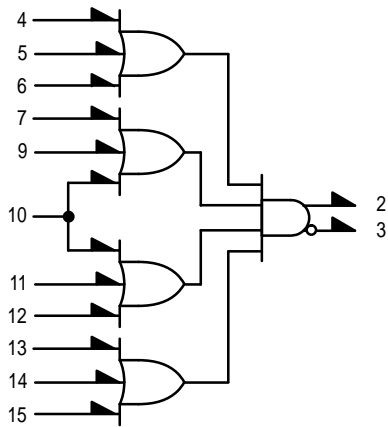


4-Wide OR-AND/OR-AND Gate

The MC10121 is a basic logic building block providing the simultaneous OR-AND/OR-AND-Invert function, useful in data control and digital multiplexing applications.

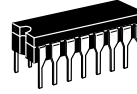
$P_D = 100 \text{ mW typ/pkg (No Load)}$
 $t_{pd} = 2.3 \text{ ns typ}$
 $t_r, t_f = 2.5 \text{ ns typ (20\%–80\%)}$

LOGIC DIAGRAM



$V_{CC1} = \text{PIN } 1$
 $V_{CC2} = \text{PIN } 16$
 $V_{EE} = \text{PIN } 8$

MC10121



L SUFFIX
CERAMIC PACKAGE
CASE 620-10

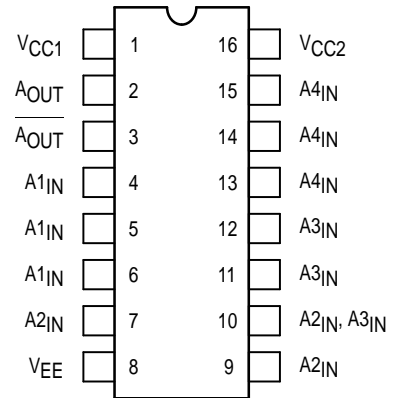


P SUFFIX
PLASTIC PACKAGE
CASE 648-08



FN SUFFIX
PLCC
CASE 775-02

DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-Line Package.
 For PLCC pin assignment, see the Pin Conversion Tables on page 6-11 of the Motorola MECL Data Book (DL122/D).



ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	Test Limits							Unit
			-30°C		+25°C			+85°C		
			Min	Max	Min	Typ	Max	Min	Max	
Power Supply Drain Current	I _E	8		29		20	26		29	mAdc
Input Current	I _{inH}	7		390			245		245	μAdc
		9		390			245		245	
		10		495			310		310	
	I _{inL}	7	0.5		0.5			0.3		μAdc
		9	0.5		0.5			0.3		
		10	0.5		0.5			0.3		
Output Voltage Logic 1	V _{OH}	3	-1.060	-0.890	-0.960		-0.810	-0.890	-0.700	Vdc
		2	-1.060	-0.890	-0.960		-0.810	-0.890	-0.700	
Output Voltage Logic 0	V _{OL}	3	-1.890	-1.675	-1.850		-1.650	-1.825	-1.615	Vdc
		2	-1.890	-1.675	-1.850		-1.650	-1.825	-1.615	
Threshold Voltage Logic 1	V _{OHA}	3	-1.080		-0.980			-0.910		Vdc
		2	-1.080		-0.980			-0.910		
Threshold Voltage Logic 0	V _{OLA}	3		-1.655			-1.630		-1.595	Vdc
		2		-1.655			-1.630		-1.595	
Switching Times (50Ω Load)										
Propagation Delay	t ₄₊₃₋	3	1.4	3.6	1.4	2.3	3.4	1.4	3.5	ns
	t ₄₋₃₊	3	1.4	3.6	1.4	2.3	3.4	1.4	3.5	
	t ₄₊₂₊	2	1.4	3.6	1.4	2.3	3.4	1.4	3.5	
	t ₄₋₂₋	2	1.4	3.6	1.4	2.3	3.4	1.4	3.5	
Rise Time (20 to 80%)	t ₃₊	3	0.9	4.1	1.1	2.5	4.0	1.1	4.6	
	t ₂₊	2	0.9	4.1	1.1	2.5	4.0	1.1	4.6	
Fall Time (20 to 80%)	t ₃₋	3	0.9	4.1	1.1	2.5	4.0	1.1	4.6	
	t ₂₋	2	0.9	4.1	1.1	2.5	4.0	1.1	4.6	

ELECTRICAL CHARACTERISTICS (continued)

			TEST VOLTAGE VALUES (Volts)					(V _{CC}) Gnd	
			V _{IHmax}	V _{ILmin}	V _{IHAmin}	V _{ILAmax}	V _{EE}		
@ Test Temperature									
-30°C			-0.890	-1.890	-1.205	-1.500	-5.2		
+25°C			-0.810	-1.850	-1.105	-1.475	-5.2		
+85°C			-0.700	-1.825	-1.035	-1.440	-5.2		
Characteristic	Symbol	Pin Under Test	TEST VOLTAGE APPLIED TO PINS LISTED BELOW						
			V _{IHmax}	V _{ILmin}	V _{IHAmin}	V _{ILAmax}	V _{EE}		
Power Supply Drain Current	I _E	8					8	1, 16	
Input Current	I _{inH}	7	7				8	1, 16	
		9	9				8	1, 16	
		10	10				8	1, 16	
	I _{inL}	7		7			8	1, 16	
		9		9			8	1, 16	
		10		10			8	1, 16	
Output Voltage	Logic 1	V _{OH}	3				8	1, 16	
		2	4, 10, 13				8	1, 16	
Output Voltage	Logic 0	V _{OL}	3				8	1, 16	
		2	4, 10, 13				8	1, 16	
Threshold Voltage	Logic 1	V _{OHA}	3				4	8	1, 16
		2	10, 13		4	4	8	1, 16	
Threshold Voltage	Logic 0	V _{OLA}	3				4	8	1, 16
		2	10, 13		4	4	8	1, 16	
Switching Times	(50Ω Load)		+1.11V			Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t ₄₊₃₋ t ₄₋₃₊ t ₄₊₂₊ t ₄₋₂₋	3	10, 13			4	3	8	1, 16
		3	10, 13			4	3	8	1, 16
		2	10, 13			4	2	8	1, 16
		2	10, 13			4	2	8	1, 16
Rise Time	(20 to 80%)	t ₃₊	3	10, 13		4	3	8	1, 16
		t ₂₊	2	10, 13		4	2	8	1, 16
Fall Time	(20 to 80%)	t ₃₋	3	10, 13		4	3	8	1, 16
		t ₂₋	2	10, 13		4	2	8	1, 16

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

OUTLINE DIMENSIONS

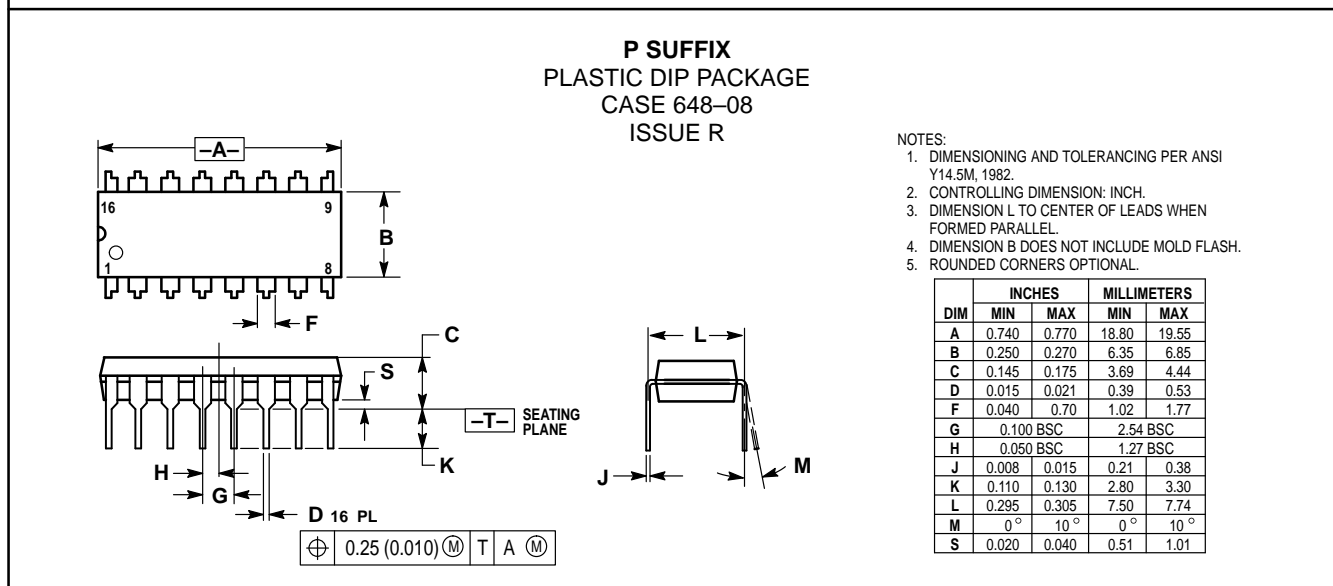
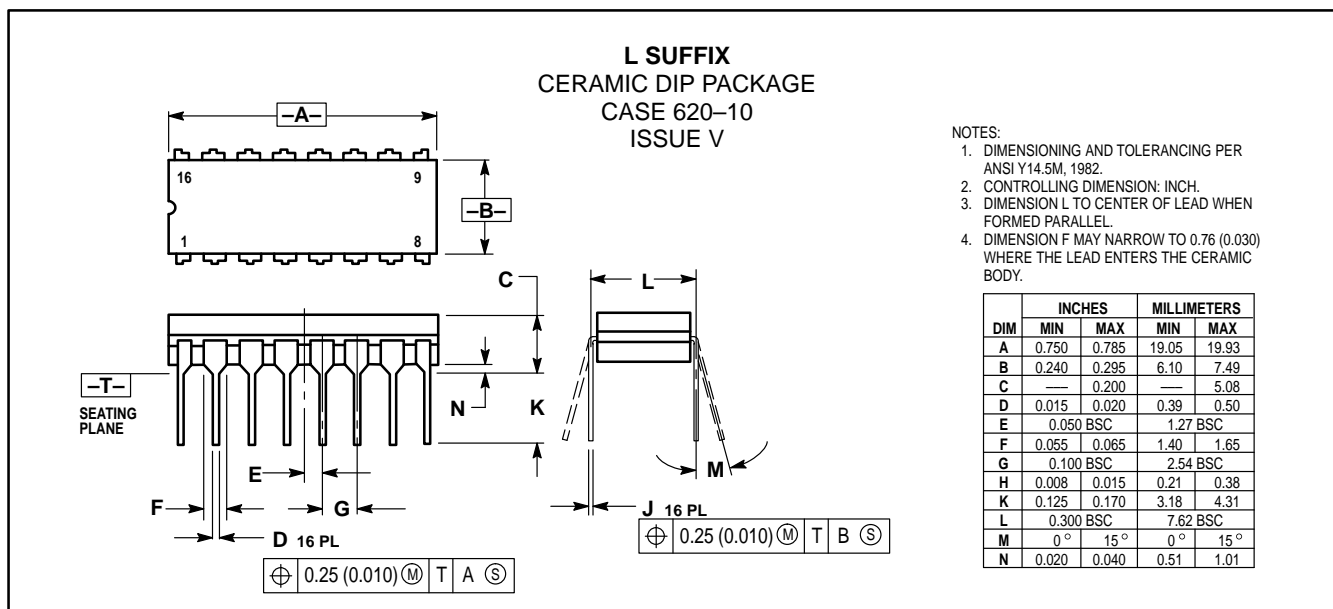
FN SUFFIX
PLASTIC PLCC PACKAGE
CASE 775-02
ISSUE C




- NOTES:
- DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
 - DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
 - DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
 - DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 - CONTROLLING DIMENSION: INCH.
 - THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
 - DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.385	0.395	9.78	10.03
B	0.385	0.395	9.78	10.03
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	—	0.51	—
K	0.025	—	0.64	—
R	0.350	0.356	8.89	9.04
U	0.350	0.356	8.89	9.04
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	—	0.020	—	0.50
Z	2°	10°	2°	10°
G1	0.310	0.330	7.88	8.38
K1	0.040	—	1.02	—

OUTLINE DIMENSIONS



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How to reach us:

USA/EUROPE/Locations Not Listed: Motorola Literature Distribution;
P.O. Box 5405, Denver, Colorado 80217. 303-675-2140 or 1-800-441-2447

Mfax™: RMFAX0@email.sps.mot.com – TOUCHTONE 602-244-6609
INTERNET: <http://Design-NET.com>

JAPAN: Nippon Motorola Ltd.; Tatsumi-SPD-JLDC, 6F Seibu-Butsuryu-Center,
3-14-2 Tatsumi Koto-Ku, Tokyo 135, Japan. 81-3-3521-8315

ASIA/PACIFIC: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park,
51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852-26629298

