HA118144AF

Video Camera CDS/AGC IC

Description

The HA118144AF is a bipolar IC that was developed to perform the analog signal processing between the CCD and the ADC in a CCD camera, and is optimal for use in CCD camera digital signal processing systems.

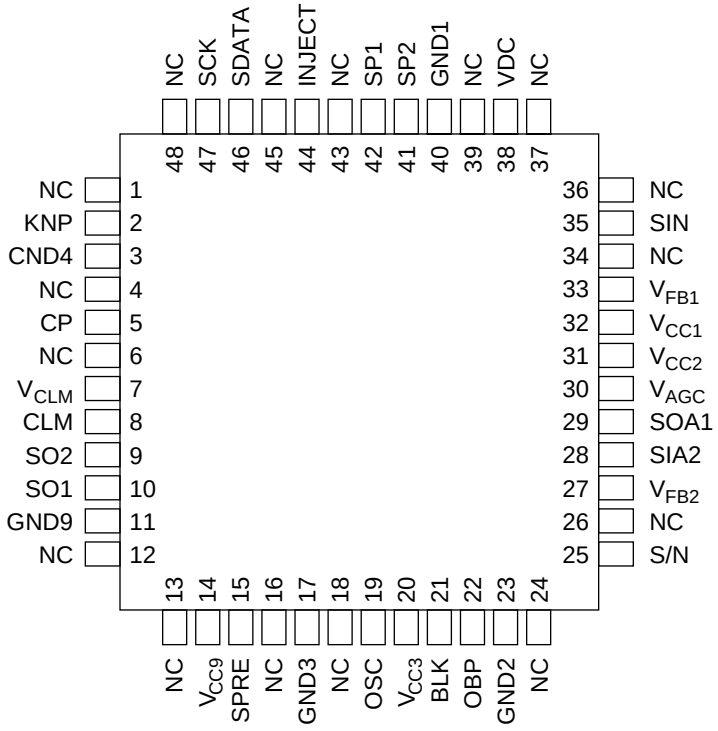
Functions

- Correlated double sampling
- AGC
- Sample and hold
- Gain select
- Knee processing
- Serial interface control

Features

- Excellent suppression of CCD output lower frequency noise by using clamp-type correlated double sampling.
- A high S/N ration by using dual (pre- and post-) AGC amplifiers and high sensitivity based on increased coverage.
- Provides compensation for IC variations and imaging device sensitivity variations with an 8 state gain select circuit.
- Allows the AGC, gain select, and knee control to be controlled from the system micro-processor over a serial interface.

Pin Arrangement



(top view)

Pin Functions

Pin No.	Pin Name	Signal	Standard DC Voltage	Signal Type	Signal Level	Impedance	Function Description
1	NC						
2	KNP	Knee pulse		Pulse	$5V_{PP}$	30 k	Knee pulse input (unused). Fix at the low level.
3	GND4	GND for IIL interface	0 V				GND = 0 V
4	NC						
5	CP	Clamp pulse		CP pulse	$5V_{PP}$	Base	Clamp pulse input (unused). Fix at the low level.
6	NC						
7	V_{CLM}	Clamp input		DC		Base	Clamp input (unused). Fix at the low level.
8	CLM	Clamp output		DC		Emitter	Clamp output (unused). Leave open.
9	SO2	Signal output 2	5.4 V	Video signal	$1.5V_{PP}$	Emitter	Signal output 2
10	SO1	Signal output 1	3.3 V	Video signal	$1.5V_{PP}$	Emitter	Signal output 1
11	GND9	GND for 9 V	0 V				GND = 0 V
12	NC						
13	NC						
14	V_{CC9}	V_{CC} for 9 V	9 V				Power supply +9 V
15	SPRE	Signal preview	1.3 V	Video signal	385 mV_{PP}	Emitter	Signal preview. For use as an output monitor.
16	NC						
17	GND3	GND for IIL	0 V				GND = 0 V
18	NC						
19	OSC	Oscillator correction	1.7 V	DC		5 k	Oscillator correction pin for the AGC DAC bias circuit. Connect to GND through a 0.1 µF capacitor.
20	V_{CC3}	V_{CC} for IIL interface	5 V				Power supply +5 V
21	BLK	Blanking pulse		BLK signal	$5V_{PP}$	Base	Blanking pulse input. The output is clipped at the BLK level when a low level is input.
22	OBP	Optical black pulse		OBP signal	$5V_{PP}$	40 k	Optical black pulse input. The feedback clamp operates when a high level is input.

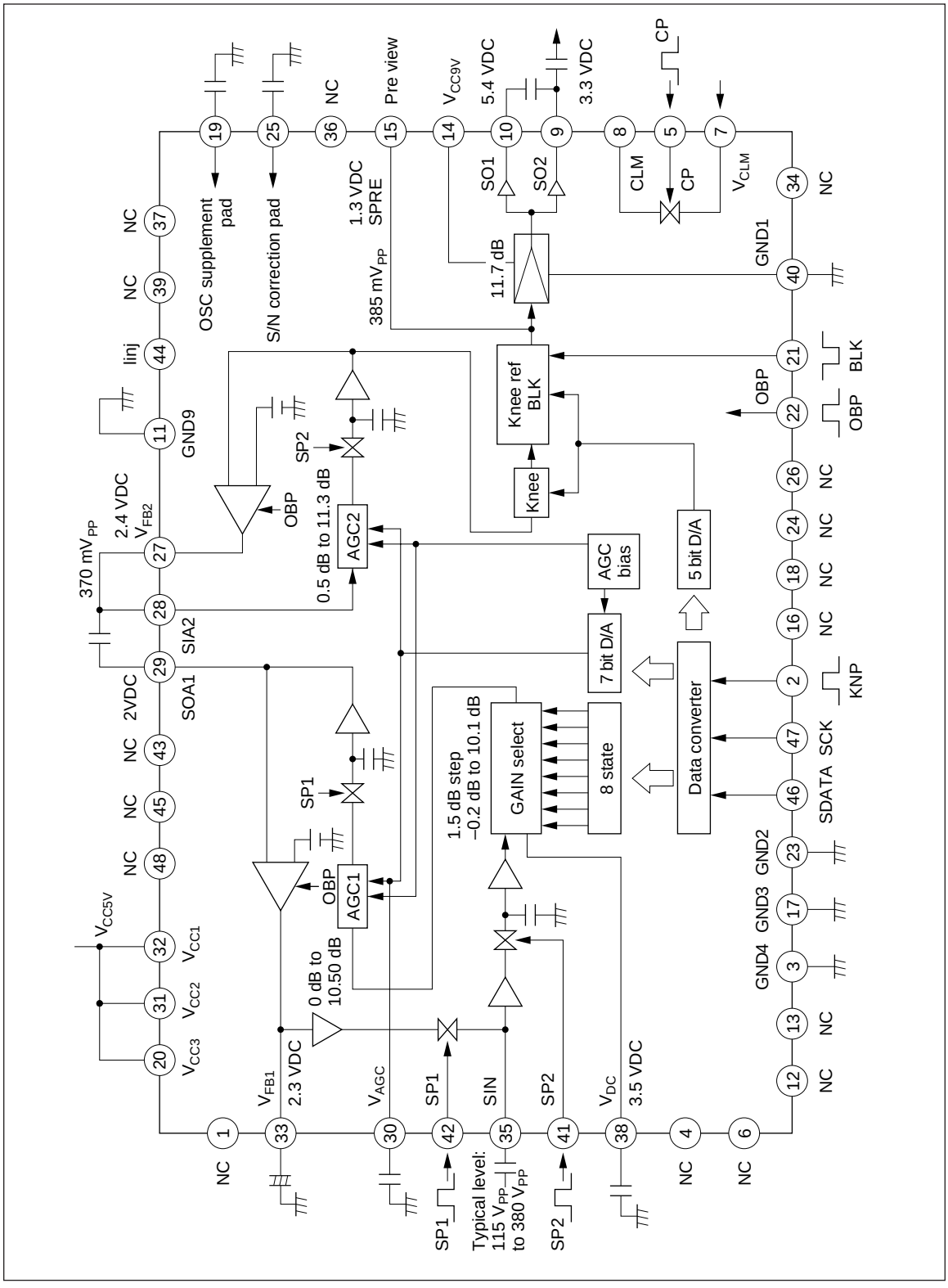
Pin Functions (cont)

Pin No.	Pin Name	Signal	Standard DC Voltage	Signal Type	Signal Level	Impedance	Function Description
23	GND2	GND for AGC, knee, BLK, DAC	0 V				GND = 0 V
24	NC						
25	S/N	S/N correction	3.1 V	DC		Base	AGC 1 bias circuit noise correction pin. Connect to GND through a 0.1 µF capacitor.
26	NC						
27	V_{FB2}	AGC2 feed back out	2.4 V	DC		Collector	AGC2 feedback output. Connect to SIA2.
28	SIA2	AGC2 input	2.4 V	Video signal	370 mV_{PP}	Base	AGC2 input. Connect to SOA1 through a 0.1 µF capacitor.
29	SOA1	AGC1 output	2 V	Video signal	370 mV_{PP}	Emitter	AGC1 output. Connect to SIA2 through a 0.1 µF capacitor.
30	V_{AGC}	AGC1 control out	2.5 V to 3.3 V	DC		Diode	AGC control voltage output. Connect to GND through a 0.1 µF capacitor.
31	V_{CC2}	V_{CC} for AGC, knee, BLK, DAC	5 V				Power supply +5 V
32	V_{CC1}	V_{CC} for gain select, CDS	5 V				Power supply +5 V
33	V_{FB1}	AGC1 feed back out	2.3 V	DC		Base	AGC1 feedback output. Connect to GND through a 0.1 µF capacitor.
34	NC						
35	SIN	Signal input	2.3 V	Video	115 mV_{PP} to 380 mV_{PP}	Base	Signal input from the CCD sensor
36	NC						
37	NC						
38	V_{DC}	Bias for FBC	3.5 V	DC		10 k	Gain select bias voltage output. Connect to GND through a 0.1 µF capacitor.
39	NC						
40	GND1	GND for gain select, CDS	0 V				GND = 0 V

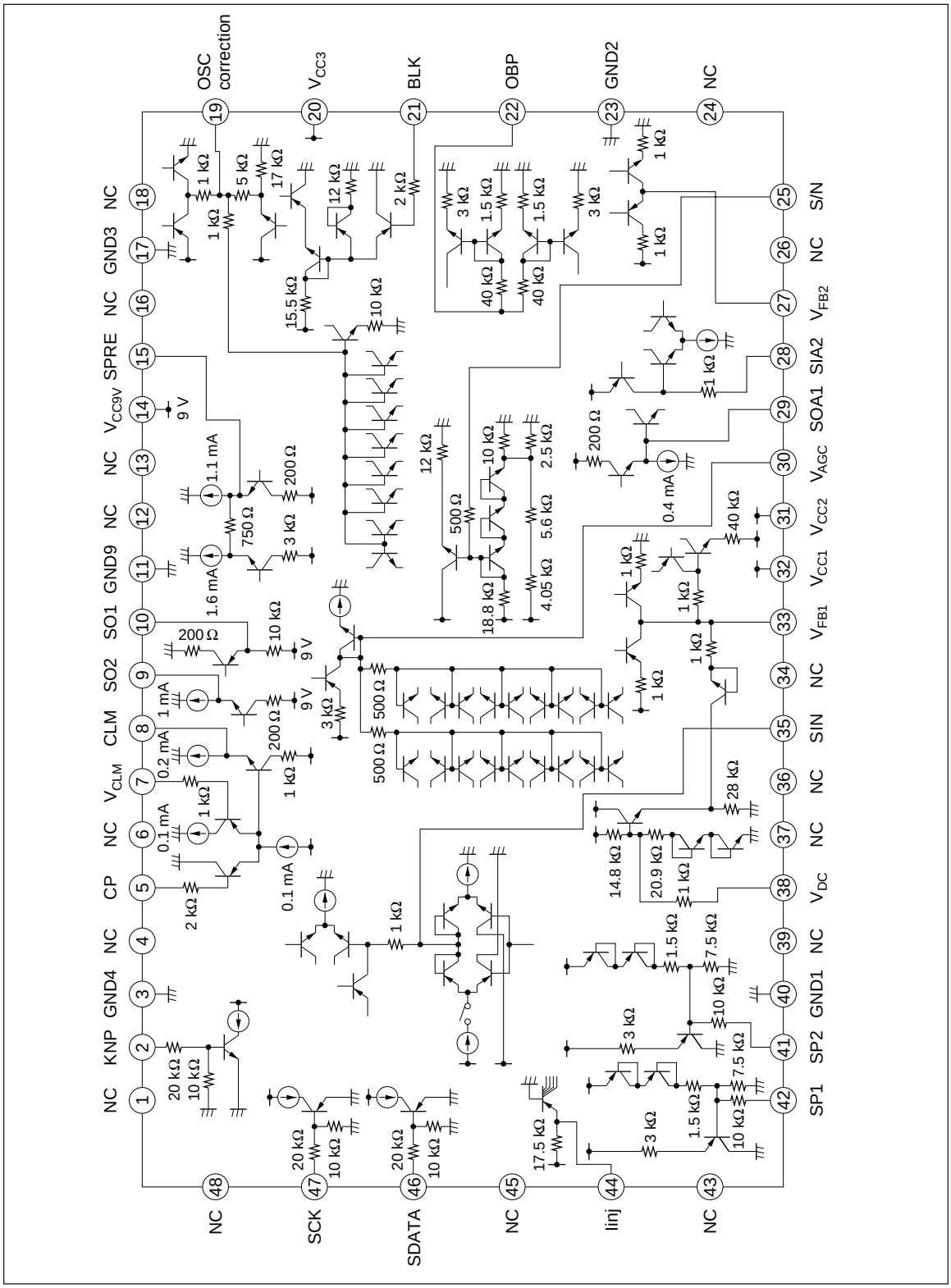
Pin Functions (cont)

Pin No.	Pin Name	Signal	Standard DC Voltage	Signal Type	Signal Level	Impedance	Function Description
41	SP2	Sample & hold pulse 2		S&H pulse	5 V_{PP}	10 k	Signal period sample and hold pulse. Duty = 25%, phase difference = 180° (with respect to SP1).
42	SP1	Sample & hold pulse 1		S&H	5 V_{PP}	10 k	Field through period clamp pulse. Duty = 25%, phase difference = 180° (with respect to SP2).
43	NC						
44	INJECT	IIL injector	0.7 V	DC	2.46 mA		Bias current pin for internal logic circuits. Leave open.
45	NC						
46	SDATA	Serial data input		Pulse	5 V_{PP}	30 k	Serial data input pin
47	SCK	Serial data clock		Pulse	5 V_{PP}	30 k	Serial clock pin. Period of 2 µs to 20 µs.
48	NC						

Block Diagram



I/O Pin Equivalent Circuits



Absolute Maximum Ratings

Item	Symbol	Rated Value	Unit
Maximum power supply voltage 1	V_{CC5} Max	6.0	V
Maximum power supply voltage 2	V_{CC9} Max	10.0	V
Operating temperature	T_{opr}	–10 to +75	°C
Storage temperature	T_{stg}	–55 to +125	°C
Operating power supply voltage 1	V_{OP5}	4.75 to 5.25	V
Operating power supply voltage 2	V_{OP9}	8.5 to 9.5	V
Power dissipation	P_T	440	mW

Notes: 1. These values are for the FQFP package mounted under the following conditions.
Substrate material: Glass epoxy
Wiring density: 40 mm□ × 1.5 mm
30%

2. This IC is for use in consumer products. It should not be used in industrial products, or in products that will be used outdoors for extended periods.

Electrical Characteristics (T_a = 25°C, V_{CC} = 5 V, 9 V)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions	Applicable Pins
Current dissipation	I_{CC} 5 V	I_{CC5}	25	36	47	mA		20, 31, 32
	I_{CC} 9 V	I_{CC9}	3.25	4.2	5.55	mA		14
FBC voltage fluctuations	VFB1 voltage fluctuation	ΔV_{FB1}	–100	0	100	mV	FBC on, $V_{VFB\ max} - V_{VFB\ min}$	33
	SIA2 voltage fluctuation	ΔS_{IA2}	–120	0	120	mV	FBC on, $V_{SIA2} - V_{SIA2\ min}$	28
Pin inflow currents	SIN pin current	I_{SIN}	–0.5	0	0.5	µA	42 pin 0 VDC	35
	VFB1 pin current 1	I_{VFB1}	–0.5	0	0.5	µA	22 pin 0 VDC	33
	VFB1 pin current 2	I_{VFB2}	60	100	140	µA	22, 41, 42 pin 5 VDC 33 pin 2.5 VDC	
	VFB1 pin current 3	I_{VFB3}	–140	–100	–60	µA	22, 41, 42 pin 5VDC 33 pin 2.5 VDC	
	SIA2 pin current	I_{SIA2}	–0.5	0	0.5	µA	22 pin 0 VDC	28
	VFB2 pin current 1	I_{VFB21}	–0.5	0	0.5	µA	22 pin 0 VDC	27
	VFB2 pin current 2	I_{VFB22}	37	50	77	µA	22, 41 pin, 5 VDC 27 pin 3 VDC	
	VFB2 pin current 3	I_{VFB23}	–75	–50	–35	µA	22, 41 pin, 5 VDC 27 pin 2 VDC	
	CP pin current	I_{CP}	–3.5	–1	0	µA	7 pin 2 VDC, 5 pin 2 VDC	5
	VCLM pin current	I_{VCLM}	–3.5	–1	0	µA	7 pin 2 VDC, 5 pin, 1 VDC	7
	CLM pin current 1	I_{CLM1}	–0.5	0	0.5	µA	7 pin 0 V, 5 pin 1 VDC, 8 pin 5 VDC	8
	CLM pin current 2	I_{CLM2}	–0.5	0	0.5	µA	7 pin 0 V, 5 pin 1 VDC, 8 pin 0 VDC	
	CLM pin current 3	I_{CLM3}	150	191	271	µA	7 pin 5 V, 5 pin 1 VDC, 8 pin 5 VDC	
	CLM pin current 4	I_{CLM4}	–5	–3	–1	µA	7 pin 5 V, 5 pin 2 VDC, 8 pin 0.7 VDC	
	OBP pin current	I_{OBP}	164	205	285	µA	22 pin 5 VDC	22
	BLK pin current	I_{BLK}	–14	–5	–2	µA	21 pin 0 VDC	21

Electrical Characteristics (T_a = 25°C, V_{CC} = 5 V, 9 V) (cont)

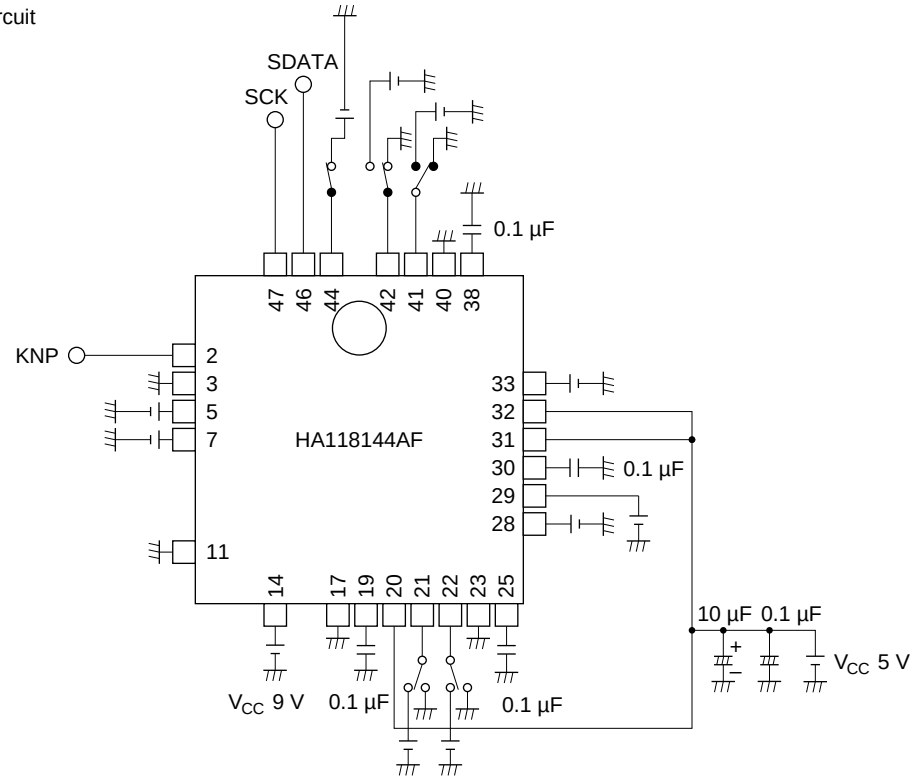
Item		Symbol	Min	Typ	Max	Unit	Test Conditions	Applicable Pins
Pin inflow currents	SDATA pin current	I_{SDATA}	8.2	10.2	12.2	µA	46 pin 0.3 VDC	46
	SCK pin current	I_{SCK}	7.9	10.4	12.1	µA	47 pin 0.3 VDC	47
	KNP pin current	I_{KNP}	8.3	10.3	12.3	µA	2 pin 0.3 VDC	2
Pin voltages	SIN pin voltage	V_{SIN}	2.5	2.8	3.1	V	41, 42 pin 5 V, 22 pin 5 V, 2 pin 0 VDC gain min	35
	VFB1 pin voltage	V_{VFB1}	2.5	2.8	3.1	V		33
	SOA1 pin voltage	V_{SOA1}	1.78	2.0	2.22	V		29
	SIA2 pin voltage	V_{SIA2}	2.2	2.4	2.6	V	41 pin 5 V, 22 pin 5 V, 21 pin 5 V, 2 pin 0 VDC gain min	28
	SPRE pin voltage	V_{SPRE}	1.2	1.4	1.6	V	41 pin 5 V, 22 pin 5 VDC, 21 pin 5 V, 2 pin 0 V, gain min	15
	SO1 pin voltage	V_{SO1}	4.95	5.25	5.65	V		10
	SO2 pin voltage	V_{SO2}	2.9	3.15	3.45	V		9
	CLM pin voltage	V_{CLM}	1.8	1.9	2.05	V	7 pin 1.9 VDC, 5 pin 5 VDC	8
	Serial input V_{TH}	SV_{TH}	2.8	—	—	V	Adjusts the pin 46 and 47 serial data amplitudes.	46, 47
AC items	Gain select 1	G_{SA1}	–0.8	–0.2	1.2	dB	22, 41, 42 pin 5 VDC AGC 1 min	33, 29
	Gain select 2	G_{SA2}	0.3	1.3	2.3	dB		
	Gain select 3	G_{SA3}	1.7	2.7	3.7	dB		
	Gain select 4	G_{SA4}	3.1	4.1	5.1	dB		
	Gain select 5	G_{SA5}	4.6	5.6	6.6	dB		
	Gain select 6	G_{SA6}	6.2	7.2	8.2	dB		
	Gain select 7	G_{SA7}	7.7	8.7	9.7	dB		
	Gain select 8	G_{SA8}	9.1	10.1	11.1	dB		
	AGC1 G (0)	G_{A01}	–1.2	–0.2	0.8	dB	22, 41, 42 pin 5 VDC gain select min	
	AGC1 G (60)	G_{A60}	–0.6	0.2	1.0	dB		
	AGC1 G (70)	G_{A70}	0.4	1.2	2.0	dB		
	AGC1 G (80)	G_{A80}	2.1	2.9	3.7	dB		
	AGC1 G (90)	G_{A90}	3.7	4.5	5.3	dB		
	AGC1 G (100)	G_{A100}	5.4	6.2	7.0	dB		
	AGC1 G (110)	G_{A110}	7.1	7.9	8.7	dB		
	AGC1 G (120)	G_{A120}	8.8	9.6	10.4	dB		
	AGC1 G (127)	G_{A127}	9.7	10.5	11.3	dB		

Electrical Characteristics (T_a = 25°C, V_{CC} = 5 V, 9 V) (cont)

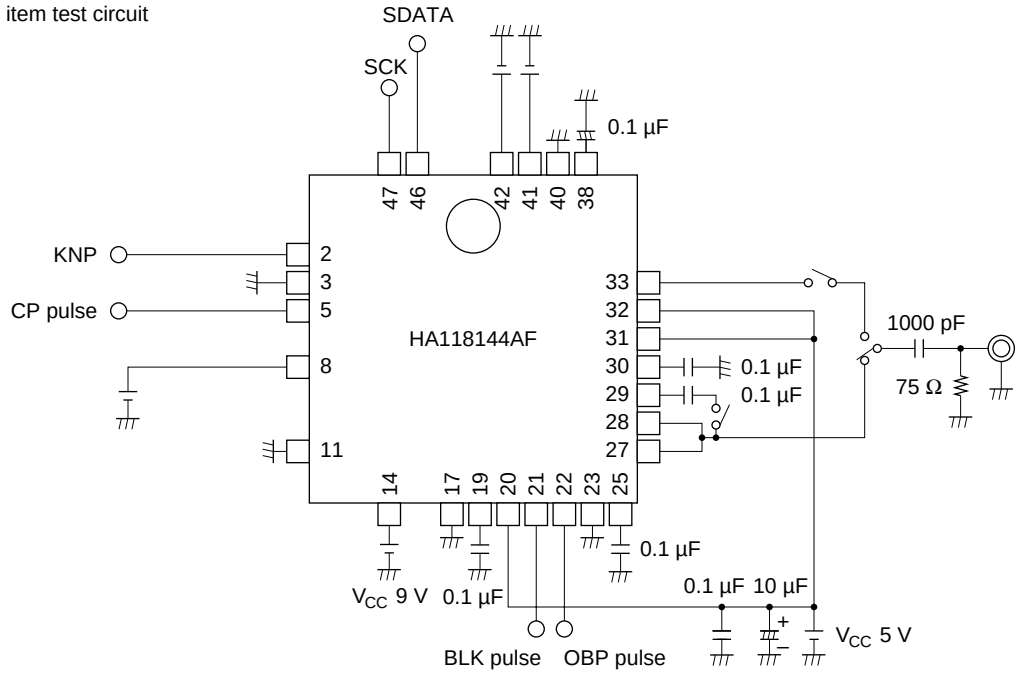
Item		Symbol	Min	Typ	Max	Units	Test Conditions	Applicable Pins
AC items	AGC2 G (0)	G_{A02}	–0.5	0.5	1.5	dB	Pins 21, 22, 41, 42: 5 VDC, Pins 27, 28: Short knee max.	28, 15
	AGC2 G (10)	G_{A10}	0.7	1.5	2.3	dB		
	AGC2 G (20)	G_{A20}	2.3	3.1	3.9	dB		
	AGC2 G (30)	G_{A30}	4.0	4.8	5.6	dB		
	AGC2 G (40)	G_{A40}	5.9	6.7	7.5	dB		
	AGC2 G (50)	G_{A50}	7.6	8.4	9.2	dB		
	AGC2 G (60)	G_{A60}	9.2	10.0	10.8	dB		
	AGC2 G (70)	G_{A70}	9.9	10.7	11.5	dB		
	SO1 gain	GS01	10.7	12.2	13.7	dB	Pins 21, 22, 41, 42: 5 VDC, Pins 27, 28: Short knee max.	28, 10
	SO2 gain	GS02	10.7	12.2	13.7	dB		28, 9
	Gain ref pulse	V_{GRP}	170	210	250	mV	Pins 41, 42: 5 VDC Pins 27, 28: Short knee max.	2, 29
	BLK level	V_{BLK}	0.5	0.6	0.7	V		21, 9
	Knee compression ratio	ΔG_{knee}	2.6	3.8	5.0	dB	41, 42 pin 5 VDC G_{knee} max–G_{knee} min	28, 15
	Knee off	Knee off	0.8	0.9	1.0	V	41, 42 pin 5 VDC knee min	
	Knee start point	Kne start	0.15	0.25	0.35	V		

Test Circuits

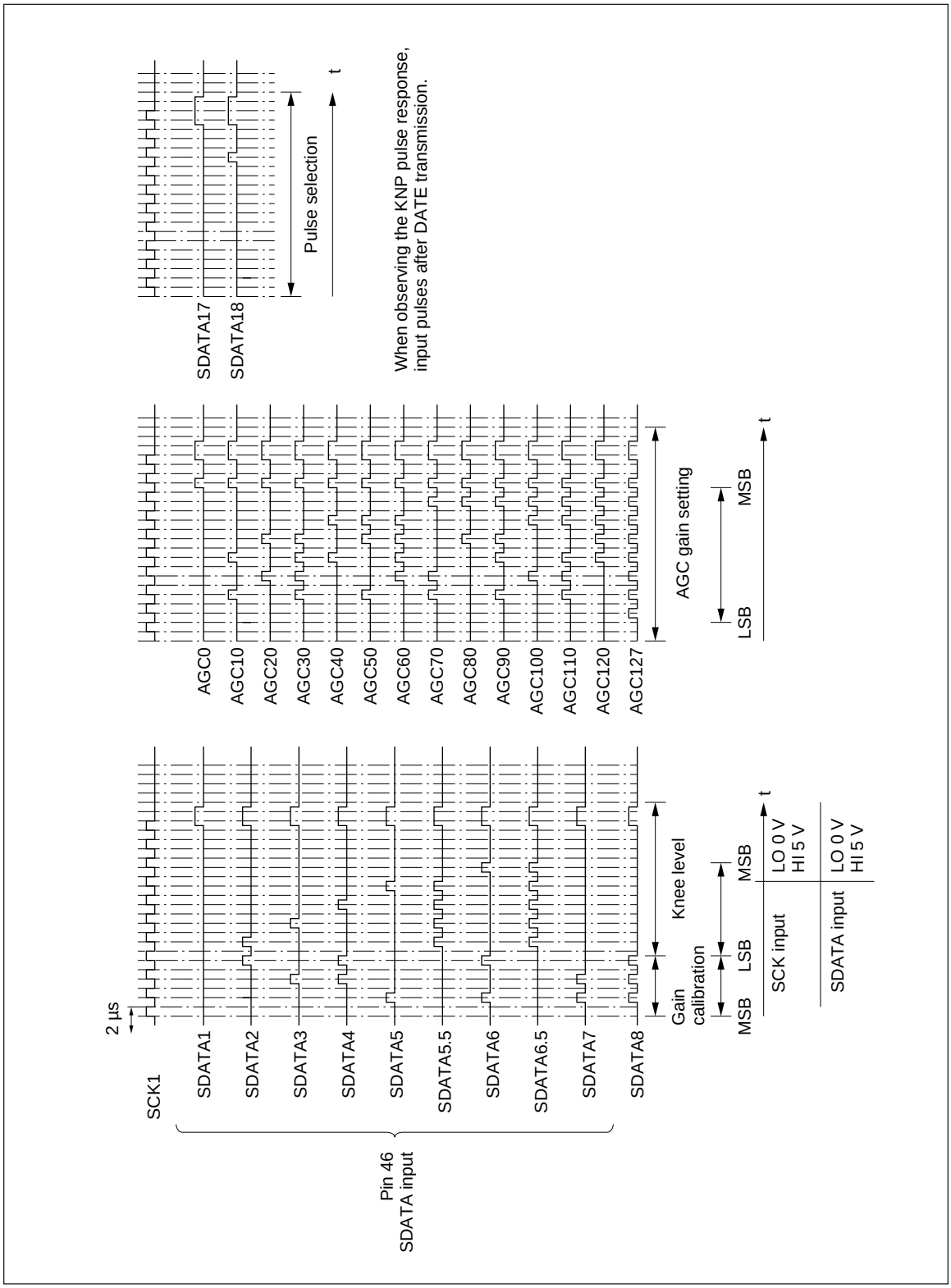
DC item test circuit



AC item test circuit

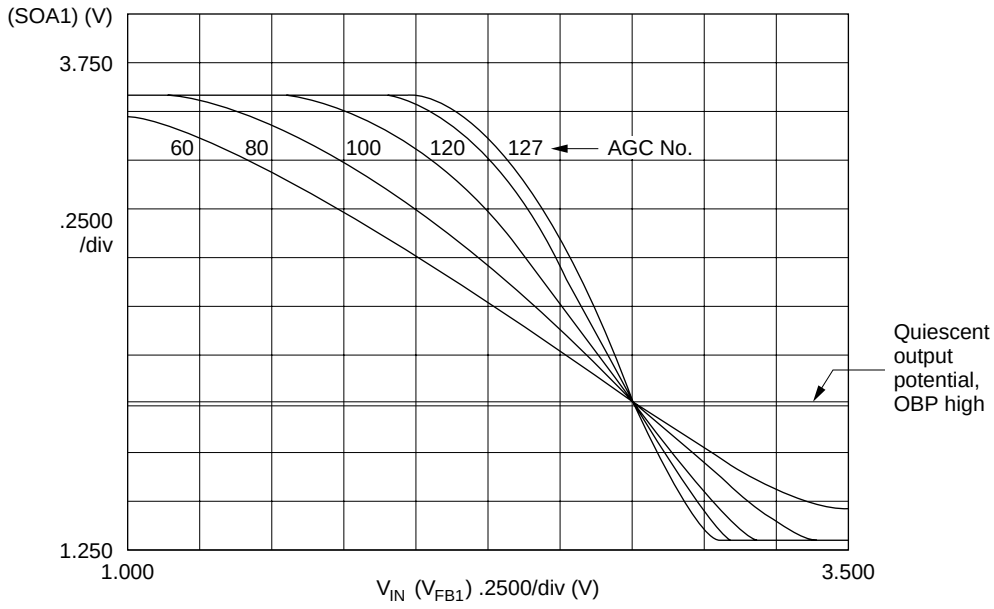


Test Patterns



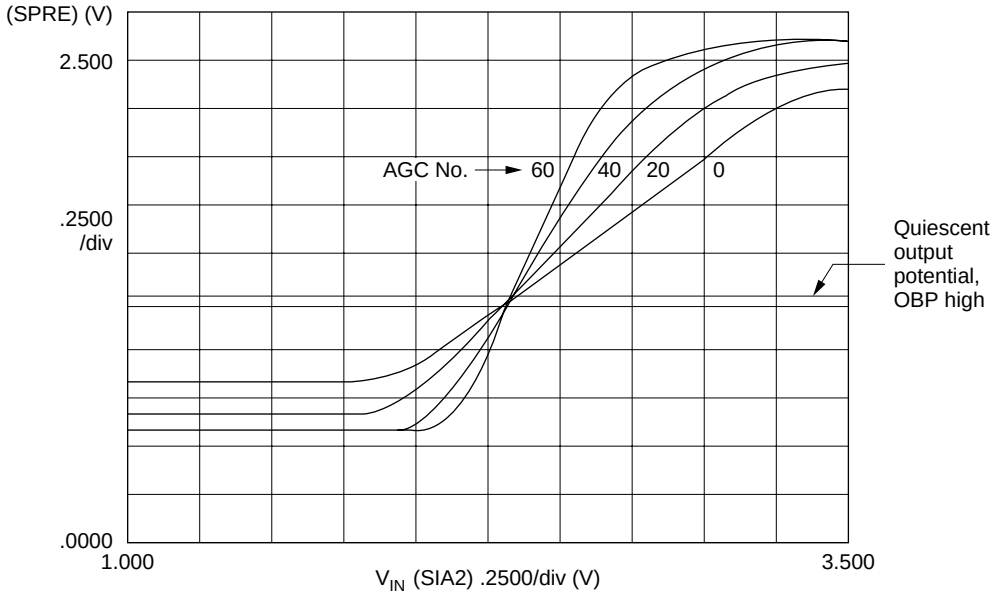
Main Characteristics

AGC1 gain I/O characteristics ($V_{FB1} \rightarrow$ SOA1)



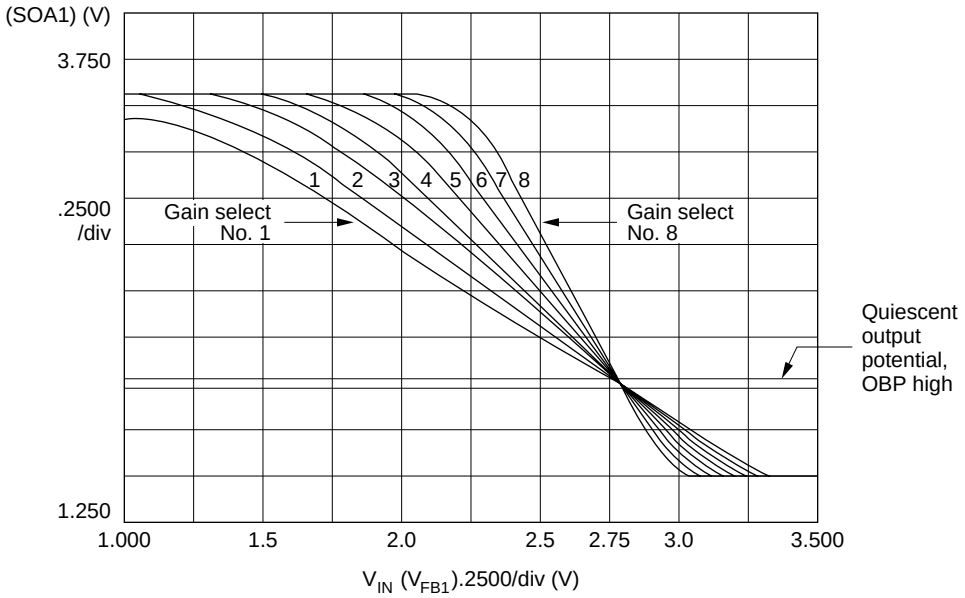
Gain select min, AGC No. 60, 80, 100, 120, 127
SP1, SP2: high, OBP: low

AGC2 gain I/O characteristics (SIA2 $\rightarrow$ SPRE)



Knee SDATA min, AGC No. 0, 20, 40, 60

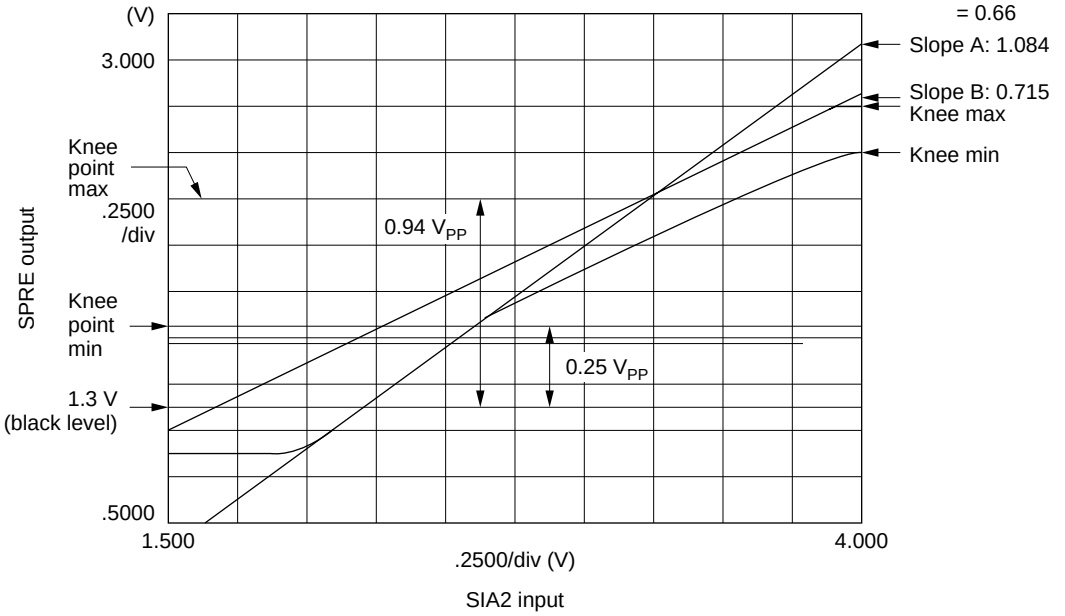
Gain select I/O characteristics ($V_{FB1} \rightarrow$ SOA1)



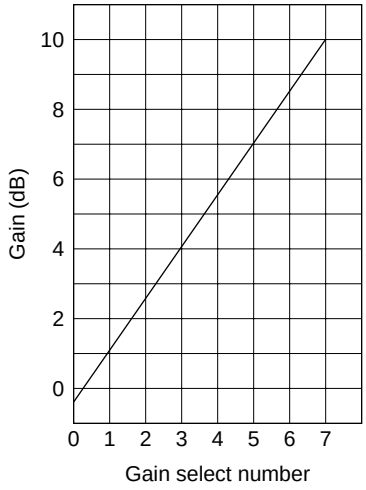
AGC gain min, gain select No. 1, 2, 3, 4, 5, 6, 7, 8
SP1, SP2: high, OBP: low

Knee I/O characteristics

Compression ratio = $\frac{\text{slope B}}{\text{slope A}}$ = 0.66

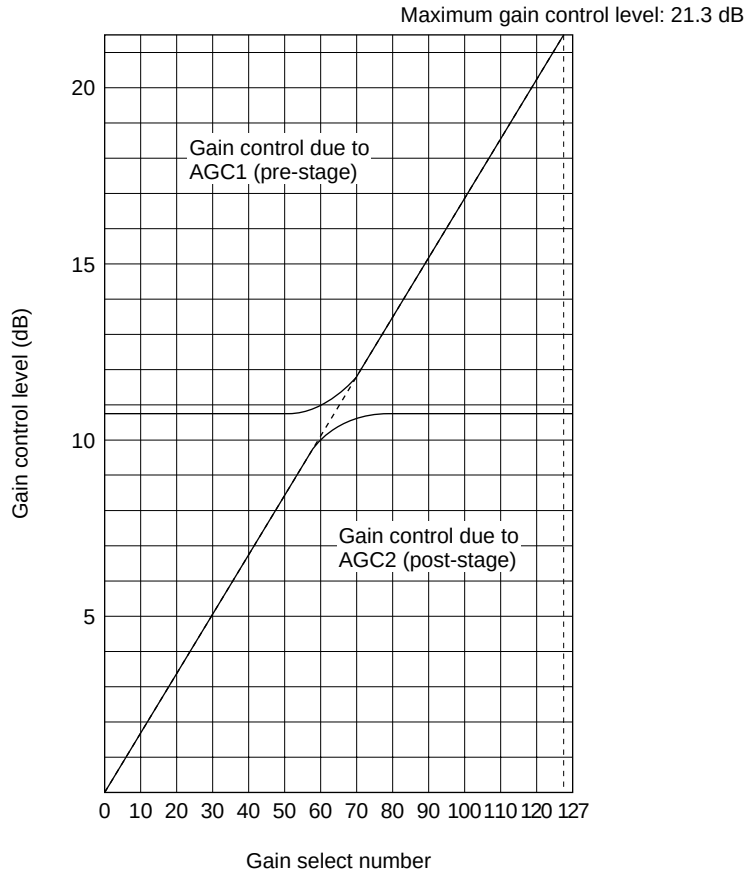


Gain select characteristics



Gain for SIN (37) → SOA1 (32) (AGC number 0)

AGC1 + AGC2 combined gain control characteristics



Built-In Functions and Timing Charts

Function Overview

- CDS (correlated double sampling) circuit
- Gain select
- AGC gain setting
- Knee level setting

Serial data control functions

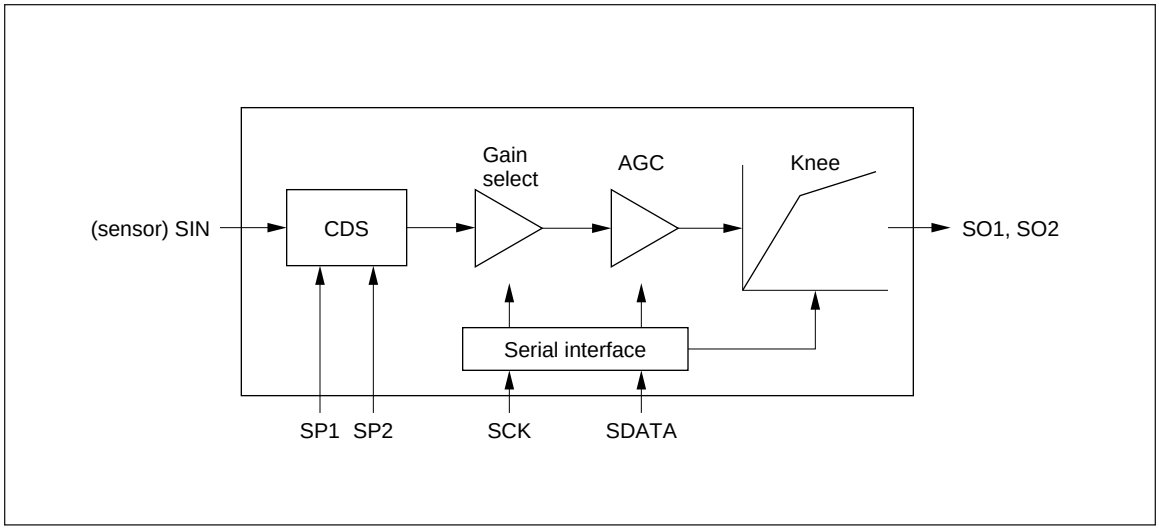


Figure 1 CDS/AGC IC Function Overview

Operation

- CDS (correlated double sampling) circuit

  A CCD image sensor alternately outputs a noise segment (the A period signal) and a signal segment (the B period signal) that includes noise. Since the main noise generated by the image sensor is low frequency noise, and that noise is added to the signal, this noise is a factor in S/N ratio degradation.

  The CDS circuit removes the low frequency noise by first clamping the image sensor output signal noise segment (the A period signal) to a fixed voltage, and then replacing the noise segment with the signal segment by sampling and holding the signal segment (B period), which includes noise. Thus the CDS circuit generates a continuous signal, and consists of a clamping circuit, and sample and hold circuit, and inverting amplifier. (See figures 2 and 3.)

— Clamp circuit (CLAMP)

  This circuit removes low frequency noise by clamping the input signal ① noise segment (A period) to a fixed voltage using the SP1 sample/hold pulse, and supplies its output signal to the sample and hold circuit. (See figures 2 and 3 ④.)

— Sample and hold circuit (S/H)

  This is a circuit that samples and holds the signal segment, and uses the SP2 sample/hold pulse to sample the signal segment (B period) and replace the noise segment with the signal segment to generate a continuous signal. (See figures 2 and 3 ⑤.)

— Following the inverting amplifier, the signal is supplied to the gain select circuit.

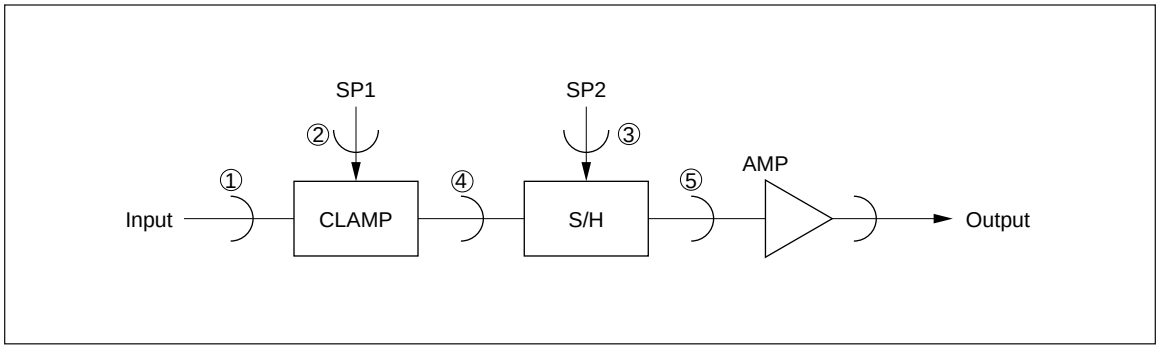


Figure 2 CDS Circuit

- Gain select

  The gain select circuit can be set to one of eight gain levels from –0.2 dB to 10.1 dB in 1.5 dB increments according to 3 bits of control data. The gain select circuit setting is used to adjust the input level to the AGC circuit in the next stage.

- AGC gain

  The AGC gain is set by 7 bits of control data. The setting range is from 0 dB to 21 dB. Internally, the circuit is divided into two stages, AGC1 (pre-stage) and AGC2 (post-stage), which together realize a variable amplification of up to 21 dB.

  The application should implement an auto-aliasing function by processing the camera DSPIC iris result in the microprocessor, and using that to control the AGC gain in this IC using serial data transfers.

- Knee level

  The amplifier I/O characteristics are shown in figure 4. The inflection point where the gain changes is determined by 5 bits of data.

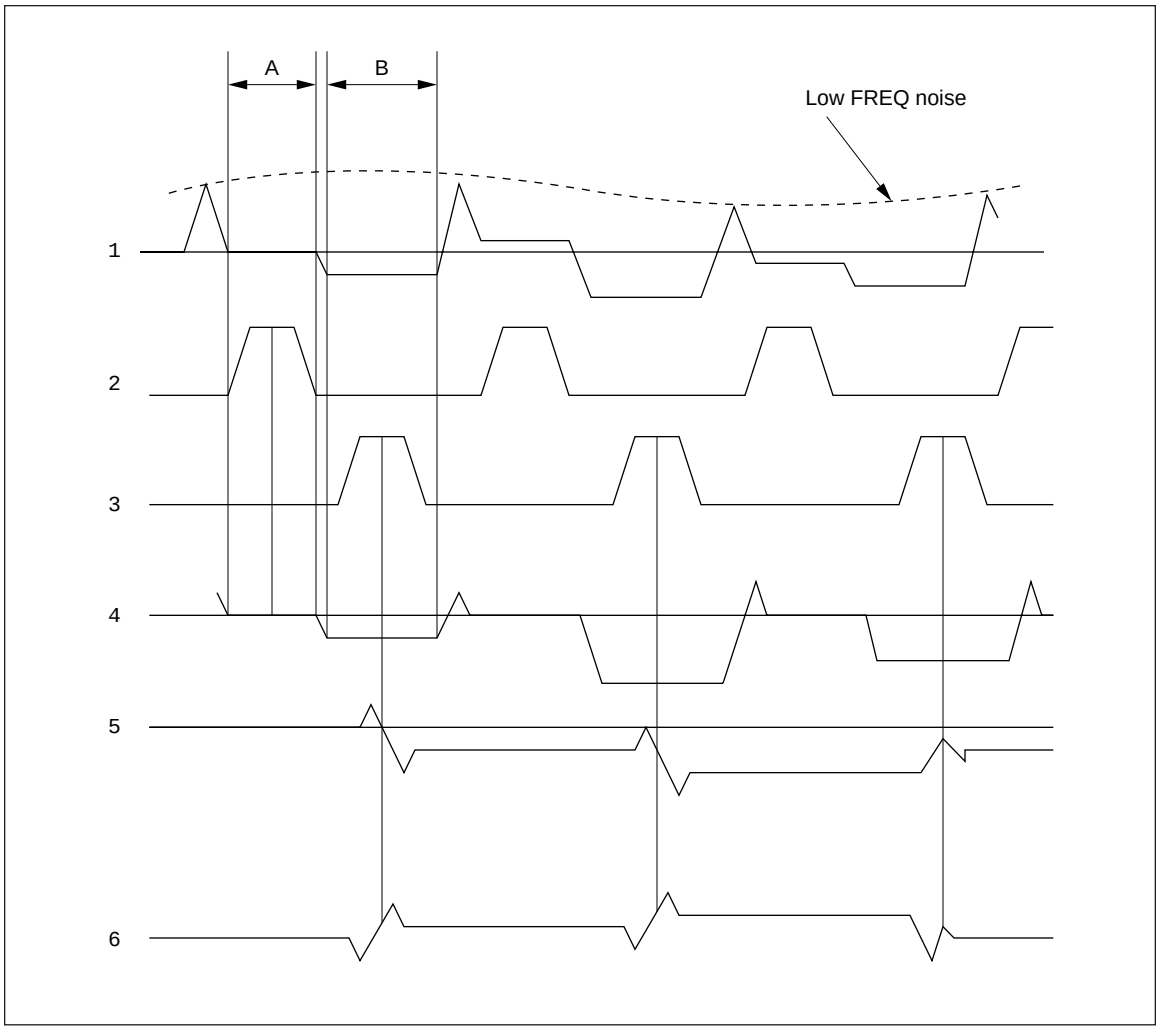


Figure 3 CDS Timing Chart

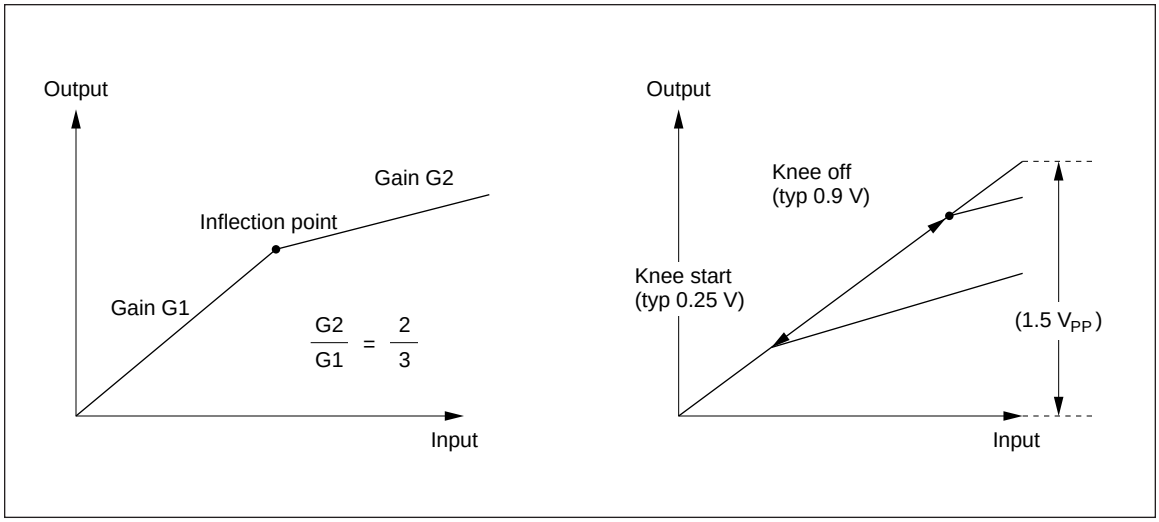


Figure 4 Knee Level Characteristics

Serial Data Control

- Timing chart
  - — Serial transfers are performed by the SCK and SDATA pins in the CDS/AGC IC.
  - — Internally, the IC takes the case where SDATA is high on the falling edge of SCK as the data latch timing.
  - — Data is acquired on the falling edge of SCK for D1 to D10 prior to the latch timing.

Table 3-1 Serial Control Overview

	SDATA									
Function	**D1**	**D2**	**D3**	**D4**	**D5**	**D6**	**D7**	**D8**	**D9**	**D10**
Knee level gain selection setting	0	0	Knee level setting					Gain select		
			d1	d2	d3	d4	d5	d1	d2	d3
AGC gain setting	0	1	AGC gain							—
			d1	d2	d3	d4	d5	d6	d7	
Pulse selection	1	0	Correc-tion/ knee	—						

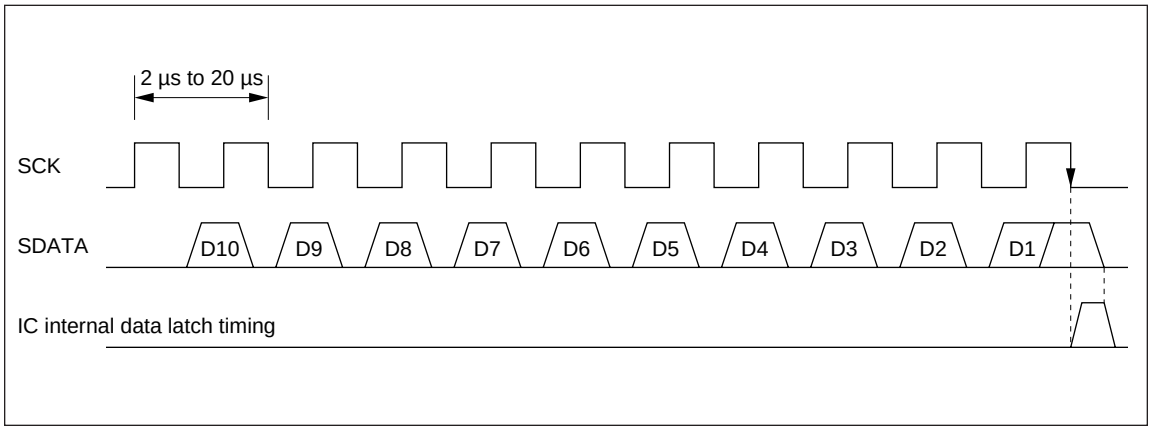


Figure 5 Serial Data Timing Chart

- Bit weightings in serial settings data

• Gain select

D_{10} d_3	D_9 d_2	D_8 d_1	
1	1	1	10.1 dB
1	1	0	
1	0	1	
1	0	0	
0	1	1	
0	1	0	
0	0	1	
0	0	0	–0.2 dB

• Knee level

D_7 d_5	D_6 d_4	D_5 d_3	D_4 d_2	D_3 d_1	
1	1	1	1	1	Knee start
0	1	1	1	1	
1	0	1	1	1	
1	1	0	0	0	
0	1	0	0	0	
1	0	0	0	0	Knee off
0	0	0	0	0	

• AGC gain

D_9 d_7	D_8 d_6	D_7 d_5	D_6 d_4	D_5 d_3	D_4 d_2	D_3 d_1	
1	1	1	1	1	1	1	21 dB
0	1	1	1	1	1	1	
1	0	1	1	1	1	1	
1	1	0	0	0	0	0	
0	1	0	0	0	0	0	
1	0	0	0	0	0	0	0 dB
0	0	0	0	0	0	0	

- Pulse selection

  Since this function is not guaranteed, it should not be used.

The KNP pin (pin 2) should be held low. This bit can be set to either 0 or 1.

Other Items

- Standard waveforms for SIN, SP1, and SP2
  - — SIN inputs a video signal from a CCD.
  - — The SP1 signal performs the field through period clamping, and the SP2 signal performs the signal period sample and hold.
- SO1 and SO2 outputs

  The figure below shows the equivalent circuit for these outputs. As shown in the figure, the output waveform response speed is increased by using a capacitor coupled push-pull structure.

Figure 6 CDS → AGC1 Operating Waveforms

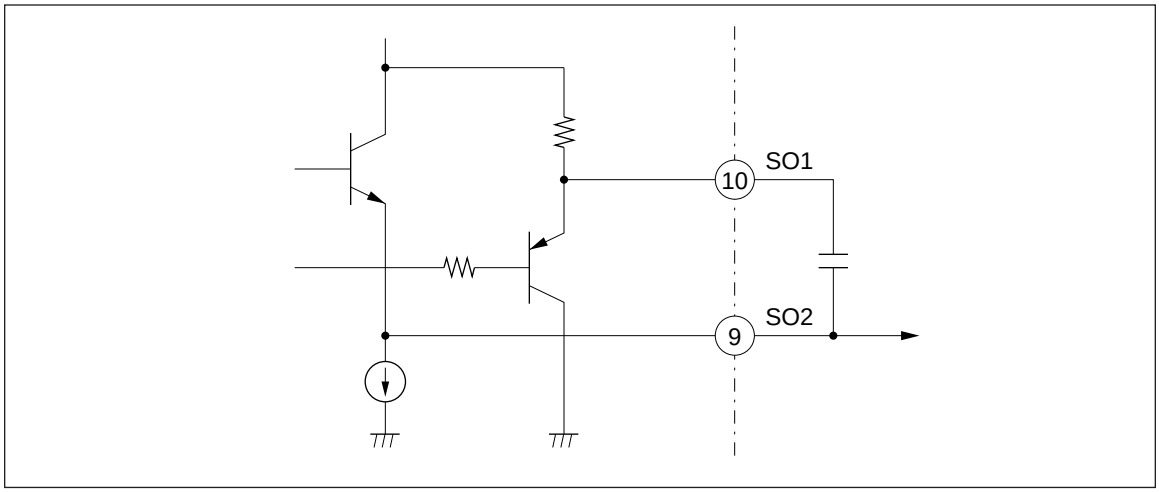


Figure 7 Internal Equivalent Circuit for SO1 and SO2