

## Receiving Dual-Band Mixer

### Description

The CXG1050TN is a receiving dual-band mixer MMIC. This IC is designed using the Sony's GaAs J-FET process.

### Features

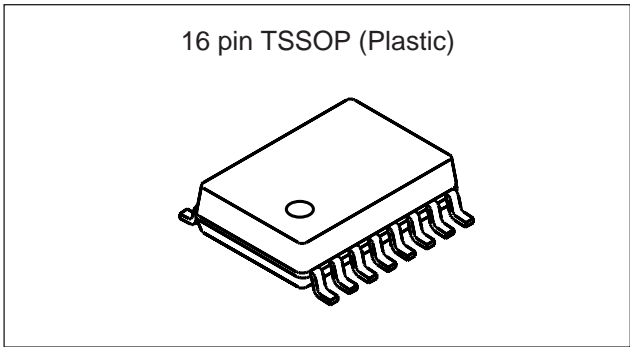
- High conversion gain  $G_c = 9.5\text{dB}$  (Typ.)
- Low noise figure  $NF = 4.9$  to  $5.2\text{dB}$  (Typ.)
- Low distortion Input  $IP_3 = -0.5$  to  $0\text{dBm}$  (Typ.)
- Single 2.7V power supply operation
- Low LO input power operation  $PLO = -15\text{dBm}$
- 16-pin TSSOP small package

### Applications

800MHz Japan digital cellular telephones (PDC)

### Structure

GaAs J-FET MMIC



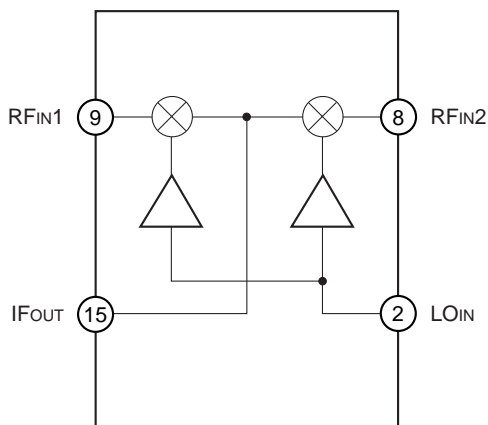
### Absolute Maximum Ratings (Ta = 25°C)

- |                         |                               |             |     |
|-------------------------|-------------------------------|-------------|-----|
| • Supply voltage        | V <sub>DD</sub>               | 4.5         | V   |
| • Input power           | P <sub>IN</sub>               | +5          | dBm |
| • Current consumption   | I <sub>DD</sub> (Mixer block) | 20          | mA  |
| • Operating temperature | T <sub>opr</sub>              | -35 to +85  | °C  |
| • Storage temperature   | T <sub>stg</sub>              | -65 to +150 | °C  |

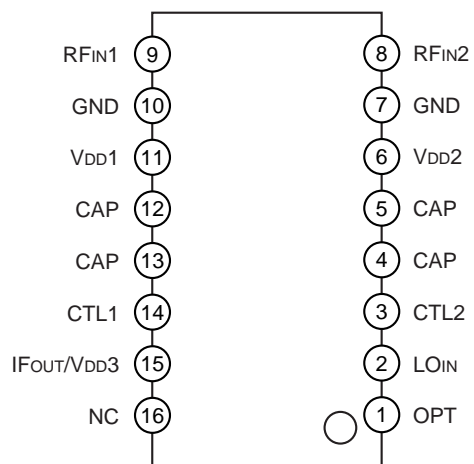
### Recommended Operating Conditions

- |                   |                      |            |   |
|-------------------|----------------------|------------|---|
| • Supply voltage  | V <sub>DD</sub>      | 2.7 to 3.3 | V |
| • Control voltage | V <sub>CTL</sub> (H) | 2.4 to 3.3 | V |
|                   | V <sub>CTL</sub> (L) | 0 to 0.3   | V |

### Block Diagram



### Pin Configuration



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**Electrical Characteristics**

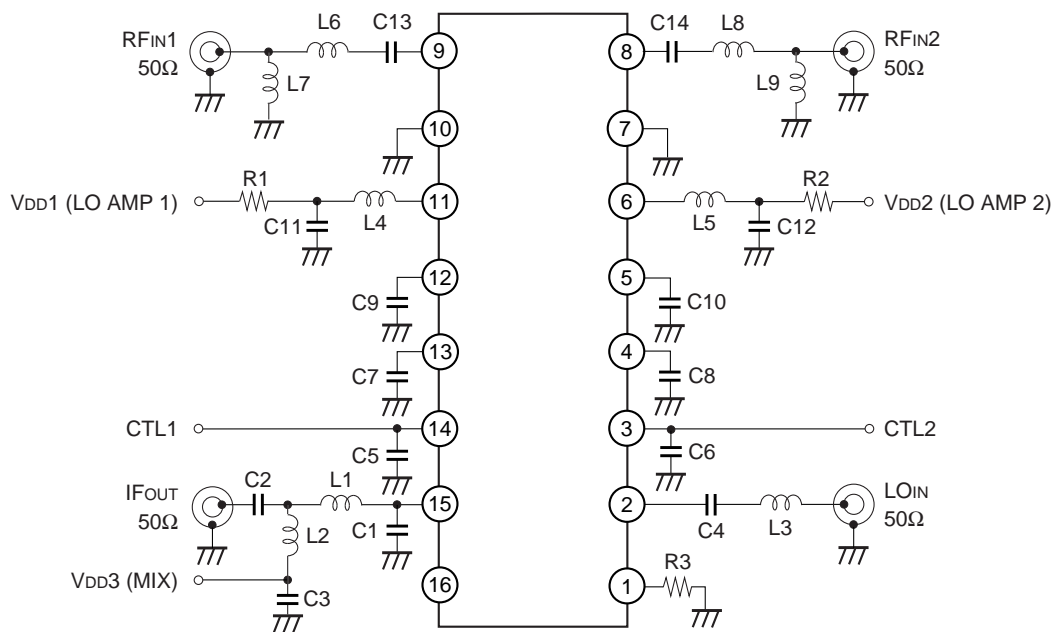
Conditions:  $V_{DD} = 2.7V$ ,  $V_{CTL} (H) = 2.7V$ ,  $V_{CTL} (L) = 0V$ ,  $f_{RF1} = 820MHz$ ,  $f_{RF2} = 870MHz$ ,  
 $f_{LO} = f_{RF} - 130MHz$ ,  $P_{LO} = -15dBm$ , unless otherwise specified

( $T_a = 25^{\circ}C$ )

Item	Symbol	Path	Control pin condition		Min.	Typ.	Max.	Unit	Measurement condition
			V <sub>CTL1</sub>	V <sub>CTL2</sub>					
Current consumption	I <sub>DD</sub>	V <sub>DD1</sub> , V <sub>DD2</sub> V <sub>DD3</sub> → GND	H	L	—	6.3	7.5	mA	When no signal
			L	H					
Control current	I <sub>CTL</sub>	CTL1 → GND	H	L	—	18	35	μA	
		CTL2 → GND	L	H					
Conversion gain	G <sub>C</sub>	RF <sub>IN1</sub> → IF <sub>OUT</sub>	H	L	7	9.5	12	dB	When a small signal
			L	H	—	-16	-12		
		RF <sub>IN2</sub> → IF <sub>OUT</sub>	H	L	—	-13	-9		
			L	H	7	9.5	12		
Noise figure	NF	RF <sub>IN1</sub> → IF <sub>OUT</sub>	H	L	—	4.9	6.5	dB	
		RF <sub>IN2</sub> → IF <sub>OUT</sub>	L	H	—	5.2	6.5		
Input IP3	IIP3	RF <sub>IN1</sub> → IF <sub>OUT</sub>	H	L	-2.5	0	—	dBm	PRF = -25dBm, offset = 100kHz Conversion by the IM3 suppression ratio for two- wave input
		RF <sub>IN2</sub> → IF <sub>OUT</sub>	L	H	-3	-0.5	—		
LO to RF leak level	P <sub>LK</sub>	LO <sub>IN</sub> → RF <sub>IN1</sub>	H	L	—	-37	-30	dBm	f <sub>LO</sub> = 690MHz
		LO <sub>IN</sub> → RF <sub>IN2</sub>	L	H	—	-37	-30		f <sub>LO</sub> = 740MHz

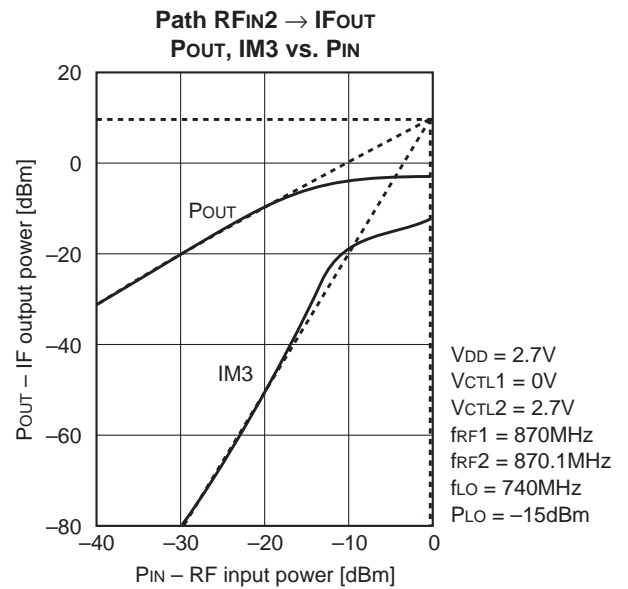
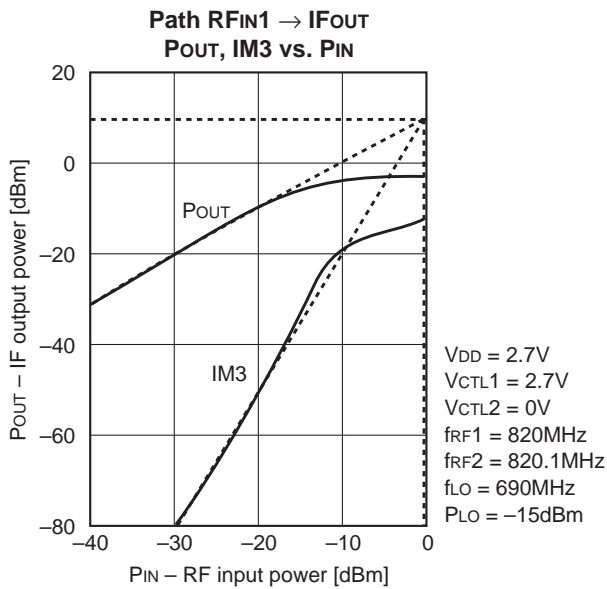
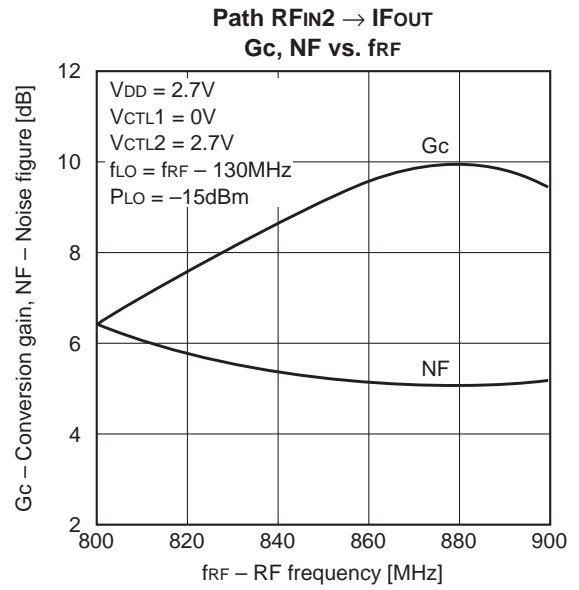
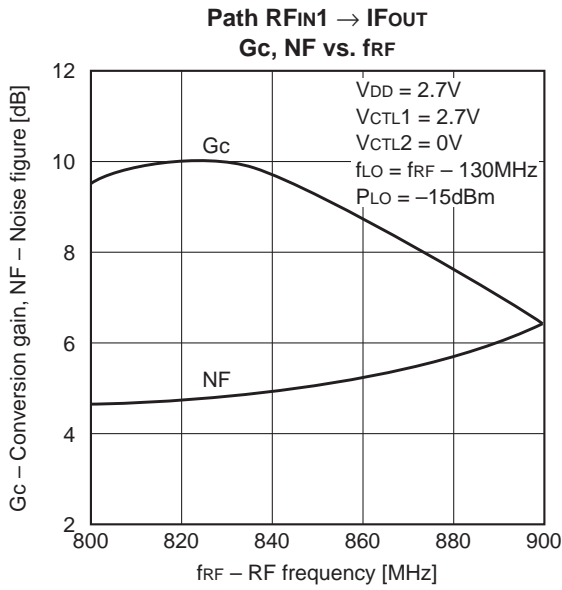
**Note)** The values shown above are the specified values on the Sony's recommended evaluation board.

Recommended Evaluation Circuit

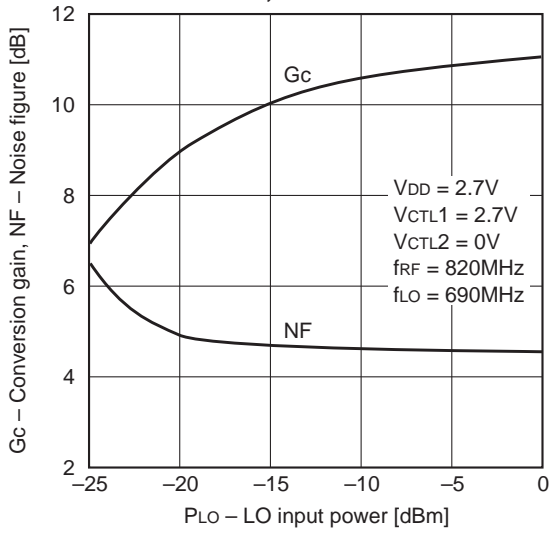


L1	82nH	C1	12pF	C10	100pF
L2	39nH	C2	1000pF	C11	100pF
L3	27nH	C3	1000pF	C12	100pF
L4	47nH	C4	100pF	C13	2pF
L5	39nH	C5	100pF	C14	2pF
L6	39nH	C6	100pF	R1	680Ω
L7	10nH	C7	1000pF	R2	680Ω
L8	33nH	C8	1000pF	R3	820Ω
L9	8.2nH	C9	100pF		

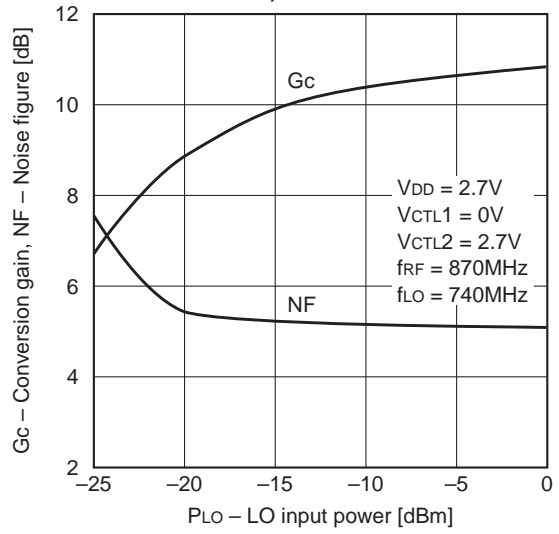
Example of Representative Characteristics (Ta = 25°C)



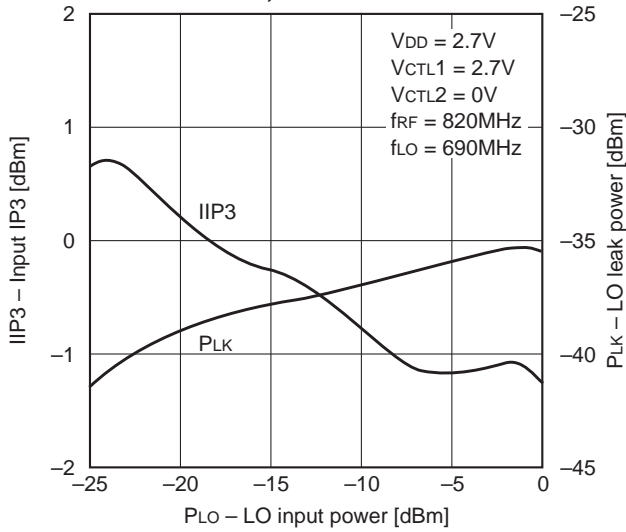
**Path RFin1 → IFout**  
**Gc, NF vs. PLO**



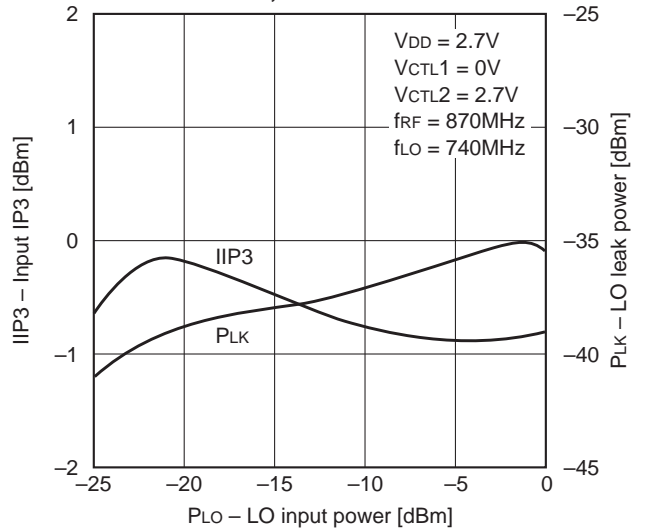
**Path RFin2 → IFout**  
**Gc, NF vs. PLO**



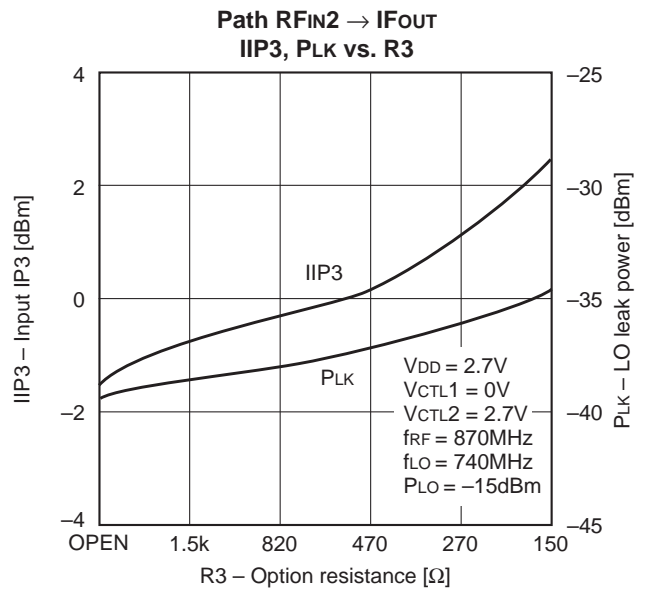
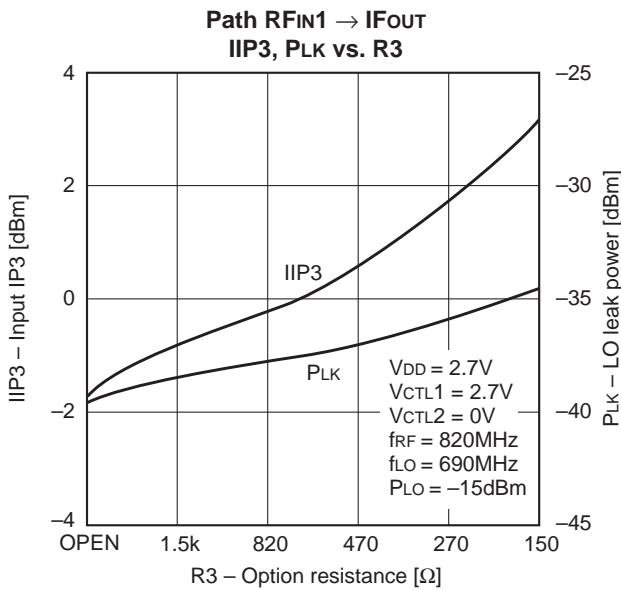
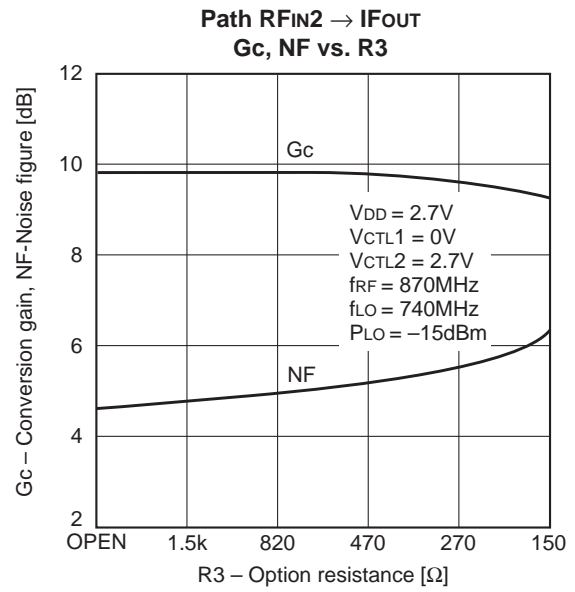
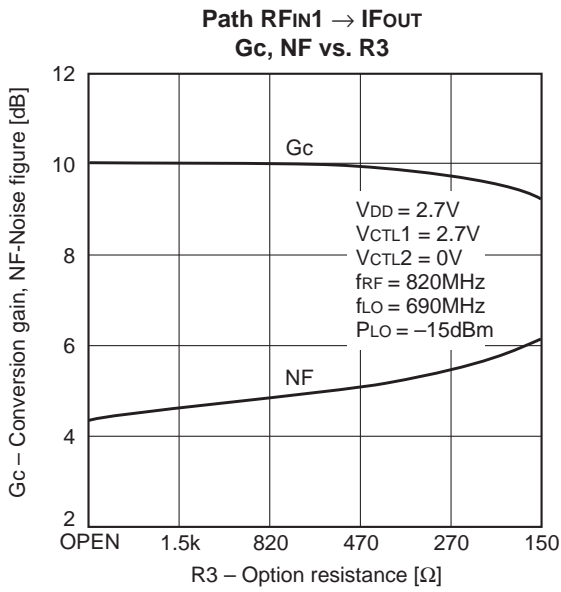
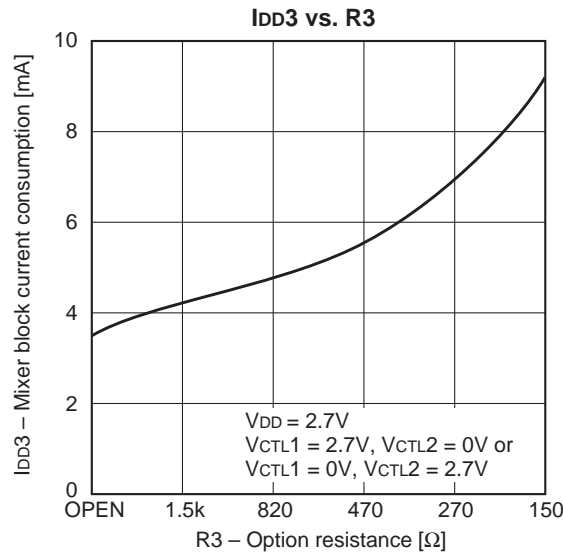
**Path RFin1 → IFout**  
**IIP3, PLK vs. PLO**



**Path RFin2 → IFout**  
**IIP3, PLK vs. PLO**



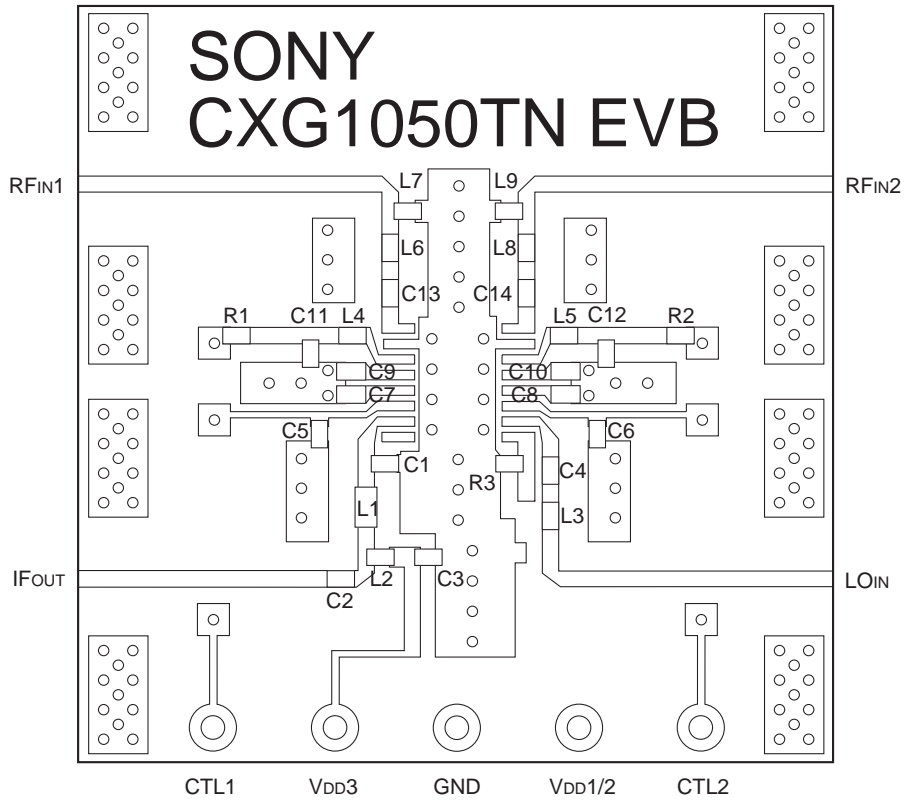
Example of Characteristics for Option Resistance R3 Changed (Ta = 25°C)



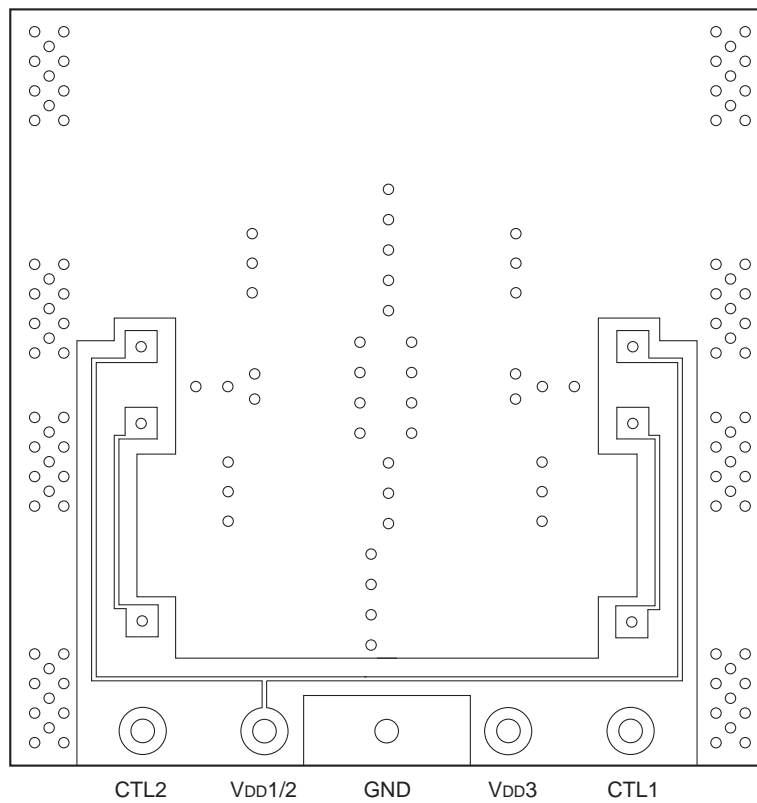
Recommended Evaluation Board

Front

25mm



Back

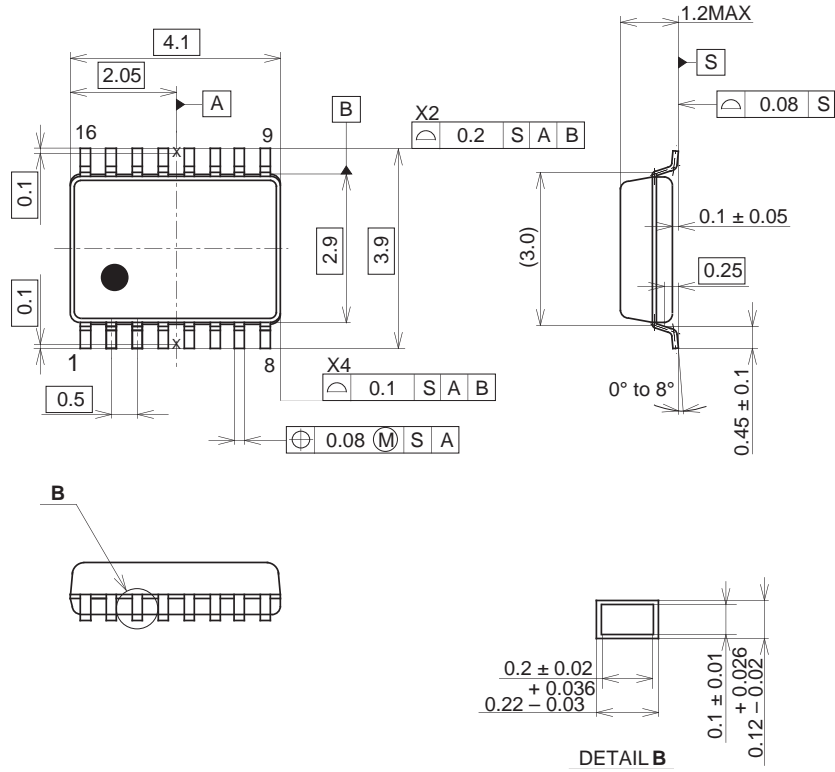


Glass fabric-base 4-layer epoxy board (thickness: 0.3mm × 2)  
GND for the 2nd and 3rd layers

**Package Outline**

Unit: mm

**16PIN TSSOP(PLASTIC)**



SONY CODE	TSSOP-16P-L01
EIAJ CODE	_____
JEDEC CODE	_____

**PACKAGE STRUCTURE**

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.03g