

High-Frequency SPDT Antenna Switch

Description

The CXG1006N is a high power antenna switch MMIC. This IC is designed using the Sony's GaAs J-FET process and operates at a single positive power supply.

Features

- Single positive power supply operation
- Low insertion loss 0.5dB (Typ.) at 2.0GHz
- High isolation 27dB (Typ.) at 2.0GHz
- High power switching

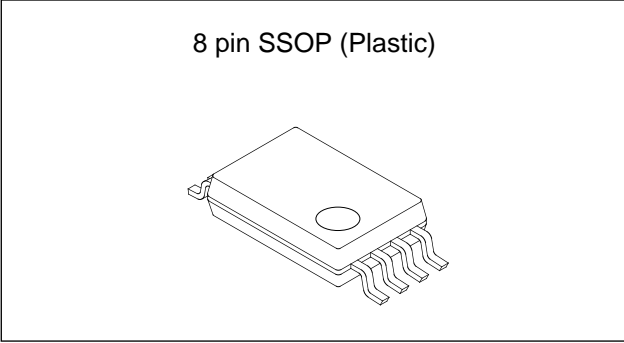
P1dB (Typ.)	32dBm	at 2.0GHz	$V_{CTL} (H) = 2.0V$
	34dBm	at 2.0GHz	$V_{CTL} (H) = 4.0V$

Application

Antenna switch for digital cellular telephones

Structure

GaAs J-FET MMIC



Absolute Maximum Ratings (Ta = 25°C)

- Control voltage V_{ctl} 7 V
- Operating temperature T_{opr} -35 to +85 °C
- Storage temperature T_{stg} -65 to +150 °C

Operating Condition

Control voltage 0/4 V

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Electrical Characteristics

V_{CTL (L)} = 0V, V_{CTL (H)} = 4V, P_{IN} = 30dBm, R_{RF} = 75kΩ (Ta = 25°C)

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Insertion Loss	IL1	f = 1.0GHz		0.3	0.6	dB
Isolation	ISO1		35	40		dB
Insertion Loss	IL1.5	f = 1.5GHz		0.4	0.7	dB
Isolation	ISO1.5		29	32		dB
Insertion Loss	IL2	f = 2.0GHz		0.5	0.8	dB
Isolation	ISO2		24	27		dB
VSWR	VSWR				1.5	
Switching Time	TSW			100		ns

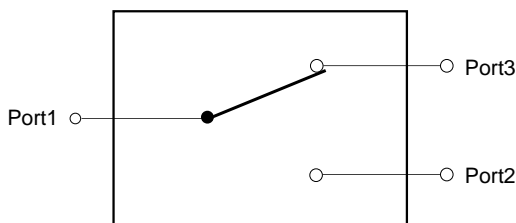
V_{CTL (L)} = 0V, f = 2GHz (Ta = 25°C)

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
1dB Compression Point	P1dB (3)	V _{CTL (H)} = 3V	30	32		dBm
1dB Compression Point	P1dB (4)	V _{CTL (H)} = 4V	32	34		dBm

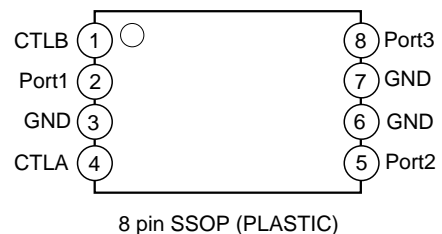
V_{CTL (L)} = 0V, R_{RF} = 75kΩ (Ta = 25°C)

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Control Current	I _{CTL (1)}	V _{CTL (H)} = 3V		100	170	μA
Control Current	I _{CTL (2)}	V _{CTL (H)} = 4V		150	220	μA
Control Current	I _{CTL (3)}	V _{CTL (H)} = 5V		200	270	μA

Block Diagram



Package Outline/Pin Configuration



V _{CTLA}	V _{CTLB}	
High	Low	Port1-Port2 ON Port1-Port3 OFF
Low	High	Port1-Port2 OFF Port1-Port3 ON

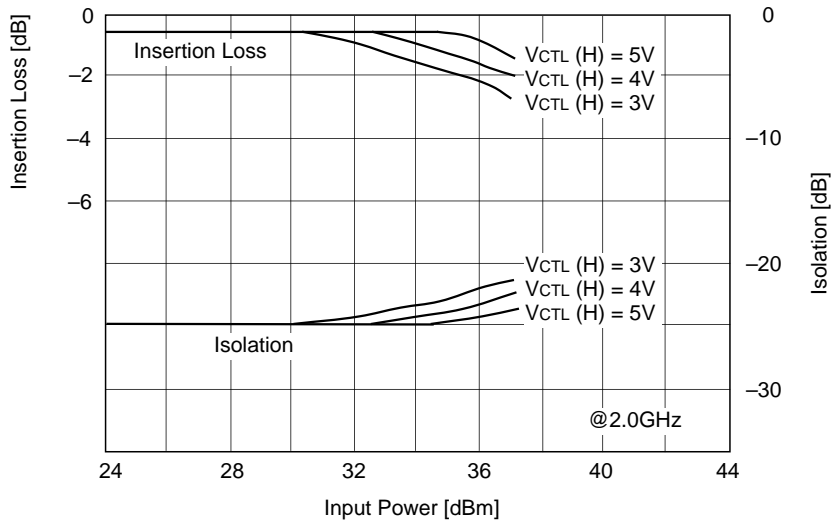
Recommended Circuit



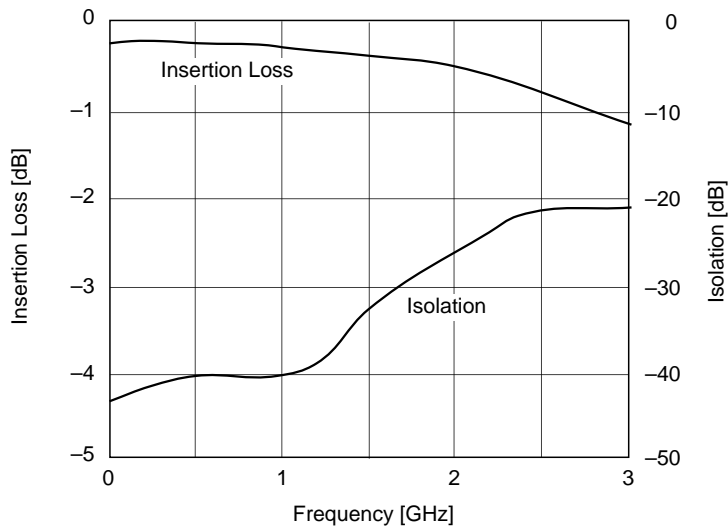
* RRF is used to stabilize the electrical characteristics at high power signal input

Example of Representative Characteristics (Ta = 25°C)

Insertion Loss and Isolation vs. Input Power



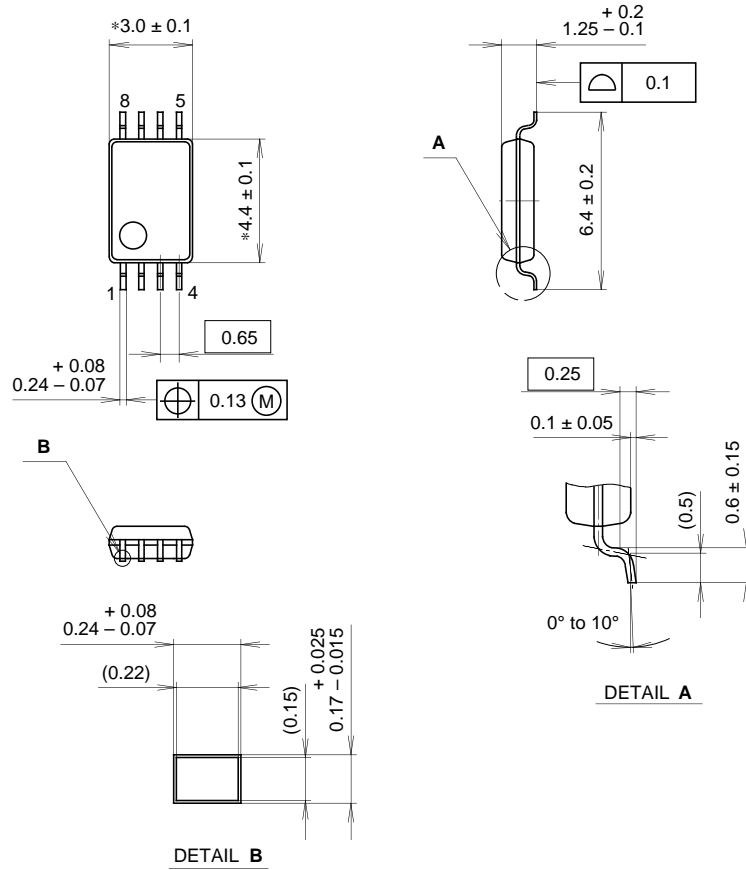
Insertion Loss and Isolation vs. Frequency



Package Outline

Unit: mm

8PIN SSOP (PLASTIC)



NOTE: Dimension "*" does not include mold protrusion.

PACKAGE STRUCTURE

SONY CODE	SSOP-8P-L01
EIAJ CODE	SSOP008-P-0044
JEDEC CODE	_____

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER / PALLADIUM PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE WEIGHT	0.04g