SONY

CXD2400R

Timing Controller for CCD cameras

Description

The CXD2400R is a timing controller for CCD camera systems which use the ICX044/045, ICX054/055 or other black/white CCD image sensors.

Features

- Supports EIA/CCIR standards
- Electronic iris (electronic shutter) function
- Sync signal generation function
- Supports external synchronization
- Supports non-interlacing
- Supports field/frame* accumulation
- Oscillator frequency: 1212 fh
  (EIA: 19.0699MHz; CCIR: 18.9375MHz)

* The characteristics of CCD image sensors are guaranteed for field accumulation operation.

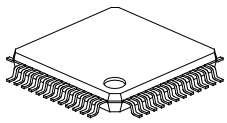
Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	V_{DD}	Vss – 0.5 to +7.5	V
• Input voltage	V_I	Vss – 0.5 to V_{DD} + 0.5	V
• Output voltage	Vo	Vss – 0.5 to V_{DD} + 0.5	V
• Operating temperature	Topr	–20 to +75	°C
• Storage temperature	Tstg	–55 to +150	°C

Recommended Operating Conditions

• Supply voltage	5.0V ± 0.25	V
• Operating temperature	–20 to +75	°C

48 pin LQFP (Plastic)



Applications

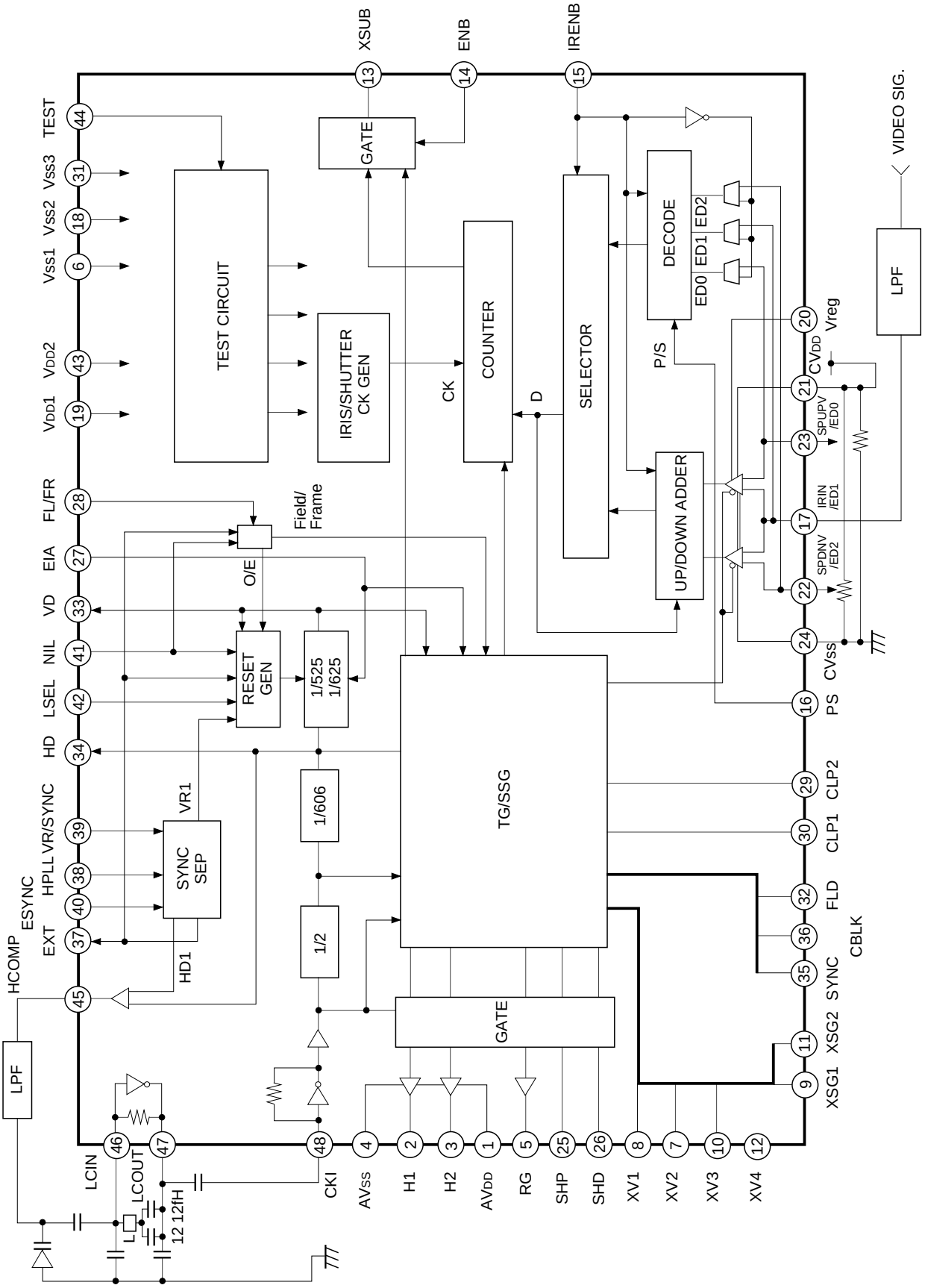
CCD cameras

Structure

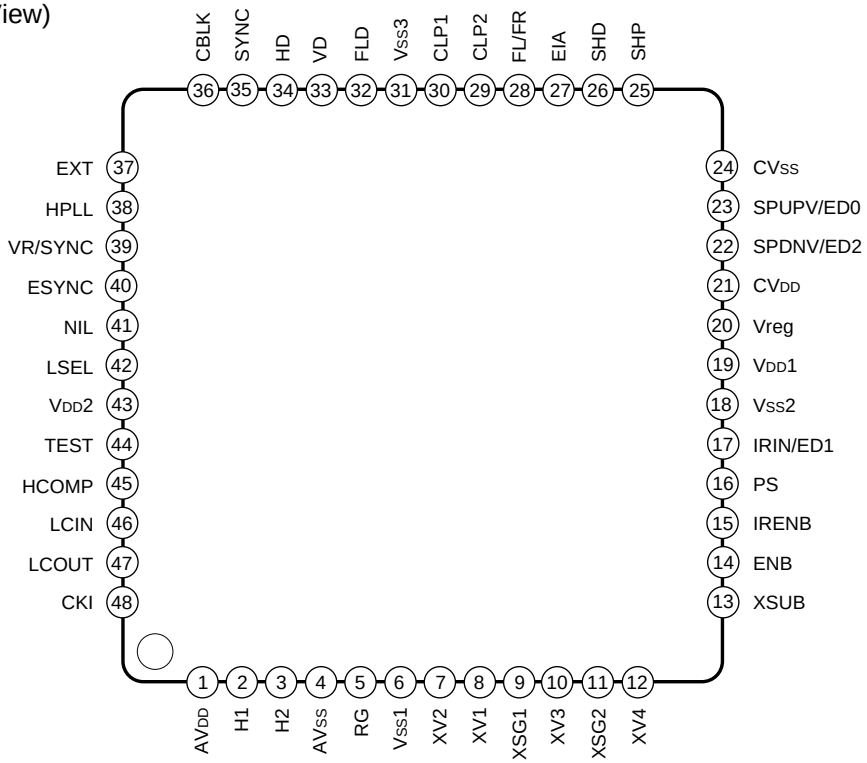
Silicon gate CMOS IC

E93308D75-PS

Block Diagram



Pin Configuration (Top View)



Pin Description

Pin No.	Symbol	I/O	Description
1	AVDD	—	Power supply (for H1, H2)
2	H1	O*2	H1 clock output for CCD horizontal register drive
3	H2	O*2	H2 clock output for CCD horizontal register drive
4	AVss	—	GND (for H1, H2)
5	RG	O*5	Reset gate pulse output
6	Vss1	—	GND
7	XV2	O	XV2 clock output for CCD vertical register drive
8	XV1	O	XV1 clock output for CCD vertical register drive
9	XSG1	O	CCD sensor charge readout pulse output
10	XV3	O	XV3 clock output for CCD vertical register drive
11	XSG2	O	CCD sensor charge readout pulse output
12	XV4	O	XV4 clock output for CCD vertical register drive
13	XSUB	O	CCD discharge pulse output
14	ENB	I	XSUB pulse output ON/OFF control (with pull-up resistance) Low: XSUB pulse output stop; high: XSUB pulse output
15	IRENB	I	Low: Electronic shutter mode; high: electronic iris mode (with pull-up resistance)
16	PS	I	Electronic shutter speed input switchover (with pull-up resistance) Low: Serial input; high: parallel input
17	IRIN/ED1	I*1	Iris signal input/shutter speed setting; clock input in serial mode.
18	Vss2	—	GND
19	VDD1	—	Power supply

Pin No.	Symbol	I/O	Description
20	Vreg	—	Bias current supply for comparator
21	CV_{DD}	—	Power supply (for comparator)
22	SPDNV /ED2	I*1	Shutter speed down reference voltage/ Shutter speed setting; data input in serial mode
23	SPUPV /ED0	I*1	Shutter speed up reference voltage/ Shutter speed setting; strobe input in serial mode
24	CVss	—	GND (for comparator)
25	SHP	O*1	Precharge level sample-and-hold pulse
26	SHD	O*1	Data sample-and-hold pulse
27	EIA	I	Low: EIA; high: CCIR (with pull-down resistance)
28	FL/FR	I	Field accumulation/frame accumulation, odd field/even field switchover (with pull-down resistance)
29	CLP2	O	Pulse output for clamp
30	CLP1	O	Pulse output for clamp
31	Vss3	—	GND
32	FLD	O	Field identification signal output High: odd field; low: even field
33	VD	O	Vertical drive output
34	HD	O	Horizontal drive output
35	SYNC	O	Composite sync output
36	CBLK	O	Composite blanking output
37	EXT	O	External sync/internal sync identification signal High: external sync; Low: internal sync
38	HPLL	I	Horizontal drive signal input (with pull-up resistance)
39	VR/SYNC	I	Vertical drive signal input/composite sync input (with pull-up resistance)
40	ESYNC	I	Low: SYNC sync or internal sync; high: VD/HD sync (with pull-down resistance)
41	NIL	I	Low: interlace mode; high: non-interlace mode (with pull-down resistance)
42	LSEL	I	Line number selection pin (with pull-down resistance) Low: EIA 262H/CCIR 312H; high: EIA 263H/CCIR 313H
43	$V_{DD}2$	—	Power supply
44	TEST	I	Fixed to low level (with pull-down resistance)
45	HCOMP	O*4	H comparator output
46	LCIN	I*2	LC oscillation (crystal oscillator) inverter input
47	LCOUT	O*3	LC oscillation (crystal oscillator) inverter output
48	CKI	I*3	Clock input

O*1 → POWERED BUFFER
O*2 → Hdriver Cell
O*3 → OSCILLATOR Cell
O*4 → Phase Comparater
O*5 → RGdriver Cell

I*1 → Comparater Input
I*2 → OSCILLATOR Cell
I*3 → Input cell with feedback resistance

Electrical Characteristics

1) DC Characteristics

(V_{DD} = 5V ± 0.25V, Topr = –20 to +75°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}		4.75	5.0	5.25	V
Input voltage 1 (All input pins except those below)	V_{IH1}		0.7V_{DD}			V
	V_{IL1}				0.3V_{DD}	V
Input voltage 2 (Pins 22, 23 only in electronic iris mode)	V_{IN2}		2.0		V_{DD}	V
Input voltage 3 (Pin 17 only in electronic iris mode)	V_{IN3}		V_{SS}		V_{DD}	V
Output voltage 1 (All output pins except those below)	V_{OH1}	I_{OH} = –2mA	V_{DD} – 0.8			V
	V_{OL1}	I_{OL} = 4mA			0.4	V
Output voltage 2 (Pins 25, 26)	V_{OH2}	I_{OH} = –4mA	V_{DD} – 0.8			V
	V_{OL2}	I_{OL} = 8mA			0.4	V
Output voltage 3 (Pin 5)	V_{OH3}	I_{OH} = –8mA	V_{DD} – 0.8			V
	V_{OL3}	I_{OL} = 8mA			0.4	V
Output voltage 4 (Pins 2, 3)	V_{OH4}	I_{CH} = –20mA	V_{DD} – 0.8			V
	V_{OL4}	I_{CL} = 20mA			0.4	V
Output voltage 5 (Pin 47)	V_{OH5}	I_{OH} = –3mA	V_{DD}/2			V
	V_{OL5}	I_{OL} = 3mA			V_{DD}/2	V
Output voltage 6 (Pin 45)	V_{OH6}	I_{OH} = –4mA	V_{DD} – 0.8			V
	V_{OL6}	I_{OL} = 4mA			0.4	V
Feedback resistance	R_{FB}	V_{IN} = Vss or V_{DD}	250k	1M	2.5M	Ω
Pull-up resistance	R_{PU}	V_{IL} = 0V	25k	50k	75k	Ω
Pull-down resistance	R_{PD}	V_{IH} = V_{DD}	25k	50k	75k	Ω
Current consumption	I_{DD}	V_{DD} = 5V ICX054AL in normal operating state		36		mA

* Power consumption: 180mW typ., ICX054AL load (in normal operating state)

2) Input/output capacitance

(V_{DD} = V_1 = 0V, f_M = 1MHz)

Item	Symbol	Min.	Typ.	Max.	Unit
Input pin capacitance	C_{IN}			9	pF
Output pin capacitance	C_{OUT}			11	pF
Input/output pin capacitance	$C_{I/O}$			11	pF

3) Comparator characteristics (V_{DD} = 5V ± 0.25V, Topr = –20 to +75°C)

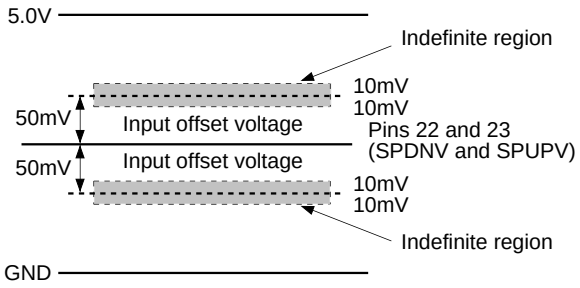
Item	Symbol	Min.	Typ.	Max.	Unit
Input offest voltage	V_{OS}			50	mV
Indefinite region	Vf			± 10	mV

Note) 1. Input offset voltage and indefinite region

Input offset voltage and indefintie region are existed in the comparator which builds in this IC as shown right figure. Note that this when designing external circuit.

2. Pins 22 and 23 for electronic iris mode

Use it in this state of Pin 22 (SPDNV) > Pin 23 (SPUPV).



Mode Control

Symbol	Pin No.	I/O	Low	High	Remarks
ENB	14	I	XSUB stop	XSUB output	
IRENB	15	I	Electronic shutter	Electronic iris	Valid only when ENB is high.
PS	16	I	Serial input	Parallel input	Valid only when ENB is high and IRENB is low.
IRIN/ED1	17	I	Electronic iris control signal input pin (IRENB = high) Shutter speed setting pin (IRENB = Low)		Valid only when ENB is high.
SPDNV/ED2	22	I			
SPUPV/ED0	23	I			
EIA	27	I	EIA	CCIR	
FL/FR	28	I	Odd field	Even field	Valid only when NIL is high and EXT is low.
			Field accumulation	Frame accumulation*	All other modes.
ESYNC	40	I	SYNC sync Internal sync	VD/HD sync	
HPLL	38	I	Internal sync : HPLL (Open) VR/SYNC (Open) SYNC sync : HPLL (Open) VR/SYNC (SYNC input) VD/HD sync : HPLL (HD input) VR/SYNC (VD input)		
VR/SYNC	39	I			
NIL	41	I	Interlace	Non-interlace	Valid only when EXT is low.
LSEL	42	I	EIA : 262H CCIR : 312H	EIA : 263H CCIR : 313H	Valid only when EXT is low and NIL is high.
EXT	37	O	Internal sync	External sync	Switchover between internal and external sync is autonatically identified by input state at Pins 38, 39 and 40.

* The characteristics of CCD image sensors are quaranteed for field acccumulation operation.

Mode Tables

1) Internal sync mode

HPLL pin (Pin 38) : Open
VR/SYNC pin (Pin 39) : Open
ESYNC pin (Pin 40) : Open

	Interlace		Non-interlace			
			Odd field*2		Even field*2	
	Field readout	Frame readout*3	Field readout	Frame readout*3	Field readout	Frame readout*3
XSUB pulse OFF*1	O	O	O	×	O	×
Electronic shutter ON	O	O	O	×	O	×
Electronic iris ON	O	O	O	×	O	×

*1 EIA for 1/60 s accumulation; CCIR for 1/50 s accumulation
O: Can be used.
*2 Line number is 262H or 263H for EIA and 312H or 313H for CCIR.
×: Cannot be used.
*3 The characteristics of CCD image sensors are guaranteed for field accumulation operation.

2) SYNC sync (external sync) mode

HPLL pin (Pin 38) : Open
VR/SYNC pin (Pin 39) : SYNC input
ESYNC pin (Pin 40) : Open

	Interlace		Non-interlace			
			Odd field*2		Even field*2	
	Field readout	Frame readout*3	Field readout	Frame readout*3	Field readout	Frame readout*3
XSUB pulse OFF*1	O	O	×	×	×	×
Electronic shutter ON	O	O	×	×	×	×
Electronic iris ON	O	O	×	×	×	×

*1 EIA for 1/60 s accumulation; CCIR for 1/50 s accumulation
O: Can be used.
*2 Line number is 262H or 263H for EIA and 312H or 313H for CCIR.
×: Cannot be used.
*3 The characteristics of CCD image sensors are guaranteed for field accumulation operation.

3) VD/HD sync (external sync) mode

HPLL pin (Pin 38) : HD input
VR/SYNC pin (Pin 39) : VD input
ESYNC pin (Pin 40) : V_{DD} (power supply)

	VD input with normal cycle						VD input with longer cycle than normal interlace	
	Interlace		Non-interlace					
			Odd field*2		Even field*2			
	Field readout	Frame readout*3	Field readout	Frame readout*3	Field readout	Frame readout*3	Field readout	Frame readout*3
XSUB pulse OFF*1	O	O	O	×	O	×	O	×
Serial input electronic shutter ON	O	O	O	×	O	×	×	×
Parallel input electronic shutter ON	O	O	Δ	×	Δ	×	×	×
Electronic iris ON	O	O	O	×	O	×	×	×

*1 EIA for 1/60 s accumulation; CCIR for 1/50 s accumulation

*2 Line number is 262H or 263H for EIA and 312H or 313H for CCIR.

*3 The characteristics of CCD image sensors are guaranteed for field accumulation operation.

O: Can be used.

Δ: The shutter speed may change from its value in the interlace mode.

×: Cannot be used.

Note) Only in the VD/HD sync mode, the external synchronization is possible during which VD pulses with longer cycle than normal are input to the VR/SYNC pin.

Electronic Shutter/Iris

By setting ENB pin (Pin 14) high, the XSUB pulse is output for a specific period to activate the electronic shutter and electronic iris.

1) Electronic iris (IRENB = high, PS = any level)

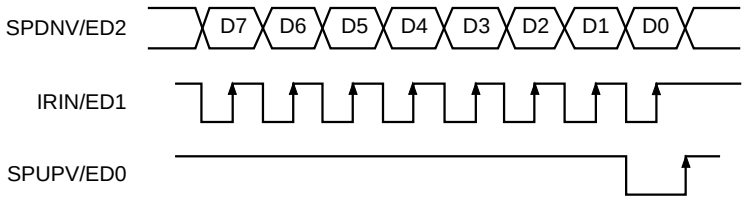
Symbol	Pin No.	Function
IRIN/ED1	17	Iris signal input
SPDNV/ED2	22	Shutter speed down reference voltage
SPUPV/ED0	23	Shutter speed up reference voltage

2) Parallel input electronic shutter (IRENB = low, PS = high)

Symbol	Pin No.	Mode							
SPUPV/ED0	23	H	L	H	L	H	L	H	L
IRIN/ED1	17	H	H	L	L	H	H	L	L
SPDNV/ED2	22	H	H	H	H	L	L	L	L
Shutter speed		EIA: 1/100 CCIR: 1/120	1/250	1/500	1/1000	1/2000	1/5000	1/10000	1/100000

3) Serial input electonic shutter (IRENB = low, PS = high)

Serial input data format

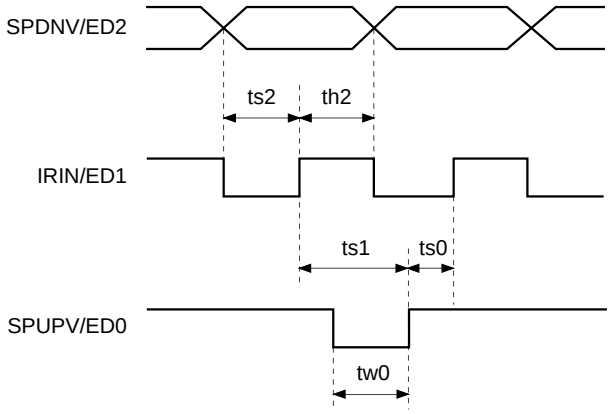


The ED2 data is latched in the register at the ED1 rise, and retrieved internally at the ED0 rise.

Typical shutter speed

EIA		CCIR	
Load value	shutter speed	Load value	shutter speed
00h	1/100000	00h	1/80000
4Eh	1/10000	4Ah	1/10000
6Ah	1/5000	65h	1/5000
87h	1/2000	82h	1/2000
9Ch	1/1000	97h	1/1000
ACh	1/500	A7h	1/500
CAh	1/250	C5h	1/250
EDh	1/100	E1h	1/120

AC Characteristics



Symbol		Min.	Max.
ts2	SPDNV (ED2) setup time for IRIN (ED1) rise	20ns	—
th2	SPDNV (ED2) hold time for IRIN (ED1) rise	20ns	—
ts1	IRIN (ED1) setup time for SPUPV (ED0) rise	20ns	—
tw0	SPUPV (ED0) pulse width	20ns	50µs
ts0	SPUPV (ED0) setup time for IRIN (ED1) rise	20ns	—

External Synchronization

1) External/internal sync selection

External or internal synchronization is selected automatically by a combination of 3 pins (VR/SYNC, HPLL and ESYNC) to which the sync signal is input externally. The table below shows the input pattern combinations.

Input pattern	VR/SYNC pin: SYNC signal HPLL pin: Open ESYNC pin: Open	VR/SYNC pin: VD signal HPLL pin: HD signal ESYNC pin: V_{DD} (power supply)	VR/SYNC pin: Open HPLL pin: Open ESYNC pin: Open
EXT pin output	High	High	Low
Sync state	External sync	External sync	Internal sync

Note) Operation is possible even if the VD cycle of the VD input in the VD/HD sync mode is longer than normal.

The EXT pin is the external/internal sync identification signal output pin. This output signal can be used as the signal to select LC oscillation for expanding the lock range for external synchronization or the oscillator for improving the oscillation accuracy for internal synchronization.

2) Modes for external synchronization

		Field accumulation	Frame accumulation*
SYNC synchronization	Interlace	O	O
	Non-interlace	× (Cannot be accomplished since interlace operation is the prior condition.)	× (Cannot be accomplished since interlace operation is the prior condition.)
VD/HD synchronization	Interlace	O	O
	Non-interlace	O	× (Not practically applicable since the sensitivity is halved.)

* The characteristics of CCD image sensors are guaranteed for field accumulation operation.

3) Reset operation

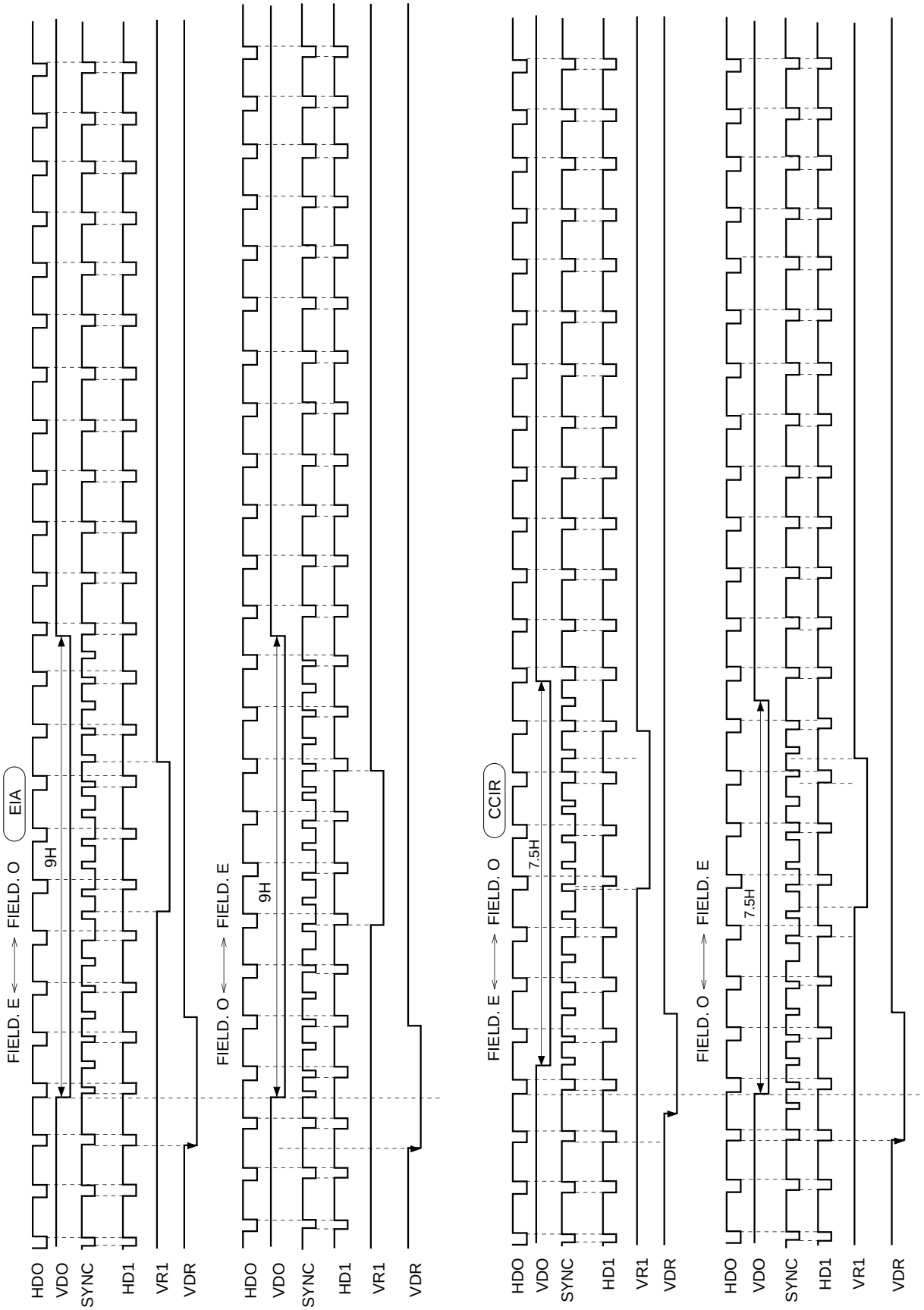
SYNC synchronization

The VR1 signal component is extracted from the SYNC signal supplied externally and, for EIA, V reset is performed so that the VDO pulse falls at the count of 259H (262.5 – 3.5H) from the fall of the VR1 pulse. For CCIR, it is reset in such a way that the VDO pulse falls at the count of 309H (312.5 – 3.5H). For these reasons, it is a prerequisite that the SYNC signal input comply with the EIA or CCIR standard.

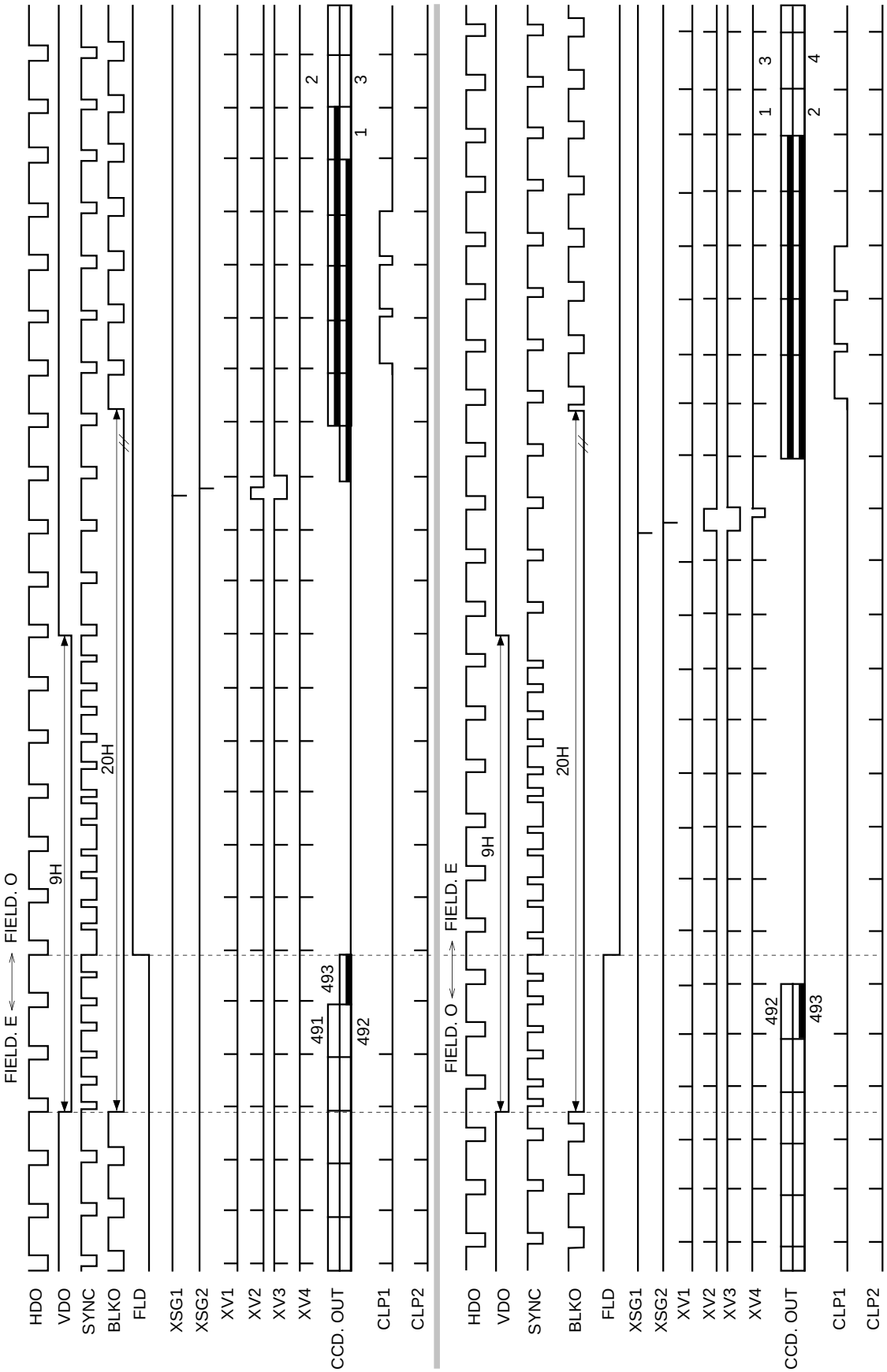
VD/HD synchronization

V reset is performed so that the VDO pulse falls 1H later after detecting the fall of the VD (VDR) pulse supplied externally. Therefore, this enables V reset operation regardless of the field line number. The phase difference between the VDR pulse and HDO pulse which is locked horizontally at PLL circuit identifies whether the field is odd or even. (VDR must have a pulse width of 2H or more.)

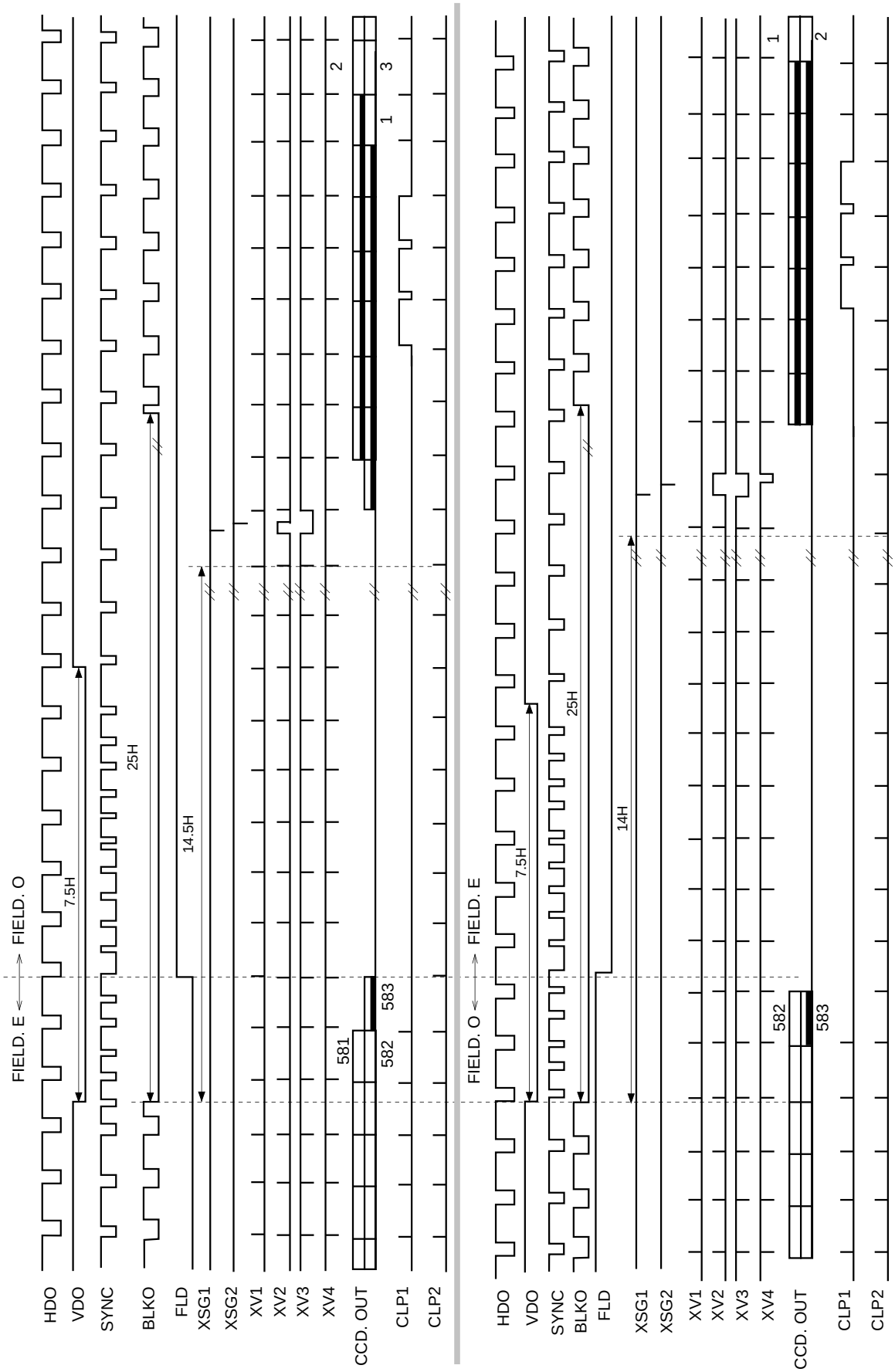
External Synchronization Reset Operation



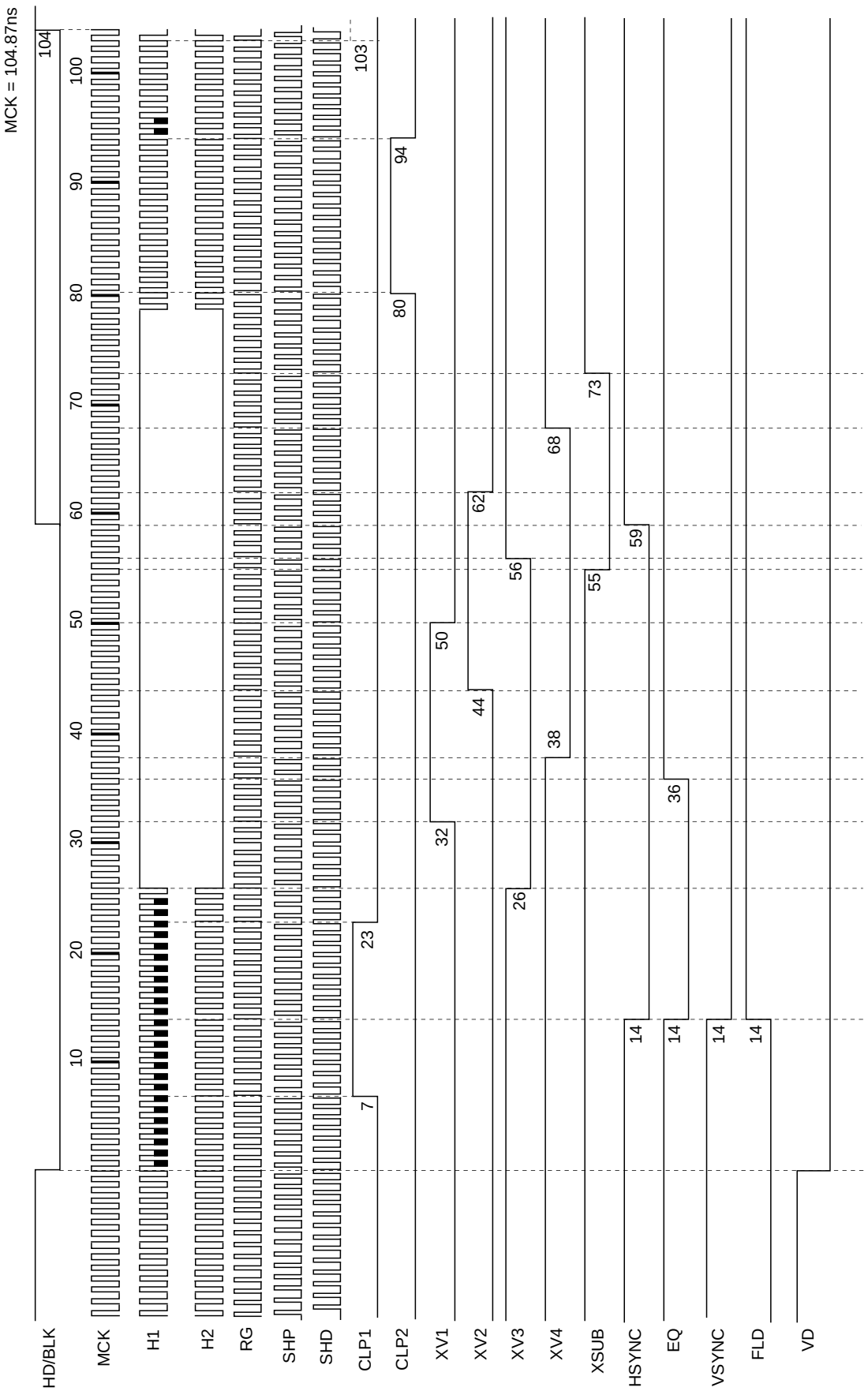
TG+SG Timing Chart
V derection, EIA



TG+SG Timing Chart
V derection, CCIR

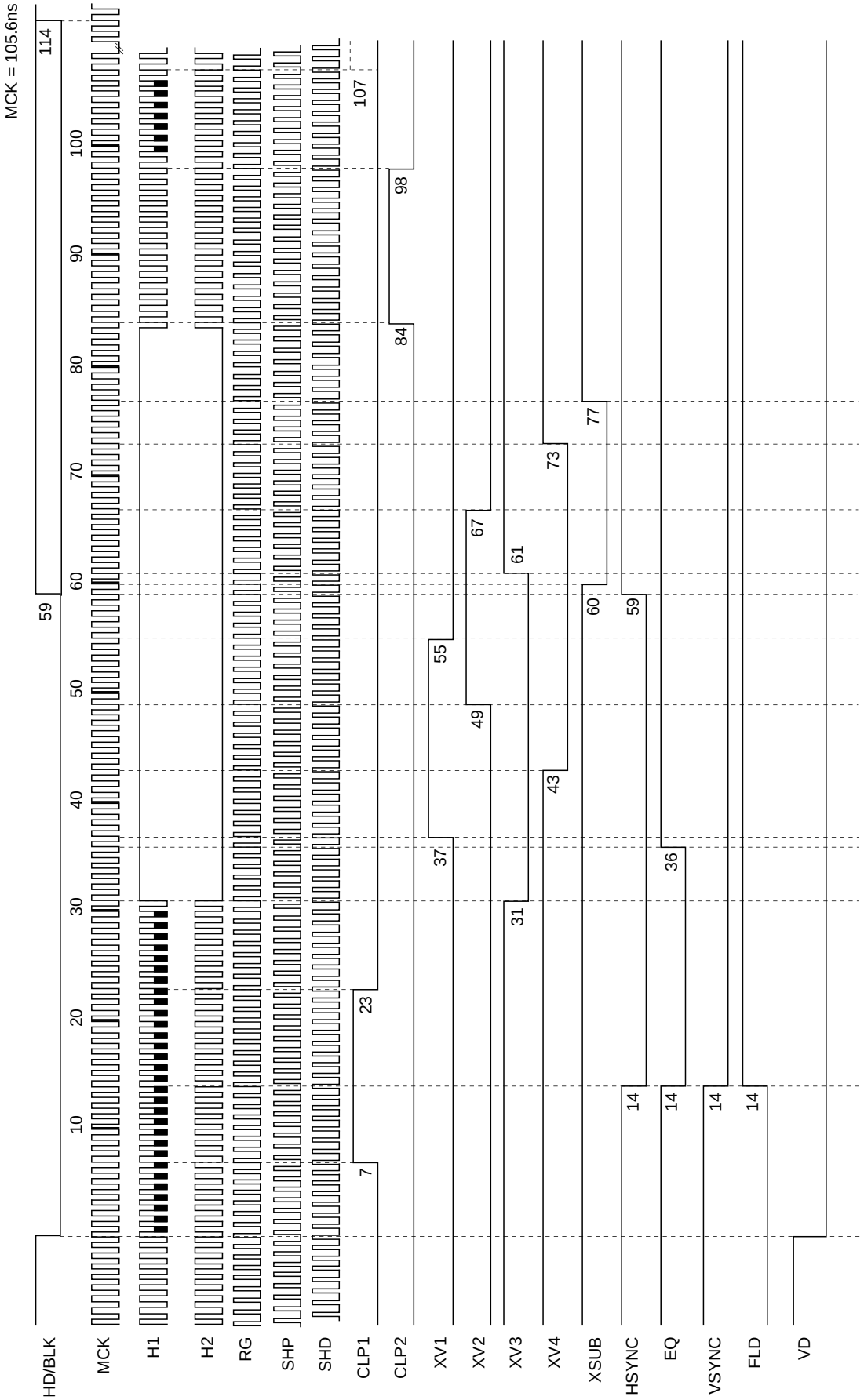


TG+SG Timing Chart
H derection, EIA



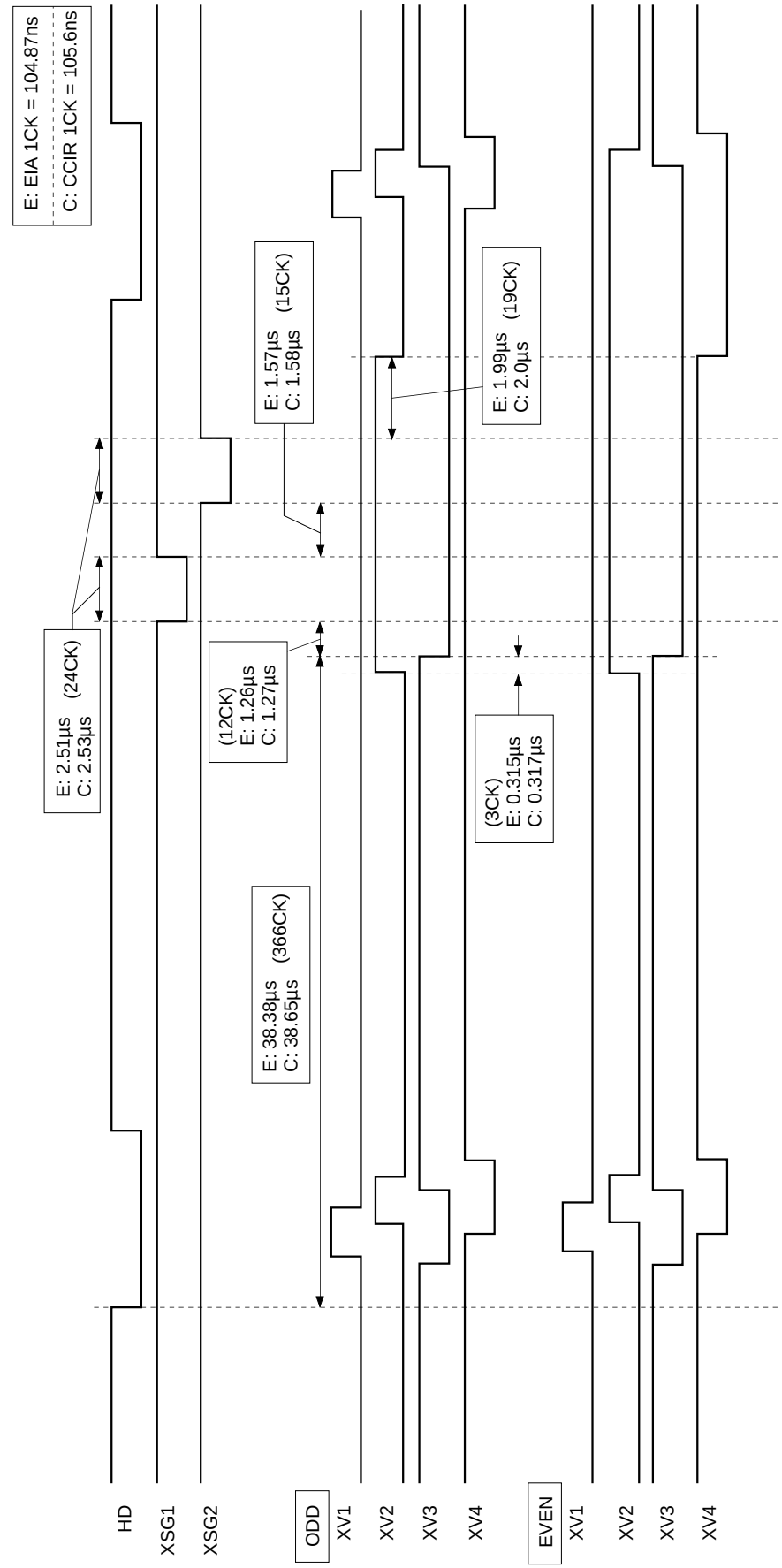
Black areas show OB output timing of CCD (ICX044/ICX054).

TG+SG Timing Chart
H derection, CCIR

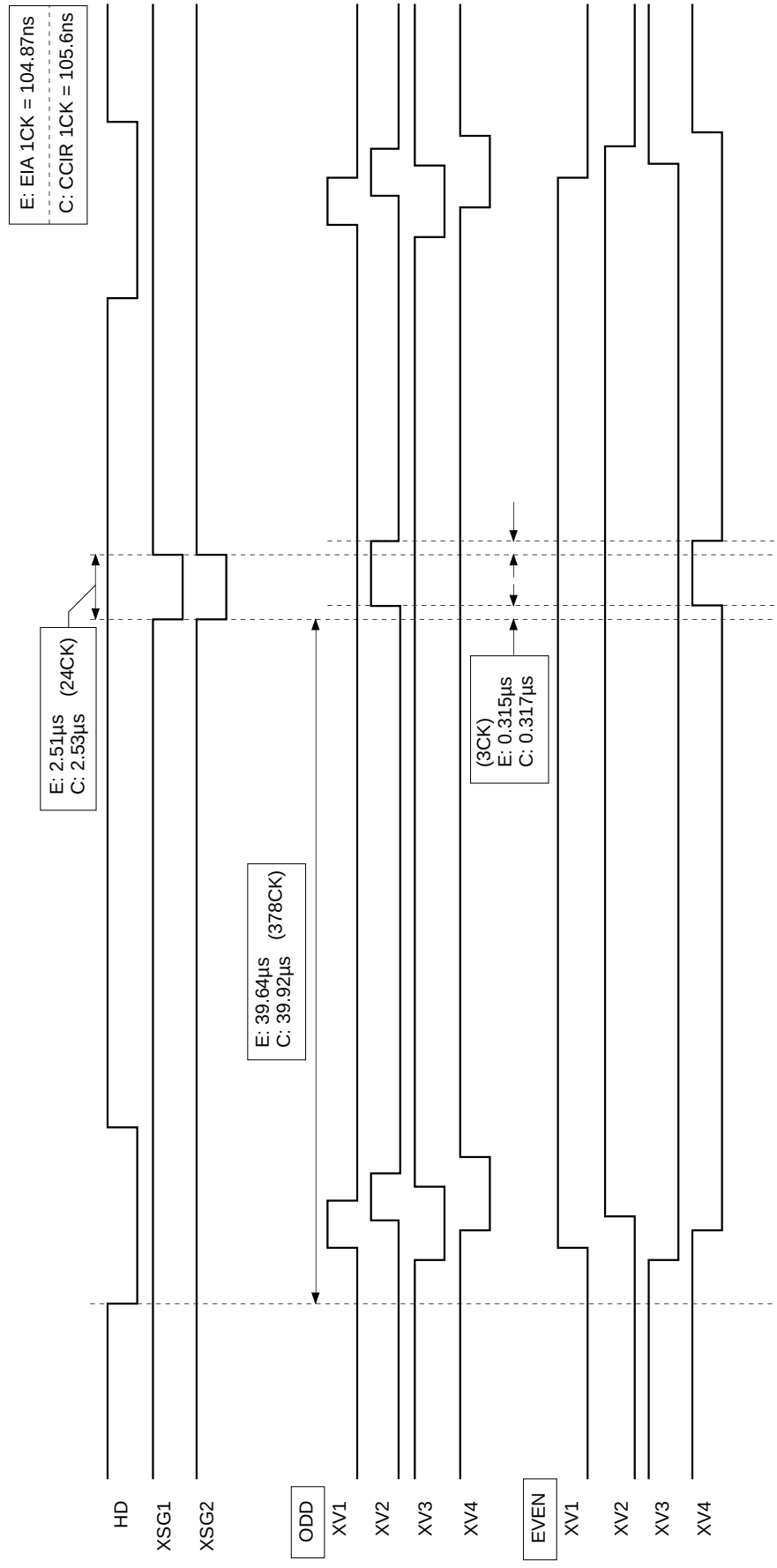


Black areas show OB output timing of CCD (ICX045/ICX055).

TG+SG Timing Chart
Charge Readout Timing
Field accumulation



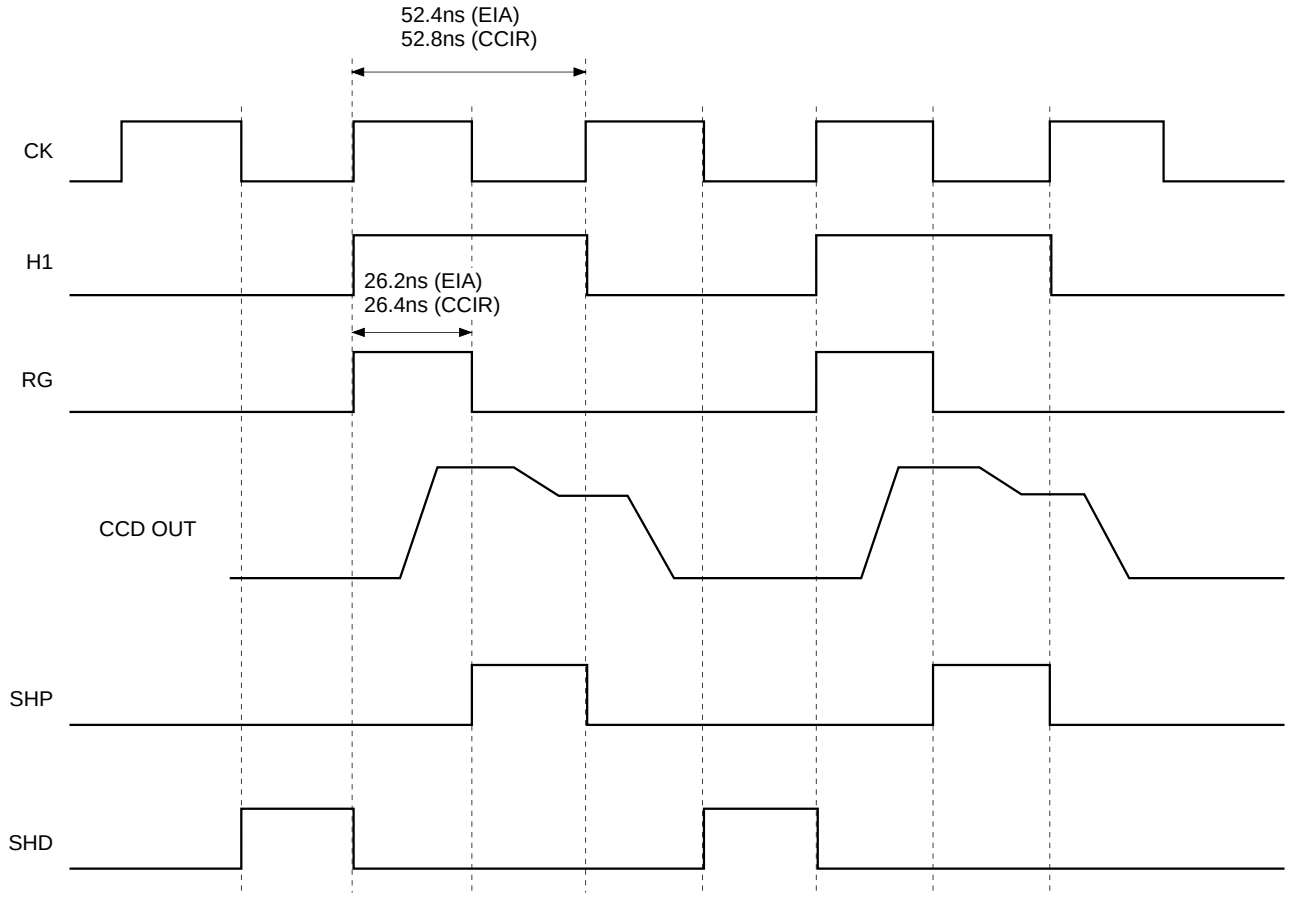
TG+SG Timing Chart
Charge Readout Timing
Frame accumulation



* The characteristics of CCD image sensors are guaranteed for field accumulation operation.

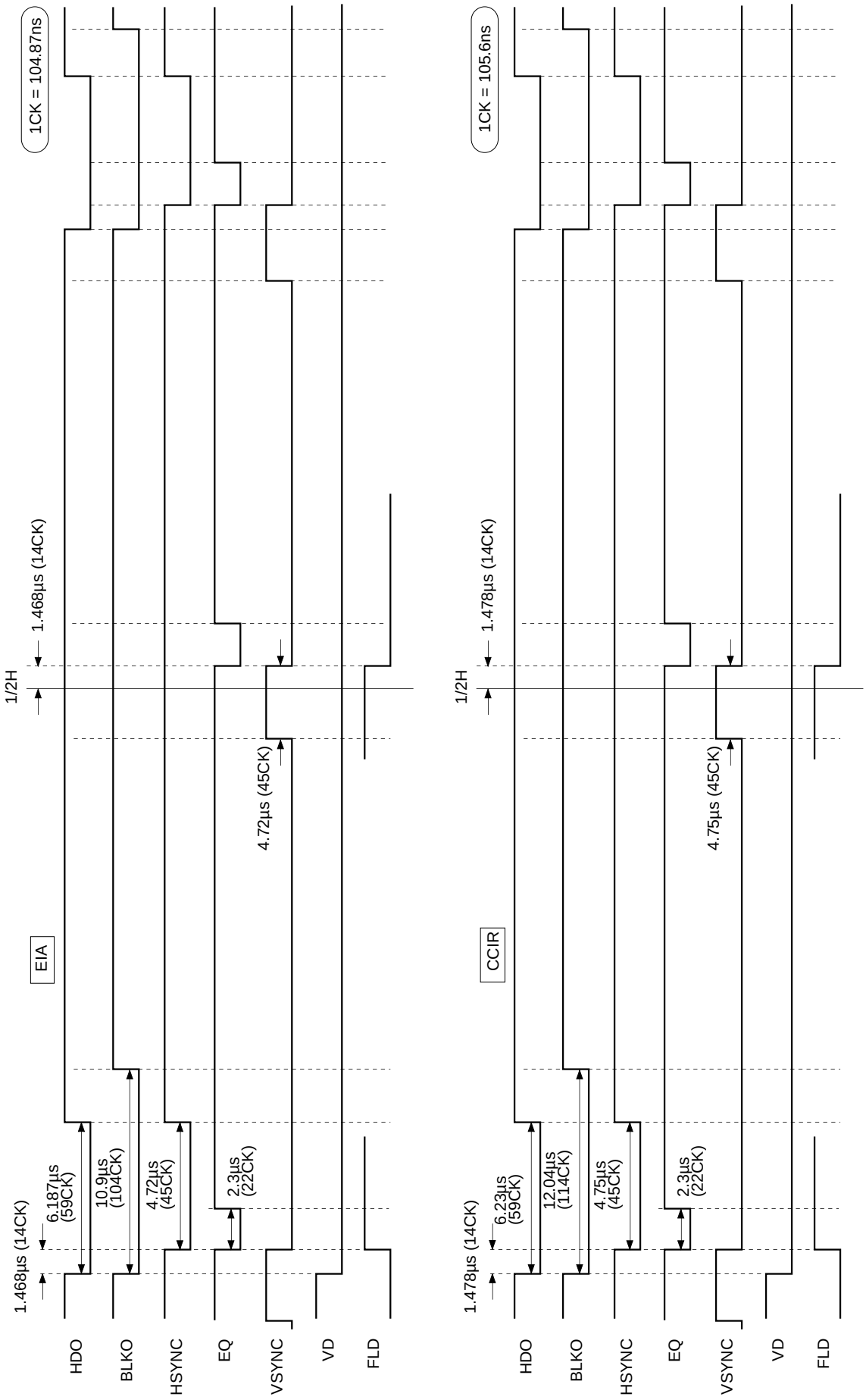
TG+SG Timing Chart

ICX054AL

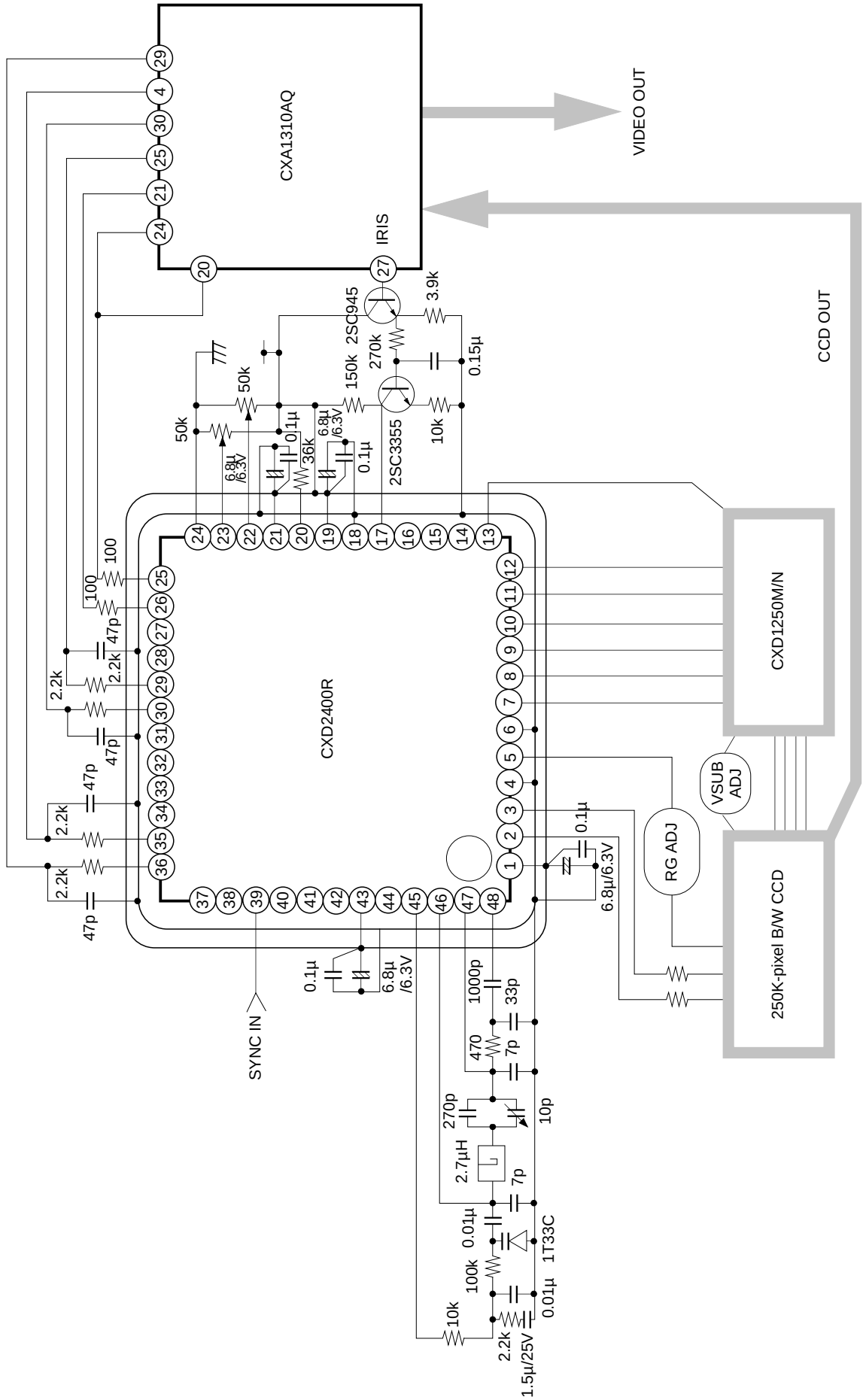


TG+SG High-Speed Phase Timing Chart

H effective period



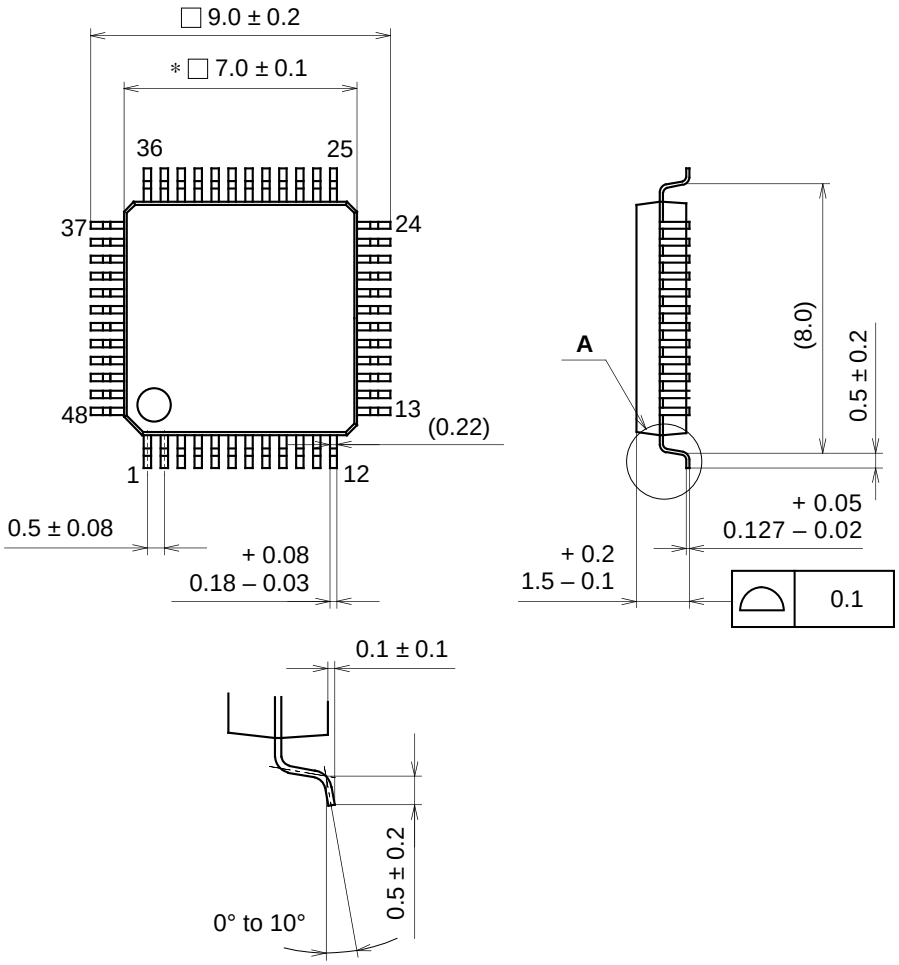
Application
<Sync input external synchronization + CCD iris mode>



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Package Outline Unit: mm

48PIN LQFP (PLASTIC)



DETAIL **A**

NOTE: Dimension "∗" does not include mold protrusion.

SONY CODE	LQFP-48P-L01
EIAJ CODE	LQFP048-P-0707
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER/PALLADIUM PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	0.2g