High Frequency Switch Mode Li-Ion Battery Charger

Preliminary Technical Data — ADP3804

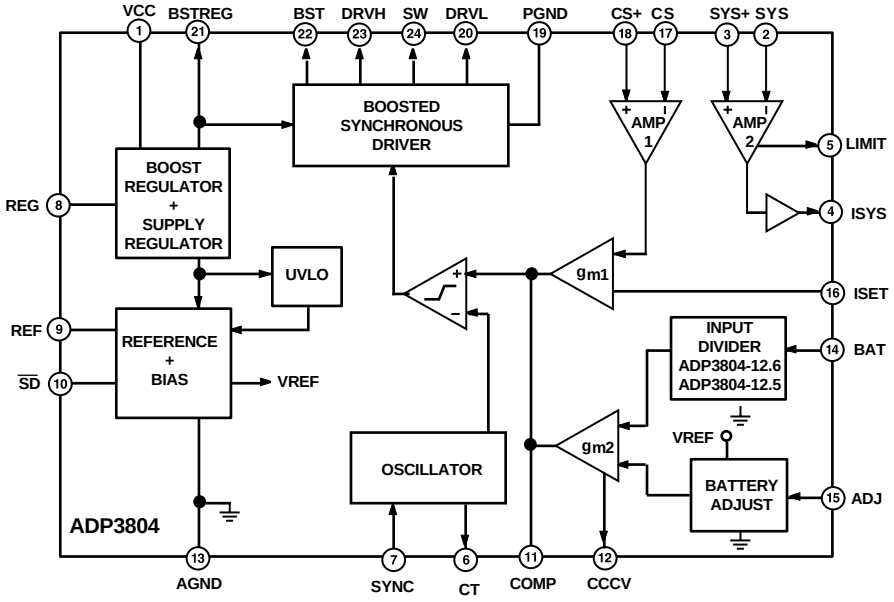
FEATURES
Li-Ion Battery Charger
Fixed 12,525 V, 12.600 V, or Adjustable Battery Voltage
High End-of-Charge Voltage Accuracy
±0.4% @ +25°C
±0.6% @ 5°C to 55°C
±0.75% @ 0°C to 85°C
Programmable Charge Current with Rail-to-Rail Sensing
System Current Sense with Reverse Input Protection
Softstart Charge Current
Undervoltage Lockout
Boosted Synchronous Drive For External NMOS
Programmable Oscillator Frequency
Oscillator SYNC Pin
Constant Current/Constant Voltage Flag
Trickle Charge

APPLICATIONS
Portable Computers
Fast Chargers

GENERAL DESCRIPTION

The ADP3804 is a complete Li-Ion battery charging IC. The device combines high output voltage accuracy with constant current control to simplify the implementation of Constant-Current, Constant-Voltage (CCCV) chargers. The ADP3804 is available in two options. The ADP3804-12.6 guarantees the final battery voltage to 12.6 V ± 0.6%, the ADP3804-12.5 guarantees 12.525 V ± 0.6% and the ADP3804 is adjustable using two external resistors to set the battery voltage. The current sense amplifier has rail-to-rail inputs to accurately operate under low drop out and short circuit conditions. The charge current is programmable with a DC voltage on ISET. A second differential amplifier senses the system current across an external sense resistor and outputs a linear voltage on the ISYS pin. The boosted synchronous driver allows the use of two NMOS transistors for lower system cost.

FUNCTIONAL BLOCK DIAGRAM



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ADP3804–SPECIFICATIONS[1] (@ 0°C ≤ T_A ≤ 100°C, VCC =16 V, unless otherwise noted)

Parameter	Conditions	Symbol	Min	Typ	Max	Units
BATTERY SENSE INPUT ADP3804-12.6						
V_{BAT}	T_A = +25°C	V_{BAT}	12.550	12.6	12.650	V
V_{BAT}	5°C ≤ T_A ≤ 55°C	V_{BAT}	12.524		12.676	V
V_{BAT}	0°C ≤ T_A ≤ 85°C	V_{BAT}	12.505		12.695	V
V_{BAT}	0°C ≤ T_A ≤ 100°C	V_{BAT}	12.474		12.726	V
Input Resistance	Part in Operation	R_{BAT}	400	500		kΩ
Input Current	Part in Shutdown	$I_{BAT(SD)}$		0.2	1.0	µA
BATTERY SENSE INPUT ADP3804-12.5						
V_{BAT}	T_A = +25°C	V_{BAT}	12.475	12.525	12.575	V
V_{BAT}	5°C ≤ T_A ≤ 55°C	V_{BAT}	12.450		12.600	V
V_{BAT}	0°C ≤ T_A ≤ 85°C	V_{BAT}	12.430		12.620	V
V_{BAT}	0°C ≤ T_A ≤ 100°C	V_{BAT}	12.400		12.650	V
Input Resistance	Part in Operation	R_{BAT}	400	500		kΩ
Input Current	Part in Shutdown	$I_{BAT(SD)}$		0.2	1.0	µA
BATTERY SENSE INPUT ADP3804						
V_{BAT}	T_A = +25°C	V_{BAT}	2.490	2.500	2.510	V
V_{BAT}	0°C ≤ T_A ≤ 85°C	V_{BAT}	2.481		2.519	V
V_{BAT}	0°C ≤ T_A ≤ 100°C	V_{BAT}	2.475		2.525	V
Input Current				0.2	1.0	µA
OSCILLATOR						
Maximum Frequency[2]		f_{CT}	1000			kHz
Frequency Variation[3]	CT = 150 pF	f_{CT}	215	250	285	kHz
CT Charge Current		I_{CT}	130	150	170	µA
0% Duty Cycle Threshold	@ COMP Pin			1.0		V
Maximum Duty Cycle Threshold	@ COMP Pin			2.5		V
SYNC Input High		$SYNC_H$	2.0			V
SYNC Input Low		$SYNC_L$			0.8	V
SYNC Input Current		I_{SYNC}		0.2	1.0	µA
GATE DRIVE						
On Resistance	I_L = 10 mA	R_{ON}		6	10	Ω
Rise, Fall Time	C_L = 1 nF, DRVL and DRVH	t_r, t_f		35		ns
Overlap Protection Delay	DRVL Falling to DRVH Rising, DRVH Falling to DRVL Rising	t_{OP}		50		ns
SW Bias Current	Part in Shutdown, V_{SW} = 12.6 V			0.2	1.0	µA
CURRENT SENSE AMPLIFIER						
Input Common-mode Range	V_{CS+} and V_{CS-}	$V_{CS(CM)}$	0.0		VCC+0.3	V
Input Differential Mode Range	V_{CS}[4]	$V_{CS(DM)}$	0.0		160	mV
Input Offset Voltage[5]	0 V ≤ $V_{CS(CM)}$ ≤ VCC	$V_{CS(VOS)}$		1.0		mV
Gain[5]				25		V/V
Input Bias Current	0 V ≤ $V_{CS(CM)}$ ≤ VCC, Part in Operation	$V_{CS(IB)}$		50	100	µA
Input Offset Current	0 V ≤ $V_{CS(CM)}$ ≤ VCC	$V_{CS(IOS)}$		1.0	2.0	µA
Input Bias Current	Part in Shutdown			0.2	1.0	µA
SYSTEM CURRENT SENSE[6]						
Input Common Mode Range	SYS+ and SYS-	$V_{SYS(CM)}$	4.0		VCC+0.3	V
Input Differential Range	(V_{SYS+}) - (V_{SYS-})	$V_{SYS(DM)}$	0		100	mV
Input Offset Voltage				1.0	2.0	mV
Input Bias Current, SYS+	$V_{SYS(DM)}$ = 0 V, $V_{SYS(CM)}$ = 16 V	$I_{B(SYS+)}$		50	100	µA
Input Bias Current, SYS-	$V_{SYS(DM)}$ = 0 V, $V_{SYS(CM)}$ = 16 V	$I_{B(SYS-)}$		25	50	µA
Voltage Gain	10 V ≤ $V_{SYS(CM)}$ ≤ VCC + 0.3V		48	50	52	V/V
Output Range	I_L = 1 mA[7], $V_{SYS(CM)}$ > 6 V	V_{ISYS}	0		5.0	V
Limit Output Threshold		$V_{TH(LIMIT)}$	2.4	2.5	2.6	V
Limit Output Voltage	V_{ISYS} > $V_{TH(LIMIT)}$, I_{SINK} = 1 mA	$V_{O(LIMIT)}$		0.1	0.2	V

Parameter	Conditions	Symbol	Min	Typ	Max	Units
ISET INPUT						
Charge Current Programming Function	0.0 V < V_{ISET} ≤ 4.0 V	V_{ISET}/V_{CS}		25		V/V
Programming Function Accuracy	V_{ISET} = 4.0 V		–5	±1.0	+5	%
	V_{ISET} = 0.50 V,		–20	±10	+20	%
ISET Bias Current	0.0 V ≤ V_{ISET} ≤ 4.0 V	I_B		0.2	1.0	µA
ADJ INPUT						
V_{BAT} Adjustment	V_{ADJ} = 1 V		–4.8	–5.0	–5.2	%
V_{BAT} Adjustment	V_{ADJ} = 4 V		+4.8	+5.0	+5.2	%
V_{BAT} Disable Threshold			4.4	4.6		V
ADJ Bias Current	1.0 V ≤ V_{ADJ} ≤ 4.0 V			0.2	1.0	µA
BOOST REGULATOR OUTPUT						
Output Voltage	C_L = 0.1 µF	V_{BSTREG}	6.8	7.0	7.2	V
Output Current		I_{BSTREG}	3	5		mA
ANALOG REGULATOR OUTPUT						
Output Voltage	C_L = 10 nF	V_{REG}	5..8	6.0	6.2	V
Output Current		I_{REG}	3.0	5.0		mA
PRECISION REFERENCE OUTPUT						
Output Voltage		V_{REF}	2.475	2.5	2.525	V
Output Current		I_{REF}	0.5	1.1		mA
SHUTDOWN ($\overline{SD}$)						
ON		$\overline{SD}_H$	2.0			V
OFF		$\overline{SD}_L$			0.8	V
$\overline{SD}$ Input Current				0.2	1.0	µA
POWER SUPPLY						
ON Supply Current	No External Loads	I_{SYON}		8.0	10	mA
OFF Supply Current	No External Loads	I_{SYOFF}		2.0	10	µA
UVLO Threshold Voltage	Turn On	V_{UVLO}	5.75	6.0	6.25	V
UVLO Hysteresis	Turn Off		0.1	0.3	0.5	V
CCCV OUTPUT						
Output Voltage Low	Constant Current Mode[8], V_{ISET} = 2.5 V, I_{SINK} = 100 µA			0.1	0.4	V
Output Voltage High	Constant Voltage Mode[9], V_{ISET} = 2.5 V			external		V
OUTPUT REVERSE LEAKAGE PROTECTION						
Leakage Current	VCC = Floating, V_{BAT} = 12.6 V	I_{DISCH}		3.0	10	µA

[1] All limits at temperature extremes are guaranteed via correlation using standard Statistical Quality Control (SQC) methods.
[2] Guaranteed by design, not tested in production.
[3] If SYNC function is used, then f_{SYNC} must be greater than f_{CT}, but less than 120% of f_{CT}.
[4] $V_{CS} = (V_{CS+}) - (V_{CS-})$.
[5] Accuracy guaranteed by ISET INPUT, Programming Function Accuracy specification.
[6] System current sense is active during shutdown.
[7] Load current is supplied through SYS+ pin.
[8] V_{BAT} < 95% of final or VCS > 80% of ISET programmed value.
[9] V_{BAT} ≥ 95% of final and VCS ≤ 80% of ISET programmed value.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Input Voltage (VCC to GND) ..... –0.3 V to +25 V
BAT, CS+, CS– to GND ..... –0.3 V to VCC+0.3 V
SYS+, SYS– to GND ..... –25 V to +25 V
BST to PGND ..... –0.3 V to +30 V
BST to SW ..... –0.3 V to +8 V
SW to PGND ..... –4 V to +25 V
DRVL to PGND ..... –0.3 V to +8 V
ISET, ADJ, CCCV, $\overline{SD}$, SYNC, CT,
LIMIT, ISYS TO GND ..... –0.3 V to +10 V
COMP ..... –0.3 V to +3 V
GND to PGND ..... –0.3 V to +0.3 V
Operating Ambient Temperature Range ..... 0°C to 100°C
θ_{JA} ..... 115°C/W
Operating Junction Temperature Range ..... 0°C to +125°C
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature Range (Soldering 10 sec) ..... +300°C

NOTES

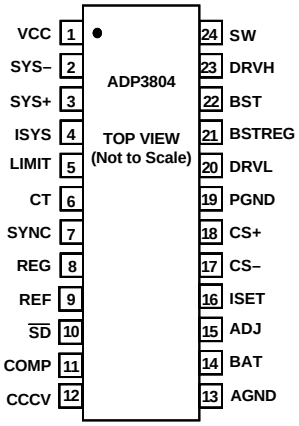
*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

θ_{JA} is specified for worst case conditions with device soldered on a circuit board.

ORDERING GUIDE

Model	Battery Voltage	Package Description	Package Option
ADP3804JRU	Adjustable	TSSOP-24	RU-24
ADP3804JRU-12.5	12.525 V	TSSOP-24	RU-24
ADP3804JRU-12.6	12.600 V	TSSOP-24	RU-24

PIN CONFIGURATION
24 Lead TSSOP



PIN FUNCTION DESCRIPTIONS

Pin Number	Mnemonic	Function
1	VCC	Supply Voltage.
2	SYS–	Negative System Current Sense Input.
3	SYS+	Positive System Current Sense Input.
4	ISYS	System Current Sense Output.
5	LIMIT	System Current Sense Limit Output.
6	CT	Oscillator Timing Capacitor.
7	SYNC	Oscillator Synchronization Pin.
8	REG	6.0 V Analog Regulator Output.
9	REF	2.5 V Precision Reference Output.
10	$\overline{SD}$	Shutdown Control Input.
11	COMP	External Compensation Node.
12	CCCV	Constant Current/Constant Voltage Output.
13	AGND	Analog Ground.
14	BAT	Battery Sense Input. 2.5 V for ADP3804, 12.525 V for ADP3804-12.5 or 12.6 V for ADP3804-12.6
15	ADJ	Battery Voltage Adjust Input.
16	ISET	Charge Current Program Input.
17	CS–	Negative Current Sense Input.
18	CS+	Positive Current Sense Input.
19	PGND	Power Ground.
20	DRVL	Low Drive Output switches between REG and PGND.
21	BSTREG	7.0 V Regulator Output for Boost.
22	BST	Floating Bootstrap Supply for DRVH.
23	DRVH	High Drive Output switches between SW and BST.
24	SW	Buck Switching Node Reference for DRVH.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the device features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

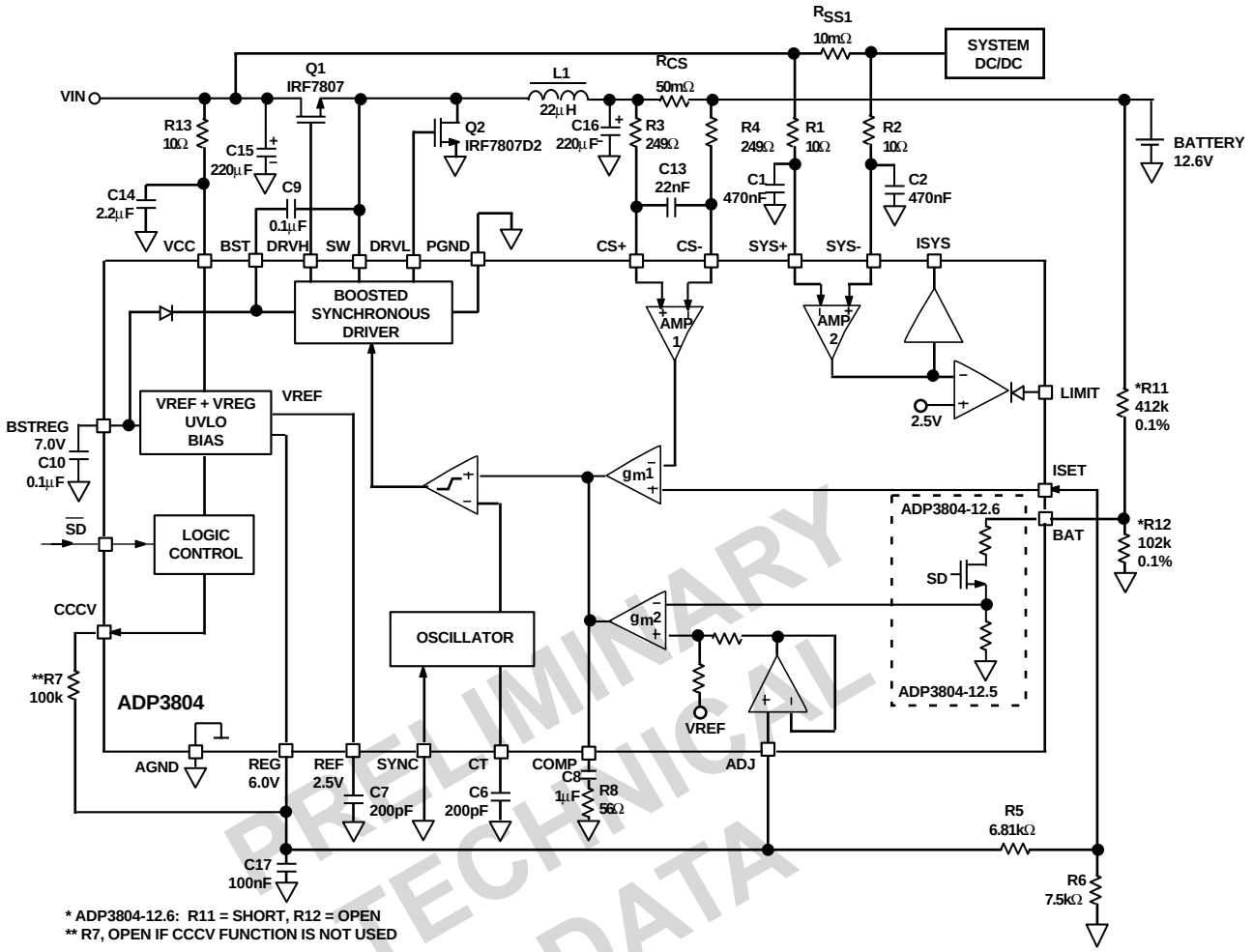


Figure 1. Typical Application

THEORY OF OPERATION

The ADP3804 combines a boosted synchronous switching driver with programmable current control and accurate final battery voltage control in a Constant Current, Constant Voltage (CCCV) Li-Ion battery charger. High accuracy voltage control is needed to safely charge Li-Ion batteries, which are typically specified at 4.2 V ± 1% per cell. For a typical notebook computer battery pack, three cells are in series giving a total voltage of 12.6 V. The ADP3804 is available in three versions, a fixed 12.525 V output, a fixed 12.6 V output and an adjustable output. The adjustable output is useful for charging batteries with slightly different chemistry that result in a final battery voltage slightly higher or lower than 4.2 V/ cell.

Another requirement for safely charging Li-Ion batteries is accurate control of the charge current. The actual charge current depends on the number of cells in parallel within the battery pack. Typically this is in the range of 2 A to 3 A. The ADP3804 provides flexibility in programming the charge current over a wide range. An external resistor is used to sense the charge current and this voltage is compared to a DC input voltage. This programmability allows the current to be changed during charging. For example, the charge current can be reduced for trickle charging.

The synchronous driver provides high efficiency when charging at high currents. Efficiency is important mainly to reduce the amount of heat generated in the charger, but also to stay within the power limits of the AC adapter. With the addition of a boosted high side driver, the ADP3804 drives two external power NMOS transistors for a simple, lower cost power stage.

The ADP3804 also provides an uncommitted current sense amplifier. This amplifier provides an analog output pin for monitoring the current through an external sense resistor. The amplifier can be used anywhere in the system that high side current sensing is needed.

Charge Current Control

AMP1 in Figure 1 has a differential input to amplify the voltage drop across an external sense resistor R_{CS}. The input common mode range is from ground to VCC allowing current control in short circuit and low drop-out conditions. The gain of AMP1 is internally set to 25 V/V for low voltage drop across the sense resistor. During CC mode, g_{m1} forces the voltage at the output of AMP1 to be equal to the external voltage at the ISET pin. By choosing R_{CS} and V_{ISET} appropriately, a wide range of charge currents can be programmed:

$$I_{CHARGE} = \frac{V_{ISET}}{25 \cdot R_{CS}} \quad (1)$$

Typical values of R_{CS} are in the range from 25 mΩ to 50 mΩ, and the input range of ISET is from 0 V to 4 V. If, for example, a 2 A charger is required, then R_{CS} could be set to 50 mΩ and V_{ISET} = 2.5 V. The power dissipation in R_{CS} should be kept below 500 mW. In this example, the power is a maximum of 200 mW. Once R_{CS} has been chosen, the charge current can be adjusted during operation with V_{ISET}. Lowering V_{ISET} to 125 mV gives a charge current of 100 mA for trickle charging. Components R3, R4, and C13 provide high frequency filtering for the current sense signal.

Final Battery Voltage Control

As the battery approaches its final voltage, the ADP3804 switches from CC mode to CV mode. The change is achieved by the common output node of g_{m1} and g_{m2}. Only one of the two outputs controls the voltage at the COMP pin. Both amplifiers can only pull down on COMP, such that when either amplifier has a positive differential input voltage, its output is not active. For example, when the battery voltage, V_{BAT}, is low, g_{m2} does not control V_{COMP}. When the battery voltage reaches the desired final voltage, g_{m2} takes control of the loop, and the charge current is reduced.

Amplifier g_{m2} compares the battery voltage to the internal reference voltage of 2.5 V. In the case of the ADP3804-12.5 and ADP3804-12.6, an internal resistor divider sets the final battery voltage to 12.6 V. In contrast, the ADP3804 requires external, precision resistors. The divider ratio should be set to divide the desired final voltage down to 2.5 V at the BAT pin:

$$\frac{R_{11}}{R_{12}} = \frac{V_{BATTERY}}{2.5V} - 1 \qquad (2)$$

These resistors should be high impedance to limit the battery leakage current. Alternatively, an external NMOS can be added in series with R12 to turn off during shutdown. In the case of the ADP3804-12.5 and ADP3804-12.6, an internal MOSFET disconnects the internal divider to reduce the leakage current into BAT to less than 1 µA during shutdown. If the ADP3804-12.5 or ADP3804-12.6 is used, then R11 should be shorted and R12 open. The reference and internal resistor divider are referenced to the AGND pin, which should be connected close to the negative terminal of the battery to minimize sensing errors.

Final Battery Voltage Adjust

The ADJ pin provides an analog input to adjust the final battery voltage by ± 5%. Figure 2 shows the control curve for this amplifier. Above the threshold voltage of 4.6 V, the amplifier is turned off. Thus, to disable this function, ADJ should be connected to REG. In the linear range between 1 V and 4 V, the percentage change in V_{BAT} is a function V_{ADJ} as follows:

$$\Delta V_{BAT}(\%) = 100 \cdot \frac{V_{ADJ} - 2.5V}{30} \qquad (3)$$

This percent change is the same for the ADP3804 (2.5 V output) and the ADP3804-12.6.

Oscillator and PWM

The oscillator generates a triangle waveform between 1 V and 2.5 V, which is compared to the voltage at the COMP pin, setting the duty cycle of the driver stage. When V_{COMP} is below 1 V, the duty cycle is zero. Above 2.5 V, the duty cycle reaches its maximum. The ADP3804 forces a minimum off time of approximately 200 nsec to ensure that the boost capacitor is always charged. This off time sets the maximum duty cycle. For example, a 200 kHz frequency (5 µsec period) gives a maximum duty cycle of 96%.

The oscillator frequency is set by the external capacitor at the CT pin and the internal current source of 150 µA according to the following formula:

$$f_{OSC} = \frac{150\mu A}{2 \cdot CT \cdot 1.5V} \qquad (4)$$

A 200 pF capacitor sets the frequency to 250 kHz. The frequency can also be synchronized to an external oscillator by applying a square wave input on SYNC. The SYNC function is designed to allow only increases in the oscillator frequency. The f_{SYNC} should be no more than 20% higher than f_{OSC}. The duty cycle of the SYNC input is not important and can be anywhere between 5% and 95%.

7V Boost Regulator

The driver stage is powered by the internal 7V boost regulator, which is available at the BSTREG pin. Because the switching currents are supplied by this regulator, decoupling must be added. A 0.1 µF capacitor should be placed close to the ADP3804, with the ground side connected close to the power ground pin, PGND. This supply is not recommended for use externally due to high switching noise.

Boosted Synchronous Driver

The PWM comparator controls the state of the synchronous driver. A high output from the PWM comparator forces DRVH on and DRVL off. The drivers have an ON resistance of approximately 5 Ω for fast rise and fall times when driving external MOSFETs. Furthermore, the boosted drive allows an external NMOS transistor for the main switch instead of a PMOS. A boost diode is internally connected between BSTREG and BST, and a boost capacitor of 0.1 µF must be added externally between BST and SW. The voltage between BST and SW is typically 6 V.

The DRVL pin switches between BSTREG and PGND. The 7 V output of BSTREG drives the external NMOS with high VGS to lower the ON resistance. PGND should be connected close to the source pin of the external synchronous NMOS. When DRVL is high, this turns on the lower NMOS and pulls the SW node to ground. At this point, the boost capacitor is charged up through the internal boost diode. When the PWM switches high, DRVL is turned off and DRVH turns on. DRVH switches between BST and SW. When DRVH is on, the SW pin is pulled up to the input supply (typically 16 V), and BST rises above this voltage by approximately 6 V.

Overlap protection is included in the driver to ensure that both external MOSFETs are not on at the same time. When DRVH turns off the upper MOSFET, the SW node goes low due to the inductor current. The ADP3804 monitors the SW voltage, and turns on DRVL when SW goes below 1 V. If, under low current loads, the SW voltage does not drop below 1 V, DRVL will turn on after time-out of 200 nsec. When DRVL turns off, an internal timer adds a delay of 50 nsec before turning DRVH on.

2.5 V Precision Reference
The voltage at the BAT pin is compared to an internal precision, low temperature drift reference of 2.5 V. The reference is available externally at the REF pin. This pin should be bypassed with a 100 pF capacitor to the analog ground pin, AGND. The reference can be used as a precision voltage externally. However, the current draw should not be greater than 100 µA, and no noisy, switching type loads should be connected.

6 V Regulator
The 6 V regulator supplies power to most of the analog circuitry on the ADP3804. This regulator should be bypassed to AGND with a 10 nF capacitor. This reference has a 3 mA source capability to power external loads if needed.

CCCV
An open drain output is available to signal when the ADP3804 switches from CC to CV charging. An external pull-up resistor of 100 kΩ to REG or other pull-up voltage is required for this function. If the CCCV signal is not needed, the pin should be left open. The CCCV function uses two comparators to monitor the battery voltage and the charge current. In order for the CCCV pin to go high, signaling CV mode, the battery voltage must be higher than 95% of its final value, and the current must be less than 80% of its programmed value. If the battery voltage is less than 95% then CCCV will be low regardless of the actual current flowing. This is to prevent a false output during startup when the current is low.

System Current Sense
An uncommitted differential amplifier is provided for additional high side current sensing. This amplifier, AMP2, has a fixed gain of 50 V/V from the SYS+ and SYS- pins to the analog output at ISYS. ISYS has a 1 µA source capability to drive an external load. The common mode range of the input pins is from 4 V to VCC. This amplifier is the only part of the ADP3804 that remains active during shutdown. The power to this block is derived from the bias current on the SYS+ and SYS- pins.

A separate comparator is included to provide a flag when the voltage at ISYS rises above 2.5 V. The open drain output is capable of sinking 1 µA when the threshold is exceeded. This comparator is turned off during shutdown to conserve power.

Shutdown
A high impedance CMOS logic input is provided to turn off the ADP3804. When the voltage on $\overline{SD}$ is less than 0.8 V, the ADP3804 is placed in low power shutdown. With the exception of the system current sense amplifier, AMP2, all other circuitry is turned off. The reference and regulators are pulled to ground during shutdown and all switching is stopped. During this state, the supply current is less than 10 µA. Also, the BAT, CS+, CS-, and SW pins go to high impedance to minimize current drain from the battery.

UVLO
Under-Voltage Lock-Out, UVLO, is included in the ADP3804 to ensure proper start-up. As VCC rises above 1 V, the reference and regulators will track VCC until they reach their final voltages. However, the rest of the circuitry is held off by the UVLO comparator. The UVLO comparator monitors both regulators to ensure that they are above 5 V before turning on the main charger circuitry. This occurs when VCC reaches 6 V. Monitoring the regulator outputs makes sure that the charger circuitry and driver stage have sufficient voltage to operate normally. The UVLO comparator includes 300 mV of hysteresis to prevent oscillations near the threshold.

Startup Sequence
During a startup from either $\overline{SD}$ going high or VCC exceeding the UVLO threshold, the ADP3804 initiates a soft-start sequence. The soft-start timing is set by the compensation capacitor at the COMP pin and an internal 40 µA source. Initially, both DRVH and DRVL are held low until V_{COMP} reaches 1 V. This delay time is set by:

$$t_{DELAY} = \frac{C_{COMP} - 1V}{40\mu A} \quad (5)$$

For a 1 µF COMP capacitor, t_{DELAY} is 25 msec. After this initial delay, DRVL is turned on first for one period to give the boost capacitor time to charge up. The duty cycle then ramps up to its final value with the same ramp rate given for t_{DELAY}. For example, if V_{IN} is 16 V and the battery is 10 V when charging is started, the duty cycle will be approximately 65%, corresponding to a V_{COMP} of ~2 V. The time for the duty cycle to ramp from 0% at V_{COMP} = 1 V to 65% at V_{COMP} = 2 V is approximately 25 msec.

Loop Feed Forward
As the startup sequence discussion shows, the response time at COMP is slowed by the large compensation capacitor. To speed up the response, two comparators can quickly feed forward around the normal control loop and pull the COMP node to ground to limit any over shoot in either short circuit or over-voltage conditions. The over-voltage comparator has a trip point set to 20% higher than the final battery voltage. The over-current comparator threshold is set to 200 mV across the CS pins, which is 25% above the maximum programmable threshold. When these comparators are tripped, a normal soft-start sequence is initiated. This will give 0% duty cycle with DRVH off and DRVL on. The over-voltage comparator is valuable when the battery is removed during charging. In this case, the current in the inductor causes the output voltage to spike up, and the comparator limits the maximum voltage. Neither of these comparators affect the loop under normal charging conditions.