

MOS INTEGRATED CIRCUIT

μ PD78CP18(A)

8-BIT SINGLE-CHIP MICROCOMPUTER

DESCRIPTION

The μ PD78CP18(A) is a version of the μ PD78C18(A) in which the internal mask ROM is replaced by one-time PROM. The one-time PROM version can be programmed once only by users, and is ideally suited for small-scale of many different products, and rapid development and time-to-market of a new product.

The detailed functions are described in the following user's manual. Read this manual before starting design work.

87AD series μ PD78C18 user's manual: IEU-1314

FEATURES

- High reliability compared to the μ PD78CP18
- Compatible with the μ PD78C11A(A), 78C12A(A), 78C14(A), 78C18(A)
- Internal PROM: 32768 W \times 8
 - Internal PROM capacity can be changed by software to conform to the μ PD78C11A(A), 78C12A(A), 78C14(A), 78C18(A).
- PROM programming characteristics: μ PD27C256A compatible
- Power supply voltage range: 5 V \pm 10 %
- Supports QTOP™ microcomputer

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Remark QTOP microcomputer is the generic name of NEC's single-chip microcomputers for which NEC provides total service including writing, marking, screening, and inspection.

ORDERING INFORMATION

Part Number	Package	Internal ROM
μ PD78CP18GF(A)-3BE	64-pin plastic QFP (14 \times 20 mm)	One-time PROM
μ PD78CP18GQ(A)-36	64-pin plastic QIUP	One-time PROM

QUALITY GRADE

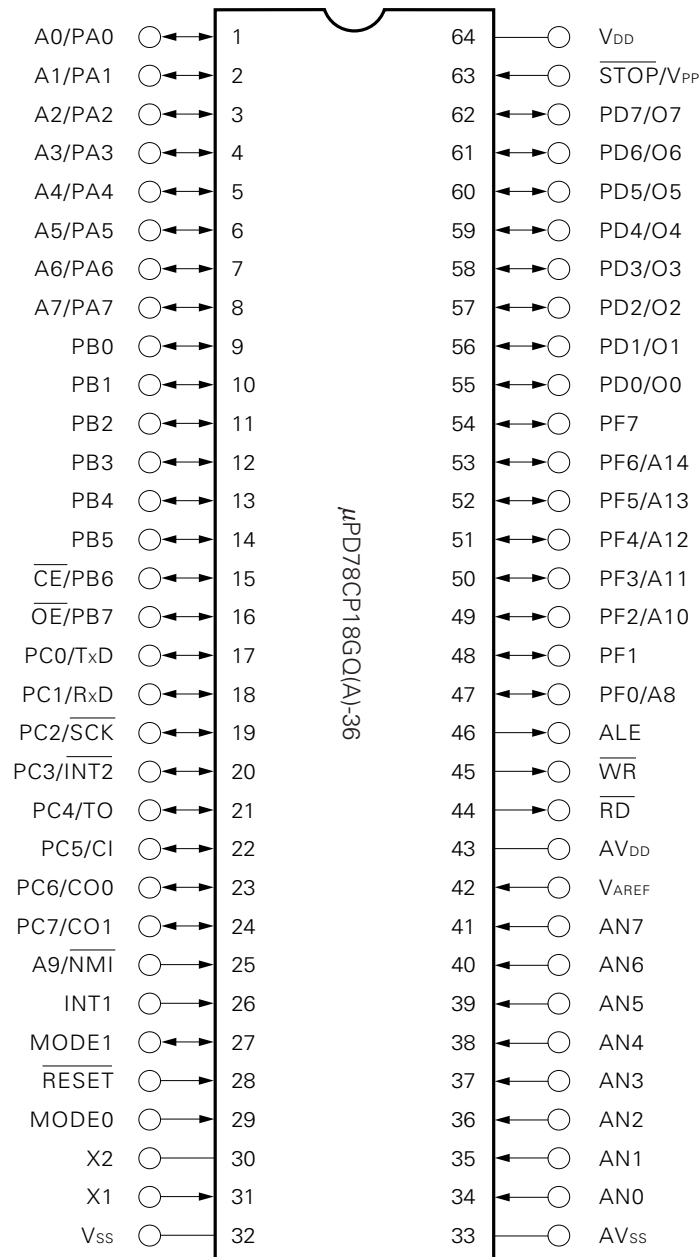
Part Number	Quality Grade
μ PD78CP18GF(A)-3BE	Special
μ PD78CP18GQ(A)-36	Special

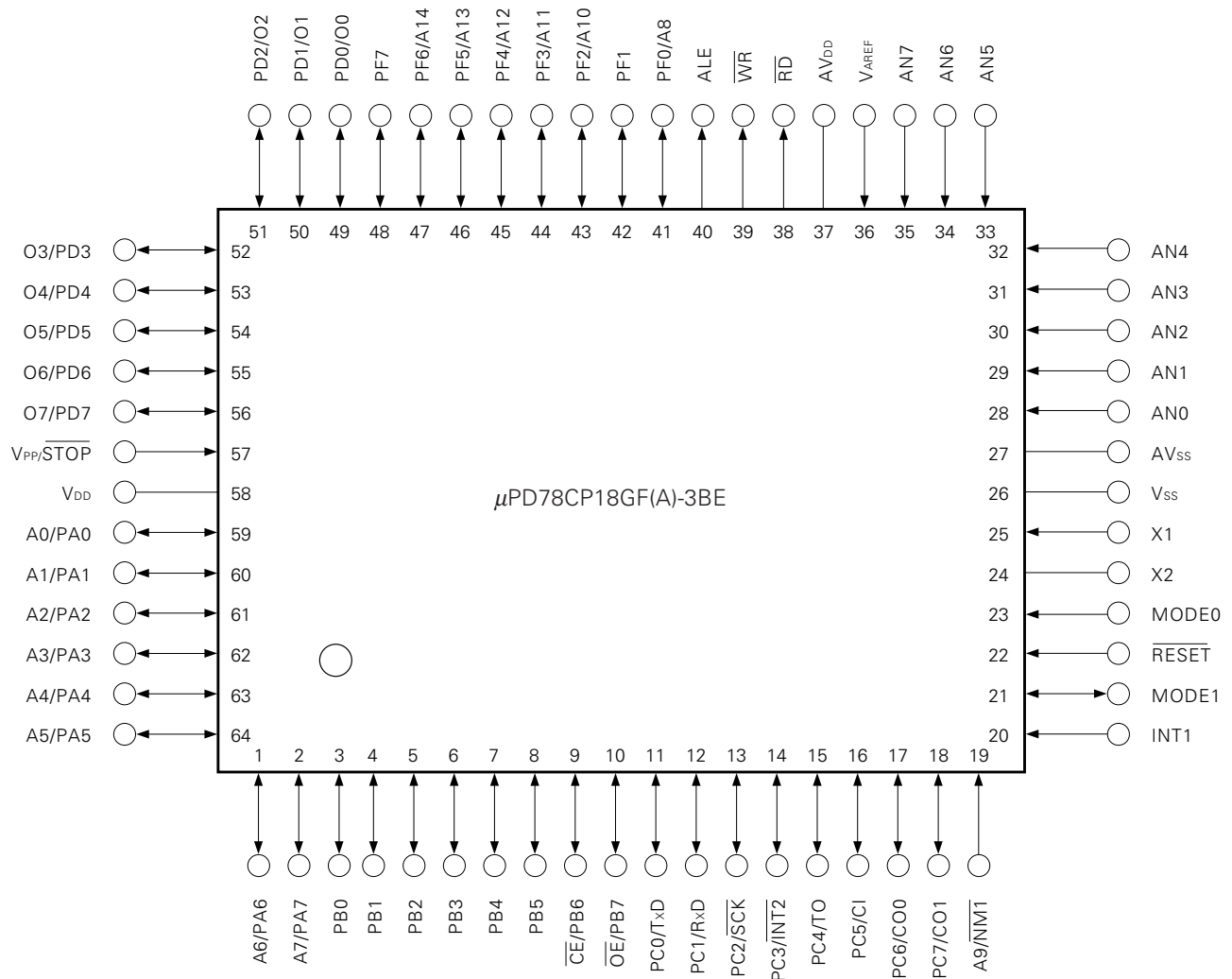
Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

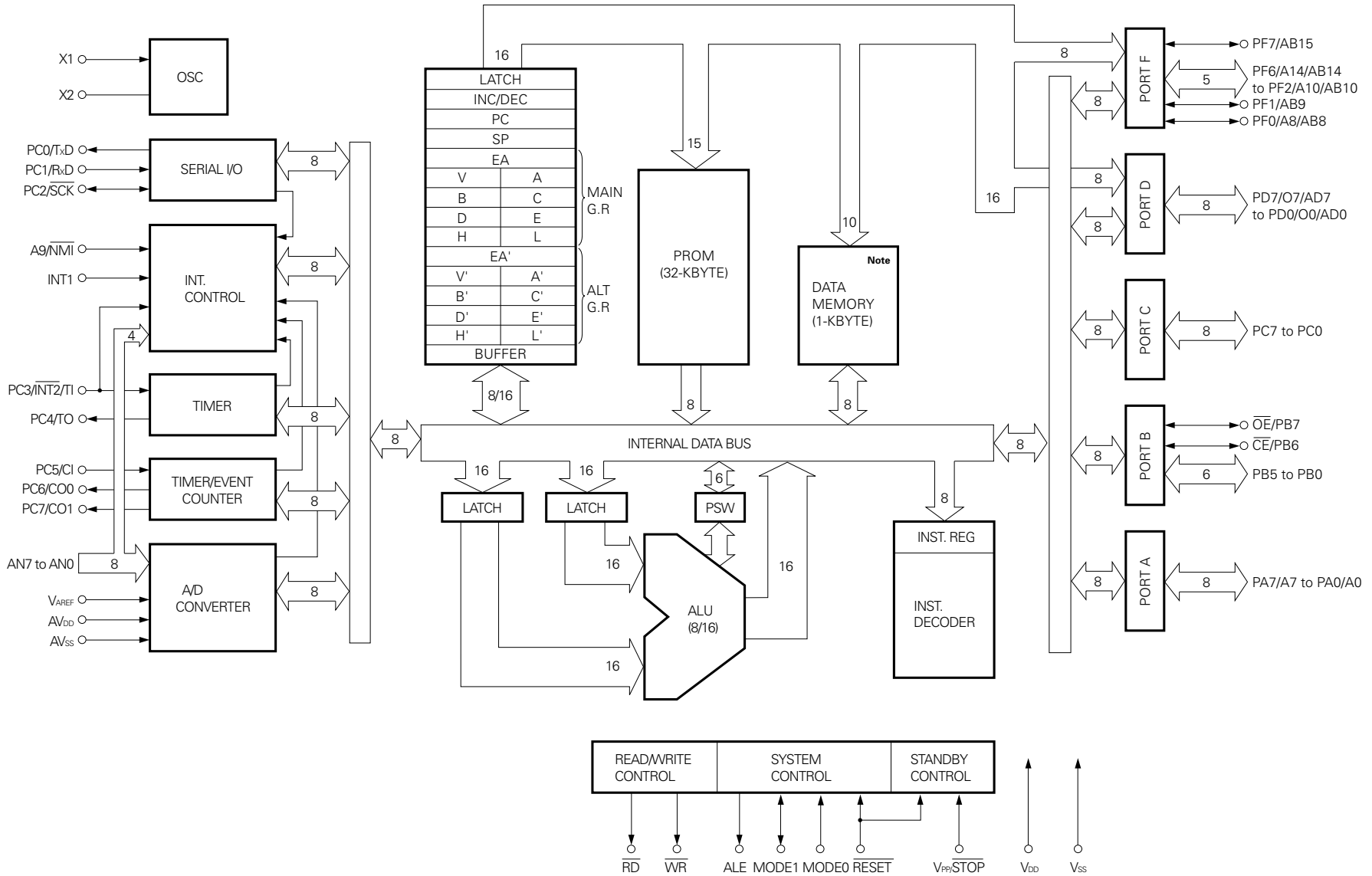
The information in this document is subject to change without notice.

The mark ★ shows major revised points.

PIN CONFIGURATION (TOP VIEW)







Note Can be used only when RAE bit of MM register is 1.
External memory is needed in case of 0.

DIFFERENCES BETWEEN THE μPD78CP18(A) AND μPD78CP18

Product Name Item	μPD78CP18(A)	μPD78CP18
Quality grade	Special	Standard
Electrical specifications	Input leakage current AN7 to AN0: ±1 μA (MAX.)	Input leakage current AN7 to AN0; ±10 μA (MAX.)
Package	<ul style="list-style-type: none"> • 64-pin plastic QFP (14 × 20 mm) • 64-pin plastic QUIP 	<ul style="list-style-type: none"> • 64-pin plastic shrink DIP (750 mil) • 64-pin plastic QUIP • 64-pin plastic QFP (14 × 20 mm) • 64-pin ceramic shrink DIP with window (750 mil) • 64-pin ceramic WQFN

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1. LIST OF PORT FUNCTIONS

1.1 PORT FUNCTIONS

Pin Name	I/O	Function
PA7 to PA0 (Port A)	Input/Output	8-bit input-output port, which can specify input/output bit-wise.
PB7 to PB0 (Port B)		
PC7 to PC0 (Port C)		
PD7 to PD0 (Port D)		8-bit input-output port, which can specify input/output in byte units.
PF7 to PF0 (Port F)		8-bit input-output port, which can specify input/output bit-wise.

Remark These port pins have alternate function pins as shown in 1.2 “NON-PORT FUNCTIONS (IN NORMAL OPERATION)” and 1.3 “NON-PORT FUNCTIONS (DURING PROM WRITE/VERIFY AND READ)”.

1.2 NON-PORT FUNCTIONS (IN NORMAL OPERATION)

Pin Name	I/O	Alternate Function Pin	Function
TxD (Transmit Data)	Output	PC0	Serial data output pin
RxD (Receive Data)	Input	PC1	Serial data input pin
$\overline{\text{SCK}}$ (Serial Clock)	Input/output	PC2	Serial clock input/output pin. Output when internal clock is used, input when external clock is used.
$\overline{\text{INT2}}$ (Interrupt Request)	Input	PC3	Edge trigger (falling edge) maskable interrupt input pin
Ti (Timer Input)	Input		Timer external clock input pin
Zero-cross	Input		AC input zero-cross detection pin
TO (Timer Output)	Output	PC4	During timer count time, square wave with one internal clock cycle as one half cycle is output.
CI (Counter Input)	Input	PC5	Timer/event counter external pulse input pin
CO0 and CO1 (Counter Output 0, 1)	Output	PC6 and PC7	Square wave output programmable by timer/event counter.
AD7 to AD0 (Address/Data Bus 7 to 0)	Input/output	PD7 to PD0	Multiplexed address/data bus when external memory is used
AB15 to AB8 (Address Bus 15 to 8)	Output	PF7 to PF0	Address bus when external memory is used
$\overline{\text{WR}}$ (Write Strobe)	Output		Strobe signal which is output for write operation of external memory. It becomes high in any cycle other than the data write machine cycle of external memory. When $\overline{\text{RESET}}$ signal is either low or in the hardware STOP mode, this signal becomes high-impedance.
$\overline{\text{RD}}$ (Read Strobe)	Output		Strobe signal which is output for read operation of external memory. It becomes high in any cycle other than the data read machine cycle of external memory. When $\overline{\text{RESET}}$ signal is either low or in the hardware STOP mode, this signal becomes output high-impedance.
ALE (Address Latch Enable)	Output		Strobe signal to latch externally the lower address information which is output to PD7 to PD0 pins to access external memory. When $\overline{\text{RESET}}$ signal is either low or in the hardware STOP mode, this signal becomes high-impedance.
MODE0 MODE1 (Mode)	Input Input/output		Set MODE0 pin to "0" (low level), and MODE1 pin to "1" (high level) ^{Note}
$\overline{\text{NMI}}$ (Non-Maskable Interrupt)	Input		Non-maskable interrupt input pin of the edge trigger (falling edge)

Note Pull-up. Pull-up resistor R is $4 \text{ [k}\Omega\text{]} \leq R \leq 0.4 \text{ t}_{\text{CYC}} \text{ [k}\Omega\text{]}$ (t_{CYC} is ns unit).

Pin Name	I/O	Alternate Function Pin	Function
INT1 (Interrupt Request)	Input		A maskable interrupt input pin of the edge trigger (rising edge). Also, it can be used as a zero-cross detection pin for AC input.
AN7 to AN0 (Analog Input)	Input		8 pins of analog input to A/D converter. AN7 to AN4 can be used as edge detection (falling edge) input.
V _{AREF} (Reference Voltage)	Input		A common pin serving both as a reference voltage input pin for A/D converter and as a control pin for A/D converter operation.
AV _{DD} (Analog V _{DD})			Power supply pin for A/D converter.
AV _{SS} (Analog V _{SS})			GND pin for A/D converter.
X1, X2 (Crystal)			Crystal connection pins for system clock oscillation. X1 should be input when a clock is supplied from outside. Inverted clock of X1 should be input in X2.
RESET (Reset)	Input		Low-level active system reset input.
STOP (Stop)	Input		Hardware STOP mode control signal input pin. When the low level is input to this pin, the oscillation stops.
V _{DD}			Positive power supply pin.
V _{SS}			GND pin.

1.3 NON-PORT FUNCTIONS (DURING PROM WRITE/VERIFY AND READ)

Pin Name	I/O	Alternate Function Pin	Function
A7 to A0	Input	PA7 to PA0	Address lower 8 bit input pins
\overline{CE}	Input	PB6	Chip enable signal input pin
\overline{OE}	Input	PB7	Output enable signal input pin
O7 to O0	Input/output	PD7 to PD0	Data input/output pins
A14 to A10	Input	PF6 to PF2	Address higher 7 bit input pins
A8		PF0	
A9		\overline{NMI}	
MODE0 MODE1	Input		Set MODE0 pin to "1" (high level), and MODE1 pin to "0" (low level).
\overline{RESET}	Input		Set to "0" (low level).
V _{PP}		\overline{STOP}	High-voltage application pin "1" (high level) is input when EPROM is read.

1.4 HANDLING OF UNUSED PINS

Pin	Recommended Connection
PA7 to PA0 PB7 to PB0 PC7 to PC0 PD7 to PD0 PF7 to PF0	Connect to V _{SS} or V _{DD} via resistor.
\overline{RD} \overline{WR} ALE	Leave open.
\overline{STOP}	Connect to V _{DD} .
INT1, \overline{NMI}	Connect to V _{SS} or V _{DD} .
AV _{DD}	Connect to V _{DD} .
V _{AREF} AV _{SS}	Connect to V _{SS} .
AN7 to AN0	Connect to AV _{SS} or AV _{DD} .

2. MEMORY CONFIGURATION

The μ PD78CP18(A) memory can operate in the following 4 modes according to the mode specification.

- μ PD78C11A mode (see **Figure 2-1**)
- μ PD78C12A mode (see **Figure 2-2**)
- μ PD78C14 mode (see **Figure 2-3**)
- μ PD78C18 mode (see **Figure 2-4**)

In addition, the internal PROM and internal RAM address ranges can be specified for efficient mapping of external memory (excluding PROM) (see **3.2 "MEMORY MAPPING REGISTER (MM)"**).

The vector area and call table area are common to all modes.

Setting the hardware/software STOP mode or HALT mode enables internal RAM data to be retained at a low consumption current.

Figure 2-1. Memory Map (μPD78C11A Mode)

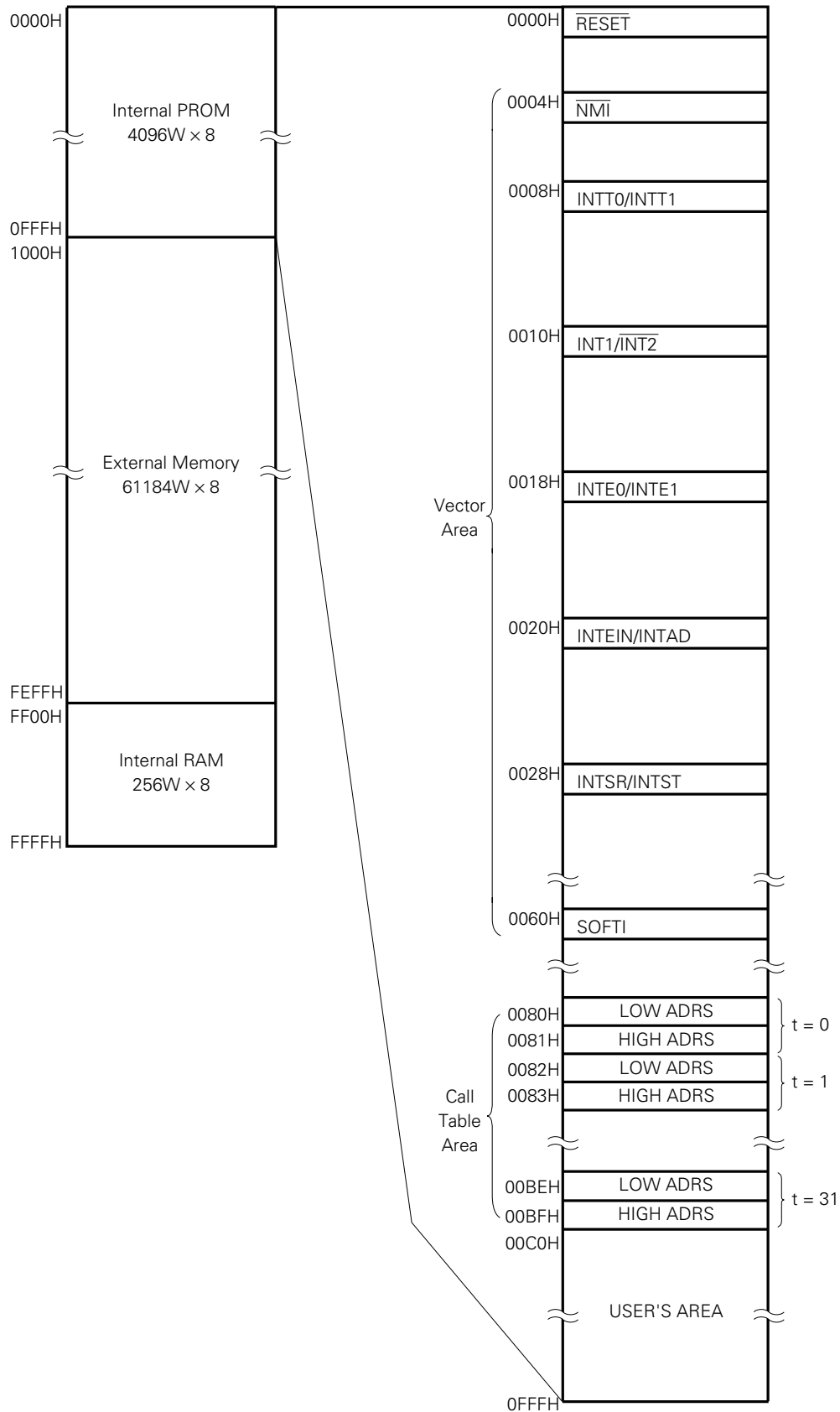


Figure 2-2. Memory Map (μPD78C12A Mode)

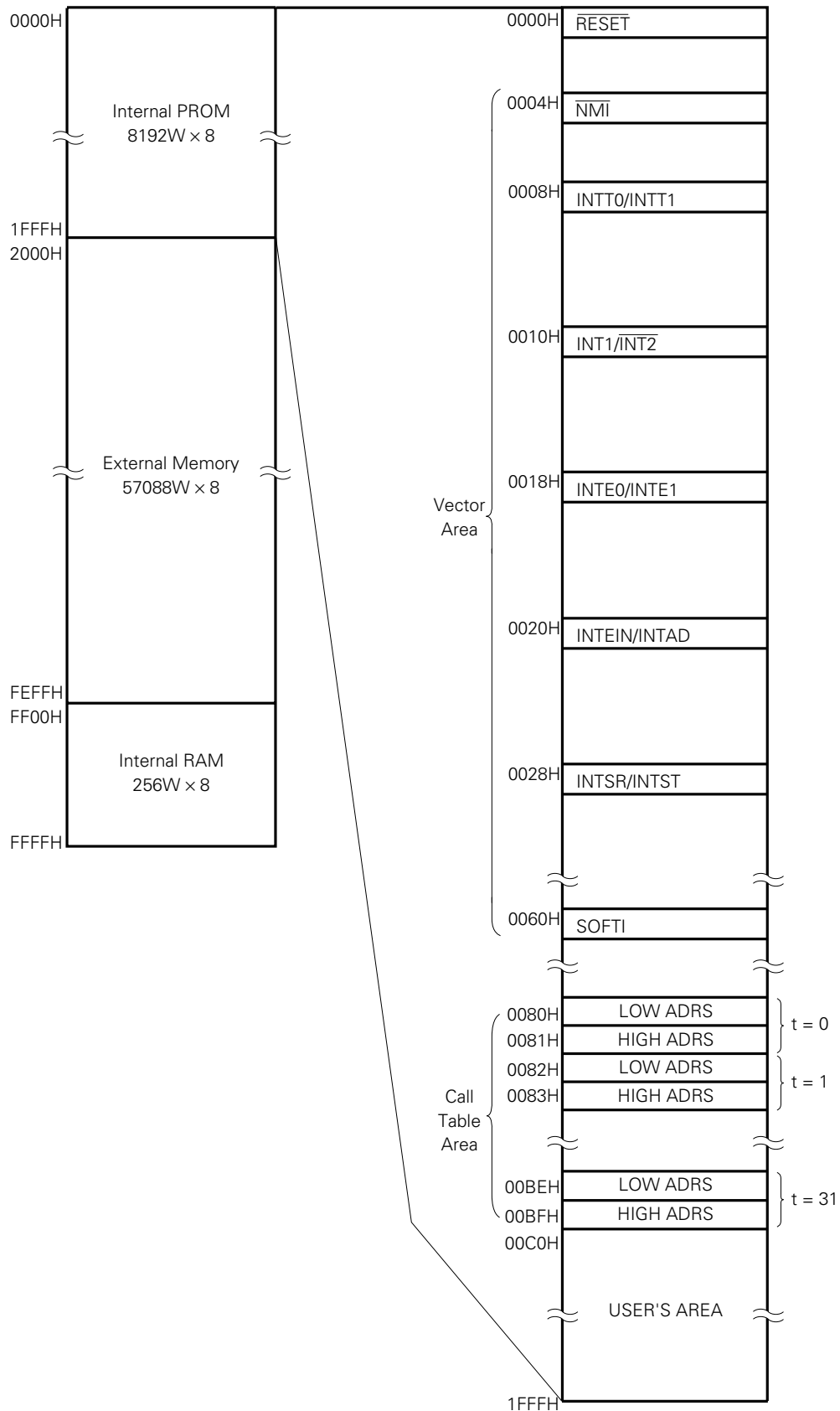


Figure 2-3. Memory Map (μPD78C14 Mode)

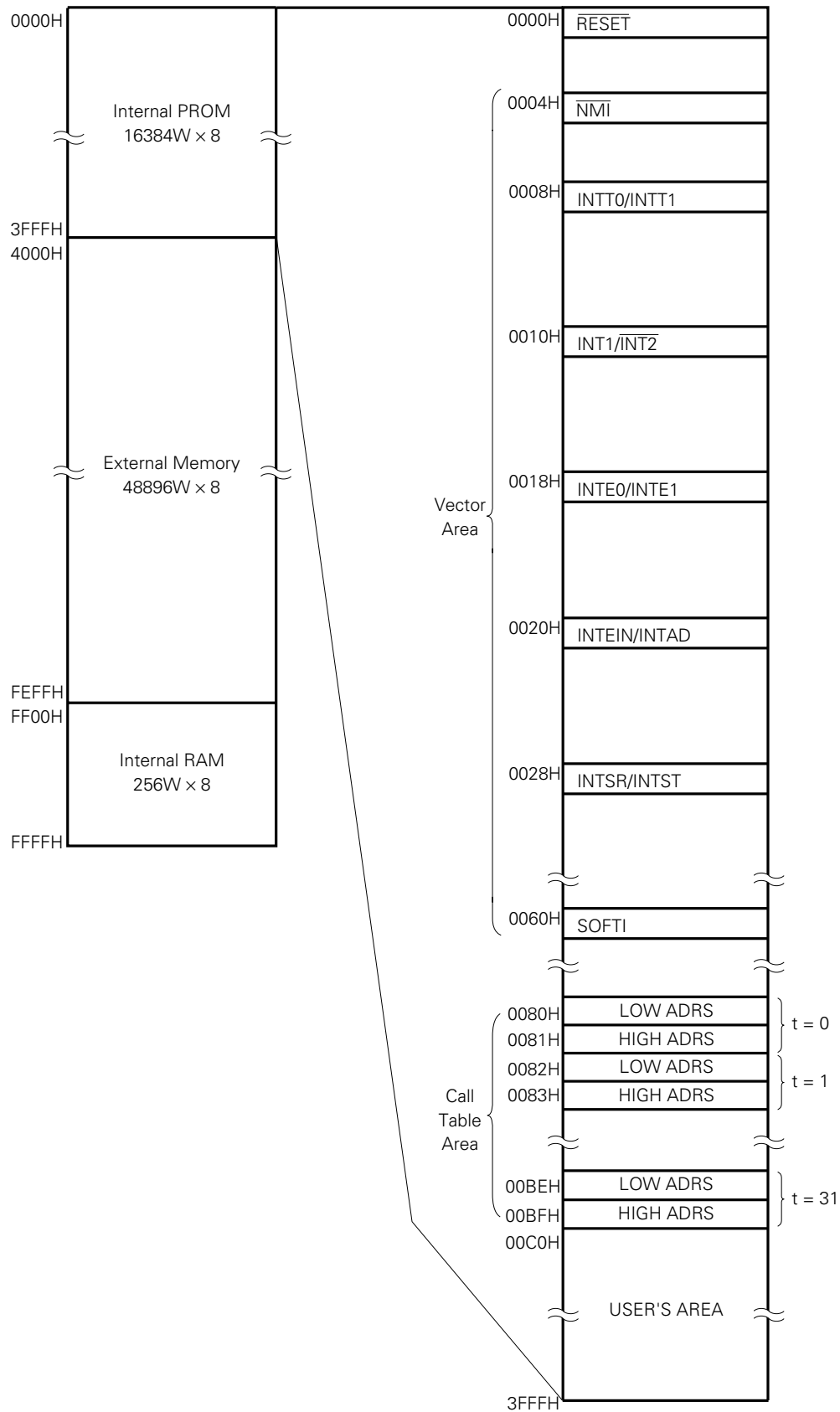
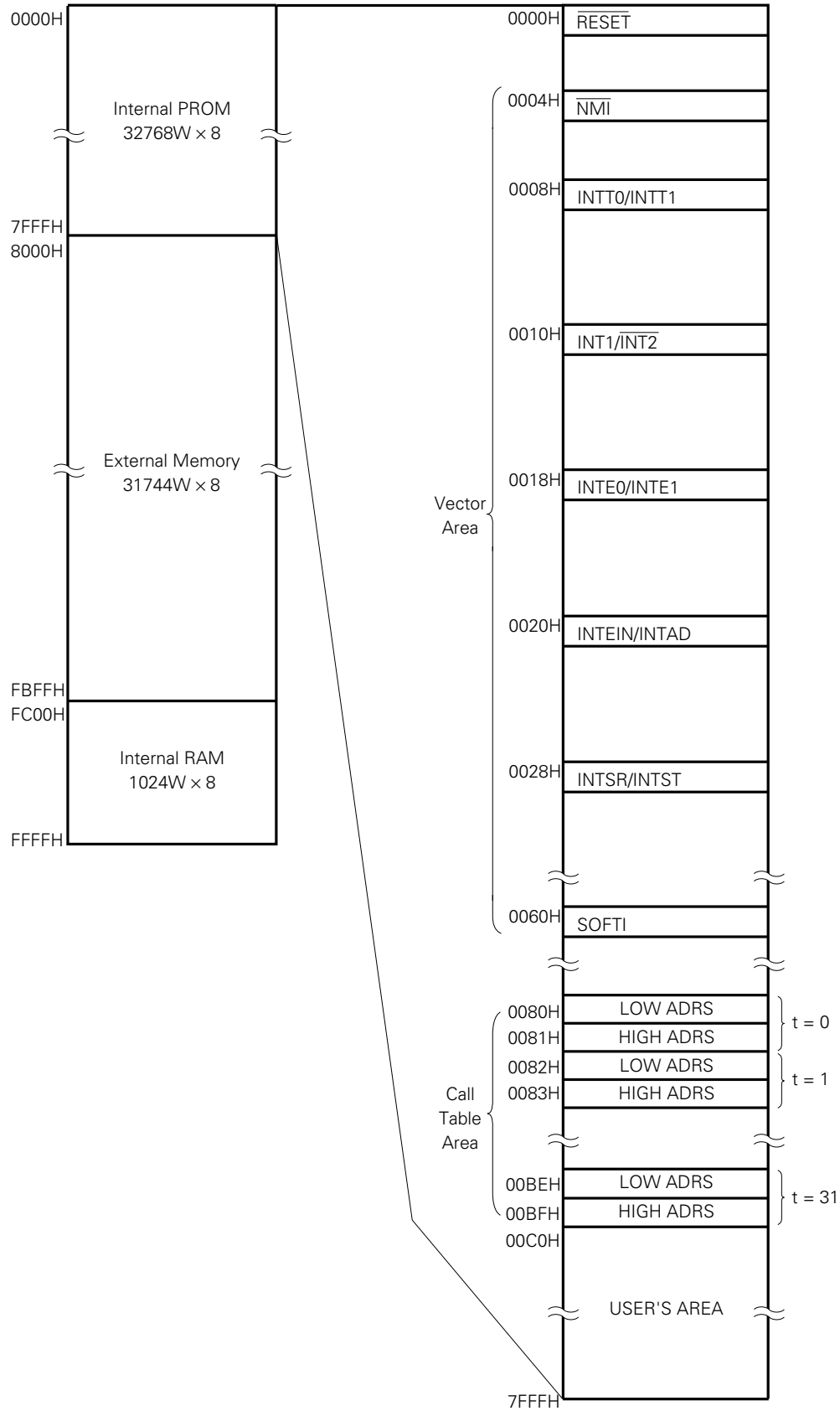


Figure 2-4. Memory Map (μPD78C18 Mode)



3. MEMORY EXTENSION

The μPD78CP18(A) allows external memory extension by means of the MEMORY MAPPING register (MM) or the MODE0 and MODE1 pins. Also, the internal PROM and internal RAM access areas can be specified by means of bits MM7, MM6 and MM5 of the MEMORY MAPPING register.

3.1 MODE PINS

The μPD78CP18(A) can be switched between programming mode and normal operation mode according to the specification of the MODE0 and MODE1 pins.

Table 3-1 shows the modes set by the MODE pins.

Table 3-1. Modes Set By MODE Pins

MODE1	MODE2	Operating Mode
L	L	Setting prohibited
L	H	Programming mode ^{Note}
H	L	Normal operation mode
H	H	Setting prohibited

Note See 4. "PROM PROGRAMMING".

When MODE0 and MODE1 are driven high, a $4 \text{ [k}\Omega\text{]} \leq R \leq 0.4 \text{ t}_{\text{CYC}} \text{ [k}\Omega\text{]}$ pull-up resistor should be used (t_{CYC}: ns units).

3.2 MEMORY MAPPING REGISTER (MM)

The MEMORY MAPPING register is an 8-bit register which performs the following controls:

- Port/extension mode specification for PD7 to PD0 and PF7 to PF0
- Enabling/disabling of internal RAM accesses
- Specification of internal PROM and RAM access areas

The configuration of the MEMORY MAPPING register is shown in Figure 3-1.

(1) Bits MM2 to MM0

These bits control the PD7 to PD0 port/extension mode specification, input/output specification, and the PF7 to PF0 address output specification.

As shown in Figure 3-1, there is a choice of four capacities for the connectable external memory:

- 256 bytes
- 4 Kbytes
- 16 Kbytes
- 32 K/48 K/56 K/60 Kbytes (set by bits MM7 to MM5)

Ports of PF7 to PF0 not used as address outputs can be used as general-purpose ports.

When $\overline{\text{RESET}}$ signal is input or in the hardware STOP mode, these bits are reset to (0) and PD7 to PD0 are set to input port mode (high-impedance).

(2) MM3 bit (RAE)

This bit enables (RAE = 1) and disables (RAE = 0) internal RAM access. This bit should be set to "0" during standby operation and when externally connected RAM, not internal RAM, is used.

In normal operation this bit retains its value when $\overline{\text{RESET}}$ signal is input. However, the RAE bit is undefined after a power-on reset, and must therefore be initialized by an instruction.

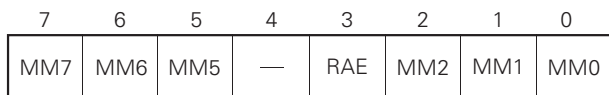
(3) Bits MM7 to MM5

These bits specify the access area of the internal PROM.

When $\overline{\text{STOP}}$ or $\overline{\text{RESET}}$ signal is input, these bits are reset, selecting the 32-Kbyte mode (μ PD78C18 mode).

These bits are only valid in the μ PD78CG14, 78CP14, 78CP18, 78CP14(A), and 78CP18(A); if data is written to these bits in the μ PD78C11A(A), 78C12A(A), 78C14(A), or 78C18(A), it will be ignored. Therefore, a program developed on the μ PD78CP18(A) can be directly ported to mask ROM.

Figure 3-1. MEMORY MAPPING Register Format



0	0	0	Port mode	Singlechip	PD7 to PD0 = Input port PF7 to PF0 = Port mode
0	0	1			PD7 to PD0 = Output port PF7 to PF0 = Port mode
0	1	0	Extension mode	256 bytes	PD7 to PD0 = Extension mode PF7 to PF0 = Port mode
1	0	0		4 Kbytes	PD7 to PD0 = } Extension mode PF3 to PF0 = } PF7 to PF4 = Port mode
1	1	0		16 Kbytes	PD7 to PD0 = } Extension mode PF5 to PF0 = } PF7 & PF6 = Port mode
1	1	1		32 K/48 K/ 56K/60K ^{Note} bytes	PD7 to PD0 = } Extension mode PF7 to PF0 = }

Note Depends on MM7 to MM5 bit-setting

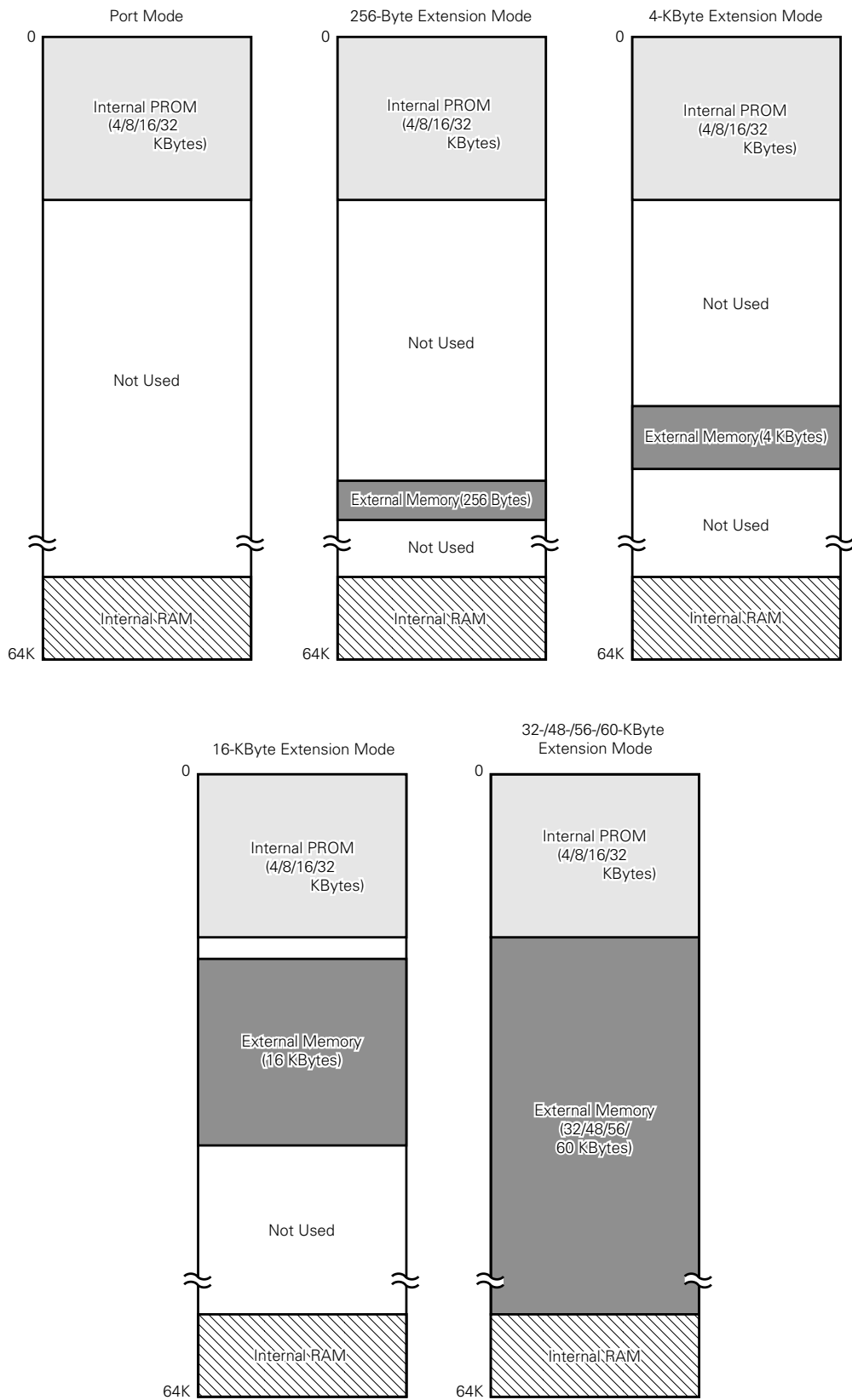
Internal RAM Access

0	Disable
1	Enable

Internal PROM/RAM Access Areas

MM7	MM6	MM5	Internal PROM Access Area	Internal RAM Access Area
0	0	0	0000H to 7FFFH (32 Kbytes: μPD78C18 mode)	FC00H to FFFFH (1 Kbyte)
0	0	1	0000H to 3FFFH (16 Kbytes: μPD78C14 mode)	FF00H to FFFFH (256 bytes)
0	1	1	0000H to 1FFFH (8 Kbytes: μPD78C12A mode)	FF00H to FFFFH (256 bytes)
1	0	1	0000H to 0FFFH (4 Kbytes: μPD78C11A mode)	FF00H to FFFFH (256 bytes)
Other than above			Setting Prohibited	

Figure 3-2. External Extension Modes Set by MEMORY MAPPING Register



Caution The internal PROM and internal RAM access areas are determined by MM7 to MM5.

4. PROM PROGRAMMING

The μ PD78CP18(A) incorporates 32768×8 -bit PROM as a program memory. The pins shown in Table 4-1 are used for write/verify operations on this PROM.

μ PD78CP18(A) program timing is compatible with the μ PD27C256A.

Please read the following in conjunction with documentation of the μ PD27C256A.

Table 4-1. Pins Used in PROM Programming

Pin Name	Function
$\overline{\text{RESET}}$	Low-level input (at write/verify and read)
MODE0	High-level input (at write/verify and read)
MODE1	Low-level input (at write/verify and read)
V_{PP}^{Note}	High-voltage input (at write/verify), high-level input (at read)
$\overline{\text{CE}}^{\text{Note}}$	Chip enable input
$\overline{\text{OE}}^{\text{Note}}$	Output enable input
A14 to A0 ^{Note}	Address input
O7 to O0 ^{Note}	Data input (at write), data output (at verify, read)
V_{DD}^{Note}	Supply voltage input

Note These pins correspond to the μ PD27C256A.

Caution The μ PD78CP18(A) one-time PROM version is not equipped with an erasure window, and therefore ultraviolet erasure cannot be performed on it.

4.1 PROM PROGRAMMING OPERATING MODES

The PROM programming operating mode is set as shown in Table 4-2. Pins not used for programming should be handled as shown in Table 4-3.

Table 4-2. PROM Programming Modes

Operating Mode	\overline{CE} ^{Note}	\overline{OE} ^{Note}	V_{PP} ^{Note}	V_{DD} ^{Note}	\overline{RESET}	MODE0	MODE1
Program	L	H	+12.5 V	+6 V	L	H	L
Program verify	H	L					
Program inhibit	H	H					
Read	L	L	+5 V	+5 V			
Output disable	L	H					
Standby	H	L/H					

Note These pins correspond to the μPD27C256A.

Caution When +12.5 V is applied to V_{PP} and +6 V is applied to V_{DD} , setting both \overline{CE} and \overline{OE} to “L” is prohibited.

Table 4-3. Recommended Connection of Unused Pins (in PROM Programming Mode)

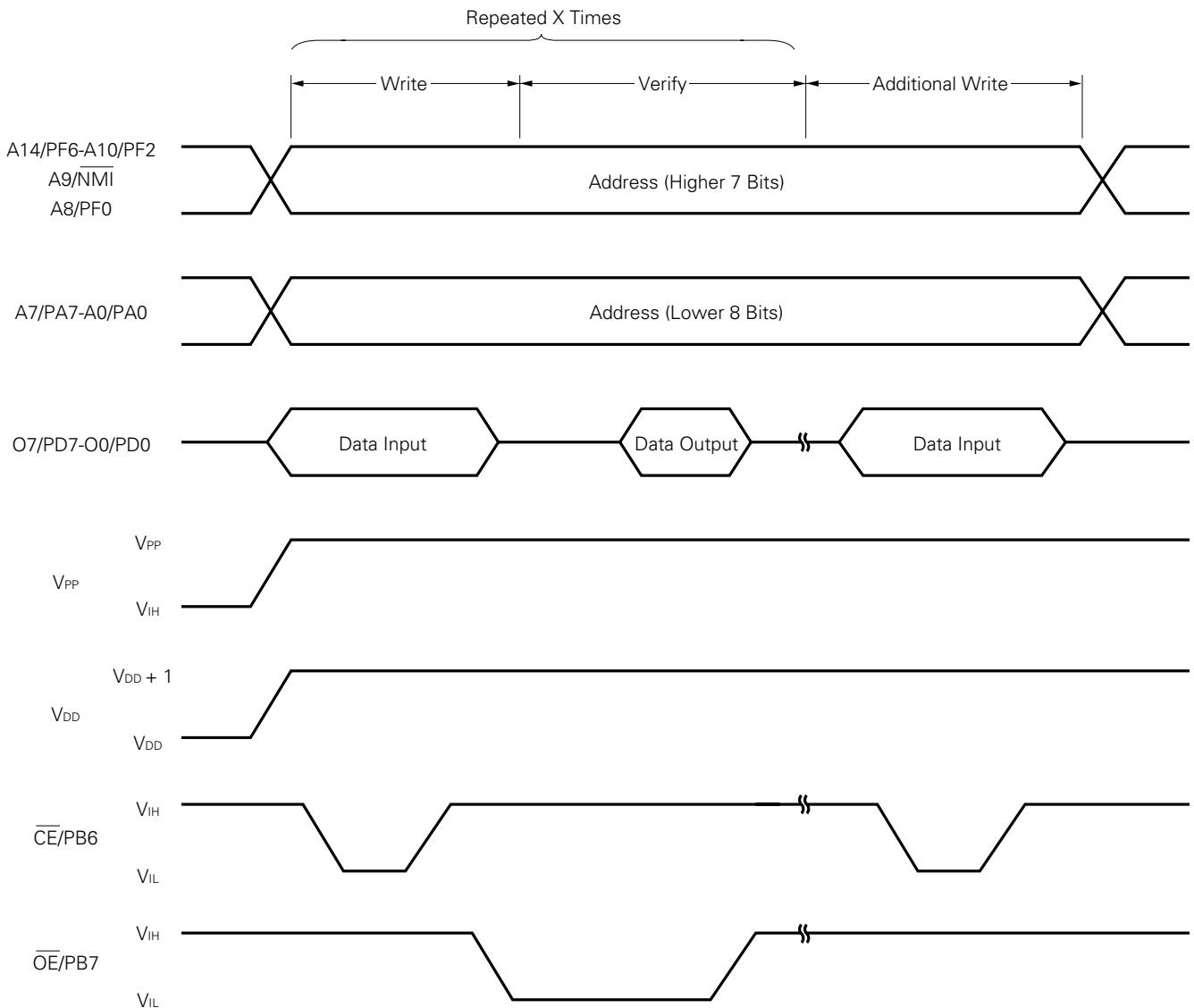
Pin	Recommended Connection
INT1	Connect to V_{SS} .
X1	
AN0 to AN7	
V_{AREF}	
AV_{DD}	
AV_{SS}	
Pins other than the above	Connect to V_{SS} via individual resistor.
X2	Leave open.

4.2 PROM WRITING PROCEDURE

The PROM writing procedure is as shown below, allowing high-speed writing.

- (1) Connect unused pins to V_{ss} via a pull-down resistor, and supply +6 V to V_{DD} and +12.5 V to V_{PP}.
- (2) Provide the initial address.
- (3) Provide the write data.
- (4) Provide a 1-ms program pulse (active low) to the \overline{CE} pin.
- (5) Verify mode. If written, go to (7); if not written, repeat (3) to (5). If the write operation has failed 25 times, go to (6).
- (6) Halt write operation due to defective device.
- (7) Provide write data and program pulse of X times x 3 ms (X; repeated times from (3) to (5)) (additional write).
- (8) Increment the address.
- (9) Repeat (3) to (8) until the final address.

Figure 4-1. PROM Write/Verify Timing



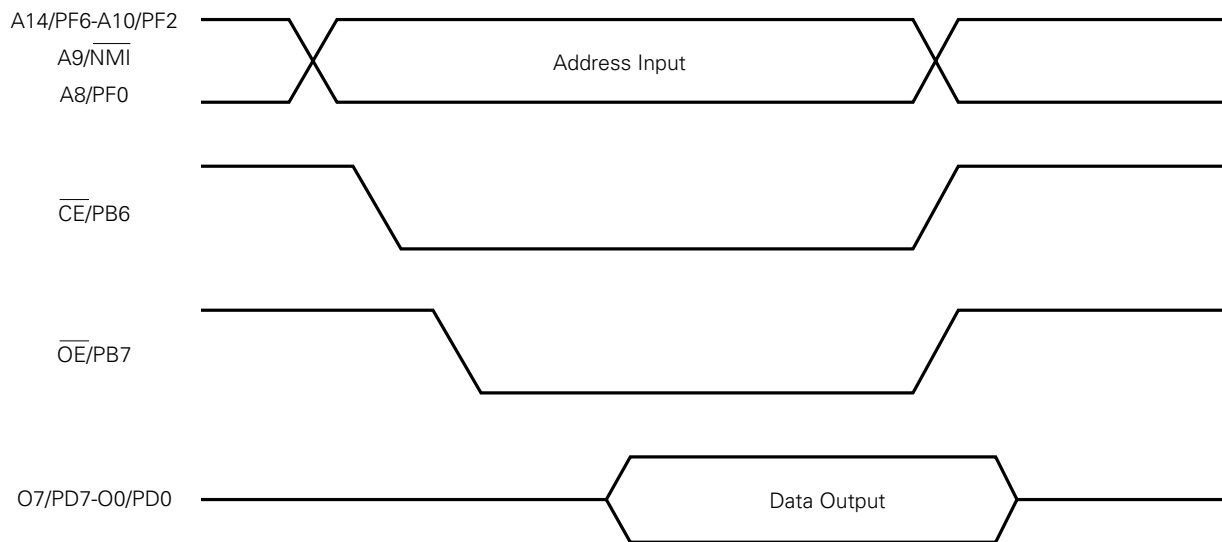
4.3 PROM READING PROCEDURE

PROM contents can be read onto the external data bus (O7 to O0) using the following procedure.

- (1) Connect unused pins to V_{SS} via a pull-down resistor.
- (2) Supply +5 V to the V_{DD} and V_{PP} pins.
- (3) Input address of data to be read to pins A14 to A0.
- (4) Read mode
- (5) Output data to pins O7 to O0.

Timing for steps (2) to (5) above is shown in Figure 4-2.

Figure 4-2. PROM Read Timing



5. SCREENING OF ONE-TIME PROM VERSIONS

Because of their construction, one-time PROM versions cannot be fully tested by NEC before shipment. After the necessary data has been written, it is recommended that screening be implemented in which PROM verification is performed after high-temperature storage under the following conditions.

Storage Temperature	Storage Time
125 °C	24 hours

- ★ NEC provides writing, marking, screening, and inspection services for single-chip microcomputers labeled QTOP microcomputers. For details, consult NEC.

6. ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C)

PARAMETER	SYMBOL	TEST CONDITIONS	RATINGS	UNIT
Power supply voltage	V _{DD}		-0.5 to +7.0	V
	AV _{DD}		AV _{SS} to V _{DD} + 0.5	V
	AV _{SS}		-0.5 to +0.5	V
	V _{PP}		-0.5 to +13.5	V
Input voltage	V _I	Other than $\overline{\text{NMI/A9}}$ pin	-0.5 to V _{DD} + 0.5	V
		$\overline{\text{NMI/A9}}$ pin	-0.5 to +13.5	V
Output voltage	V _O		-0.5 to V _{DD} + 0.5	V
Output current low	I _{OL}	All output pins	4.0	mA
		Total of all output pins	100	mA
Output current high	I _{OH}	All output pins	-2.0	mA
		Total of all output pins	-50	mA
A/D converter reference input voltage	V _{AREF}		-0.5 to AV _{DD} + 0.3	V
Ambient operating temperature	T _A		-40 to +85	°C
Storage temperature	T _{stg}		-65 to +150	°C

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Caution If the absolute maximum rating of even one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. The absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product with these rated values never exceeded. ★

OSCILLATOR CHARACTERISTICS ($T_A = -40$ to $+85$ °C, $V_{DD} = AV_{DD} = +5.0$ V \pm 10 %, $V_{SS} = AV_{SS} = 0$ V, $V_{DD} - 0.8$ V \leq $AV_{DD} \leq V_{DD}$, 3.4 V \leq $V_{AREF} \leq AV_{DD}$)

RESONATOR	RECOMMENDED CIRCUIT	PARAMETER	TEST CONDITIONS	MIN.	MAX.	UNIT
Ceramic or crystal resonator		Oscillator frequency (f_{xx})	A/D converter not used	4	15	MHz
			A/D converter used	5.8	15	
External clock		X1 input frequency (f_x)	A/D converter not used	4	15	MHz
			A/D converter used	5.8	15	
		X1 rise time, fall time (t_r, t_f)		0	20	ns
X1 input high-, low-level width ($t_{\phi H}, t_{\phi L}$)		20	250	ns		

- Cautions**
1. Place the oscillator as close as possible to the X1 and X2 pins.
 2. Ensure that no other signal lines pass through the shaded area.

CAPACITANCE (T_A = 25 °C, V_{DD} = V_{SS} = 0 V)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input capacitance	C _i	f _c = 1 MHz Unmeasured pins returned to 0 V			10	pF
Output capacitance	C _o				20	pF
Input-output capacitance	C _{io}				20	pF

DC CHARACTERISTICS (T_A = -40 to +85 °C, V_{DD} = AV_{DD} = +5.0 V ± 10 %, V_{SS} = AV_{SS} = 0 V)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Input voltage low	V _{IL1}	All except $\overline{\text{RESET}}$, $\overline{\text{STOP}}$, $\overline{\text{NMI}}$, $\overline{\text{SCK}}$, INT1, TI, AN4 to AN7	0		0.8	V	
	V _{IL2}	$\overline{\text{RESET}}$, $\overline{\text{STOP}}$, $\overline{\text{NMI}}$, $\overline{\text{SCK}}$, INT1, TI, AN4 to AN7	0		0.2V _{DD}	V	
Input voltage high	V _{IH1}	All except $\overline{\text{RESET}}$, $\overline{\text{STOP}}$, $\overline{\text{NMI}}$, $\overline{\text{SCK}}$, INT1, TI, AN4 to AN7, X1, X2	2.2		V _{DD}	V	
	V _{IH2}	$\overline{\text{RESET}}$, $\overline{\text{STOP}}$, $\overline{\text{NMI}}$, $\overline{\text{SCK}}$, INT1, TI, AN4 to AN7, X1, X2	0.8 V _{DD}		V _{DD}	V	
Output voltage low	V _{OL}	I _{oL} = 2.0 mA			0.45	V	
Output voltage high	V _{OH}	I _{oH} = -1.0 mA	V _{DD} - 1.0			V	
		I _{oH} = -100 μA	V _{DD} - 0.5			V	
Input current	I _i	INT1 ^{Note1} , TI(PC3) ^{Note2} ; 0 V ≤ V _i ≤ V _{DD}			±200	μA	
Input leakage current	I _{LI}	All except INT1, TI (PC3), AN7 to AN0; 0 V ≤ V _i ≤ V _{DD}			±10	μA	
		AN7 to AN0; 0 V ≤ V _i ≤ V _{DD}			±1	μA	
Output leakage current	I _{LO}	0 V ≤ V _o ≤ V _{DD}			±10	μA	
AV _{DD} power supply current	A _{IDD1}	Operating mode f _{xx} = 15 MHz		0.5	1.3	mA	
	A _{IDD2}	STOP mode		10	20	μA	
V _{DD} power supply current	I _{DD1}	Operating mode f _{xx} = 15 MHz		16	35	mA	
	I _{DD2}	HALT mode f _{xx} = 15 MHz		7	13	mA	
Data retention voltage	V _{DDDR}	Hardware/software STOP mode	2.5			V	
Data retention current	I _{DDDR}	Hardware/software ^{Note3}	V _{DDDR} = 2.5 V		1	15	μA
		STOP mode	V _{DDDR} = 5 V ± 10 %		10	50	μA

★

- Notes**
1. If self-bias should be generated by ZCM register.
 2. If the control mode is set by MCC register, and self-bias should be generated by ZCM register.
 3. If self-bias is not generated.

AC CHARACTERISTICS (T_A = -40 to +85 °C, V_{DD} = AV_{DD} = +5.0 V ± 10 %, V_{SS} = AV_{SS} = 0 V)
READ/WRITE OPERATION:

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	MAX.	UNIT
X1 input cycle time	t _{CYC}		66	167	ns
Address setup time (to ALE↓)	t _{AL}	f _{XX} = 15 MHz, C _L = 150 pF	30		ns
Address hold time (from ALE↓)	t _{LA}		35		ns
\overline{RD} ↓ delay time from address	t _{AR}		100		ns
Address float time from \overline{RD} ↓	t _{AFR}	C _L = 150 pF		20	ns
Data input time from address	t _{AD}	f _{XX} = 15 MHz, C _L = 150 pF		250	ns
Data input time from ALE↓	t _{LDR}			135	ns
Data input time from \overline{RD} ↓	t _{RD}			120	ns
\overline{RD} ↓ delay time from ALE↓	t _{LR}		15		ns
Data hold time (from \overline{RD} ↑)	t _{RDH}	C _L = 150 pF	0		ns
ALE↑ delay time from \overline{RD} ↑	t _{RL}	f _{XX} = 15 MHz, C _L = 150 pF	80		ns
\overline{RD} low-level width	t _{RR}	In data read f _{XX} = 15 MHz, C _L = 150 pF	215		ns
		In OP code fetch f _{XX} = 15 MHz, C _L = 150 pF	415		ns
ALE high-level width	t _{LL}	f _{XX} = 15 MHz, C _L = 150 pF	90		ns
\overline{WR} ↓ delay time from address	t _{AW}	f _{XX} = 15 MHz, C _L = 150 pF	100		ns
Data output time from ALE↓	t _{LDW}			197	ns
Data output time from \overline{WR} ↓	t _{WD}	C _L = 150 pF		140	ns
\overline{WR} ↓ delay time from ALE↓	t _{LW}	f _{XX} = 15 MHz, C _L = 150 pF	15		ns
Data setup time (to \overline{WR} ↑)	t _{DW}		127		ns
Data hold time (from \overline{WR} ↑)	t _{WDH}		60		ns
ALE↑ delay time from \overline{WR} ↑	t _{WL}		80		ns
\overline{WR} low-level width	t _{WW}		215		ns

ZERO-CROSS CHARACTERISTICS :

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	MAX.	UNIT
Zero-cross detection input	V _{ZX}	AC coupling 60-Hz sine wave	1	1.8	V _{AC P-P}
Zero-cross accuracy	A _{ZX}			±135	mV
Zero-cross detection input frequency	f _{ZX}		0.05	1	kHz

SERIAL OPERATION :

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	MAX.	UNIT
$\overline{\text{SCK}}$ cycle time	t_{CYK}	$\overline{\text{SCK}}$ input	Note1	800		ns
			Note2	400		ns
		$\overline{\text{SCK}}$ output		1.6		μs
$\overline{\text{SCK}}$ low-level width	t_{KLL}	$\overline{\text{SCK}}$ input	Note1	335		ns
			Note2	160		ns
		$\overline{\text{SCK}}$ output		700		ns
$\overline{\text{SCK}}$ high-level width	t_{KHH}	$\overline{\text{SCK}}$ input	Note1	335		ns
			Note2	160		ns
		$\overline{\text{SCK}}$ output		700		ns
RxD setup time (to $\overline{\text{SCK}}\uparrow$)	t_{RXK}	Note1	80		ns	
RxD hold time (from $\overline{\text{SCK}}\uparrow$)	t_{KRX}	Note1	80		ns	
TxD delay time from $\overline{\text{SCK}}\downarrow$	t_{KTX}	Note1		210	ns	

- Notes**
1. If clock rate is $\times 1$ in asynchronous mode, synchronous mode, or I/O interface mode.
 2. If clock rate is $\times 16$ or $\times 64$ in asynchronous mode.

Remark The numeric values in the table are those when $f_{\text{XX}} = 15 \text{ MHz}$, $\text{CL} = 100 \text{ pF}$.

OTHER OPERATION :

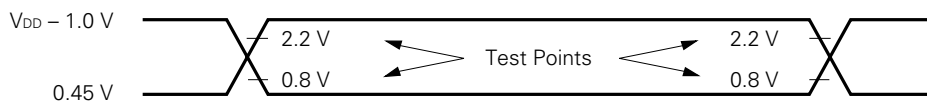
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	MAX.	UNIT
Tl high-, low-level width	$t_{\text{TIH}}, t_{\text{TIL}}$		6		tcyc
Cl high-, low-level width	$t_{\text{CI1H}}, t_{\text{CI1L}}$	• Event counter mode	6		tcyc
		• Frequency test mode			
Cl high-, low-level width	$t_{\text{CI2H}}, t_{\text{CI2L}}$	• Pulse width test mode	48		tcyc
		• ECNT latch and clear input			
		• INTEIN set input			
$\overline{\text{NMI}}$ high-, low-level width	$t_{\text{NIH}}, t_{\text{NIL}}$		10		μs
INT1 high-, low-level width	$t_{\text{I1H}}, t_{\text{I1L}}$		36		tcyc
$\overline{\text{INT2}}$ high-, low-level width	$t_{\text{I2H}}, t_{\text{I2L}}$		36		tcyc
AN4 to AN7, low-level width	$t_{\text{ANH}}, t_{\text{ANL}}$		36		tcyc
$\overline{\text{RESET}}$ high-, low-level width	$t_{\text{RSH}}, t_{\text{RSL}}$		10		μs

A/D CONVERTER CHARACTERISTICS ($T_A = -40$ to $+85$ °C, $V_{DD} = +5.0$ V \pm 10 %, $V_{SS} = AV_{SS} = 0$ V, $V_{DD} - 0.5$ V \leq $AV_{DD} \leq V_{DD}$, 3.4 V \leq $V_{AREF} \leq AV_{DD}$)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Resolution			8			Bits
Absolute accuracy ^{Note}		3.4 V \leq $V_{AREF} \leq AV_{DD}$, 66 ns \leq $t_{CYC} \leq 167$ ns			± 0.8 %	FSR
		4.0 V \leq $V_{AREF} \leq AV_{DD}$, 66 ns \leq $t_{CYC} \leq 167$ ns			± 0.6 %	FSR
		$T_A = -10$ to $+70$ °C, 4.0 V \leq $V_{AREF} \leq AV_{DD}$, 66 ns \leq $t_{CYC} \leq 167$ ns			± 0.4 %	FSR
Conversion time	t_{CONV}	66 ns \leq $t_{CYC} \leq 110$ ns	576			t_{CYC}
		110 ns \leq $t_{CYC} \leq 167$ ns	432			t_{CYC}
Sampling time	t_{SAMP}	66 ns \leq $t_{CYC} \leq 110$ ns	96			t_{CYC}
		110 ns \leq $t_{CYC} \leq 167$ ns	72			t_{CYC}
Analog input voltage	V_{IAN}		-0.3		$V_{AREF} + 0.3$	V
★ Analog input impedance	R_{AN}			50		MΩ
Reference voltage	V_{AREF}		3.4		AV_{DD}	V
V_{AREF} current	I_{AREF1}	Operating mode		1.5	3.0	mA
	I_{AREF2}	STOP mode		0.7	1.5	mA
AV_{DD} power supply current	AI_{DD1}	Operating mode $f_{XX} = 15$ MHz		0.5	1.3	mA
	AI_{DD2}	STOP mode		10	20	μA

Note Quantization error ($\pm 1/2$ LSB) is not included.

AC Timing Test Point



tcyc-Dependent AC Characteristics Expression

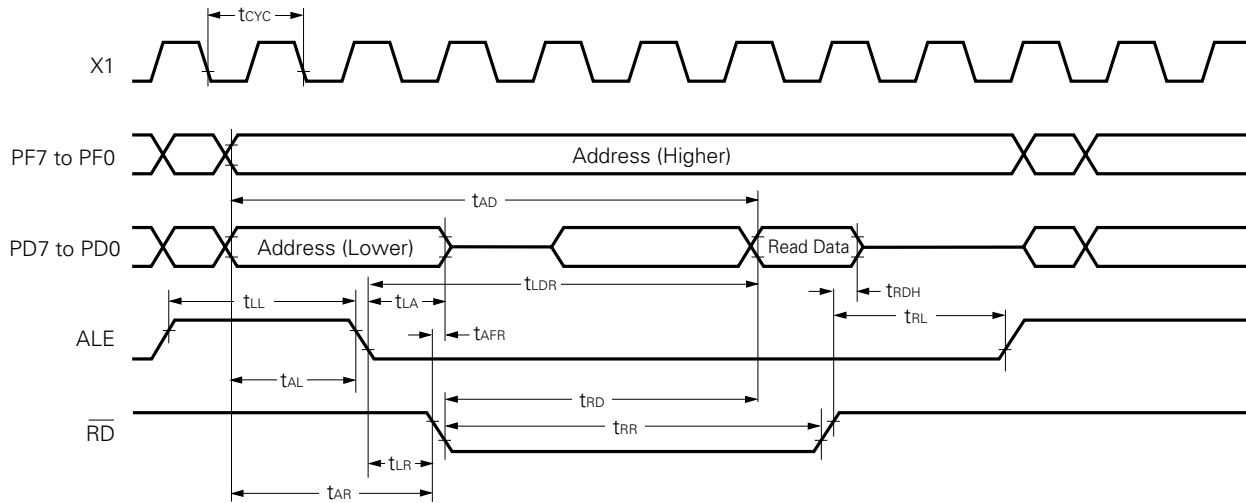
PARAMETER	EXPRESSION	MIN./MAX.	UNIT
t _{AL}	2T - 100	MIN.	ns
t _{LA}	T - 30	MIN.	ns
t _{AR}	3T - 100	MIN.	ns
t _{AD}	7T - 220	MAX.	ns
t _{LDR}	5T - 200	MAX.	ns
t _{RD}	4T - 150	MAX.	ns
t _{LR}	T - 50	MIN.	ns
t _{RL}	2T - 50	MIN.	ns
t _{RR}	4T - 50 (In data read)	MIN.	ns
	7T - 50 (In OP code fetch)		
t _{LL}	2T - 40	MIN.	ns
t _{AW}	3T - 100	MIN.	ns
t _{LDW}	T + 130	MAX.	ns
t _{LW}	T - 50	MIN.	ns
t _{DW}	4T - 140	MIN.	ns
t _{WDH}	2T - 70	MIN.	ns
t _{WL}	2T - 50	MIN.	ns
t _{WW}	4T - 50	MIN.	ns
tcyc	12T (SCK input) ^{Note1}	MIN.	ns
	6T (SCK input) ^{Note2}		
	24T (SCK output)		
t _{KKL}	5T + 5 (SCK input) ^{Note1}	MIN.	ns
	2.5T + 5 (SCK input) ^{Note2}		
	12T - 100 (SCK output)		
t _{KKH}	5T + 5 (SCK input) ^{Note1}	MIN.	ns
	2.5T + 5 (SCK input) ^{Note2}		
	12T - 100 (SCK output)		

- Notes**
1. If clock rate is ×1, in asynchronous mode, synchronous mode, or I/O interface mode.
 2. If clock rate is ×16, ×64 in asynchronous mode.

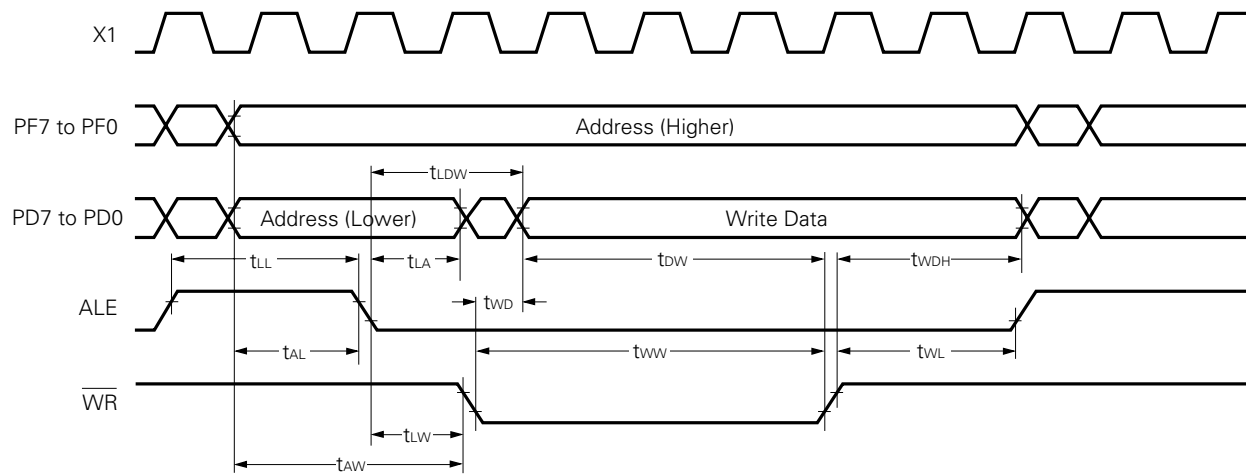
- Remarks**
1. T = tcyc = 1/fxx
 2. Other items which are not listed in this table are not dependent on oscillator frequency (fxx).

Timing Waveforms

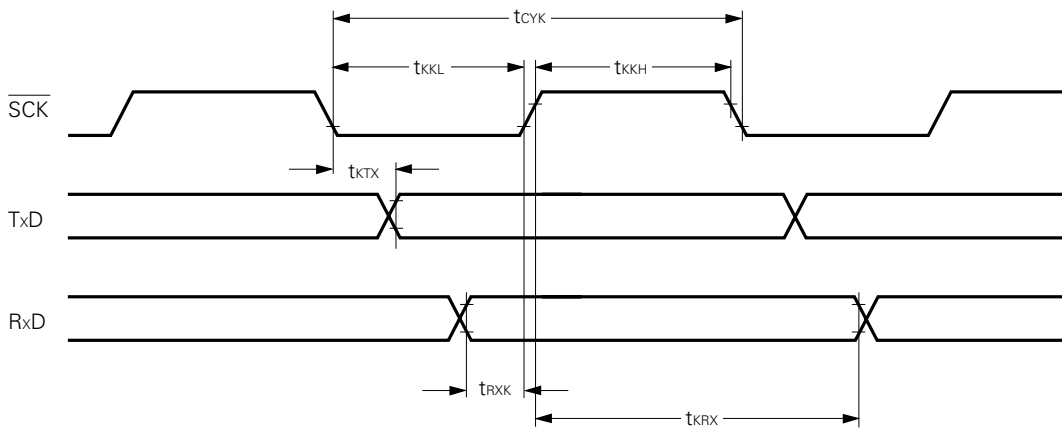
Read Operation



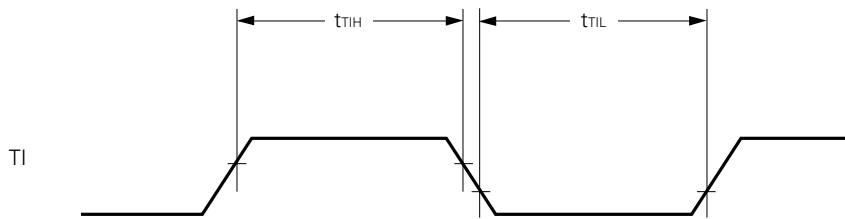
Write Operation



Serial Operation

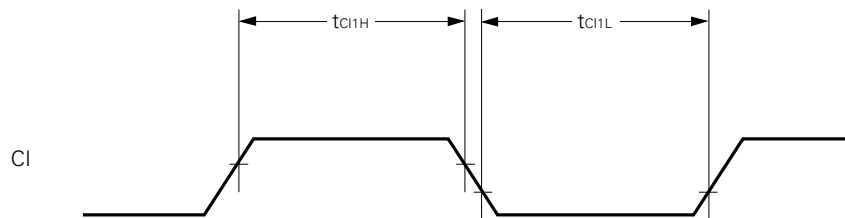


Timer Input Timing

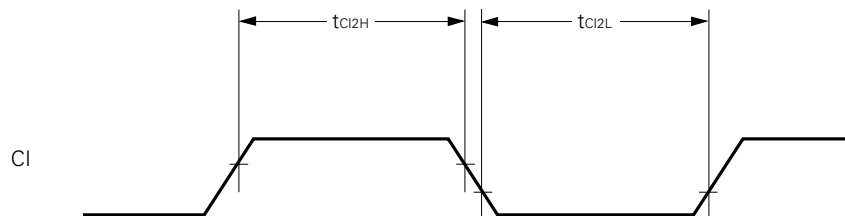


Timer/Event Counter Input Timing

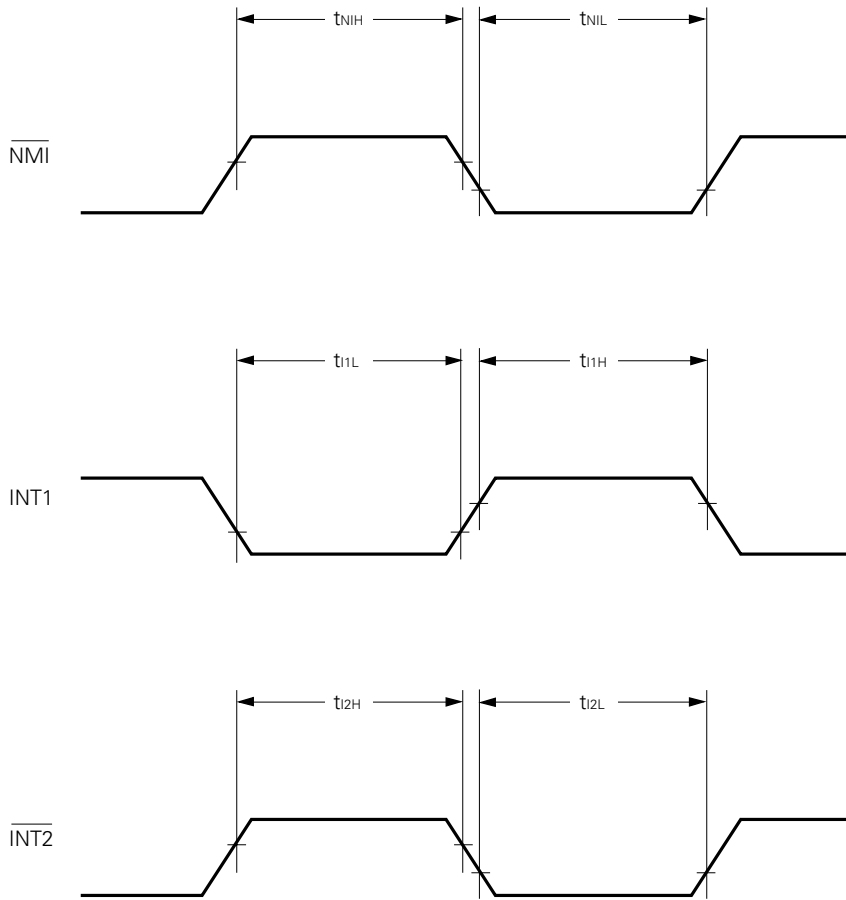
Event Counter Mode



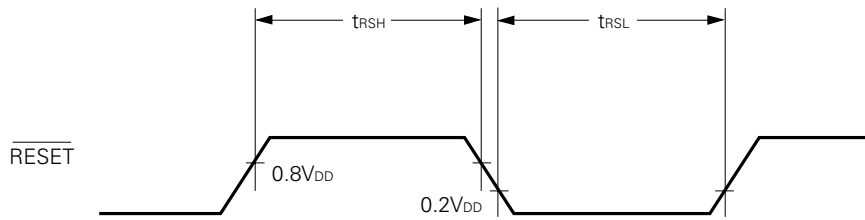
Pulse Width Test Mode



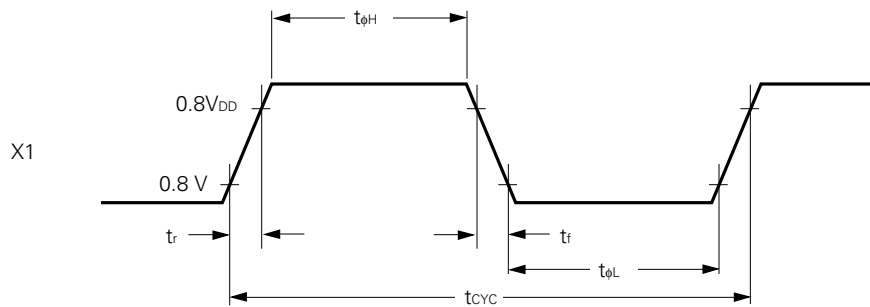
Interrupt Input Timing



Reset Input Timing



External Clock Timing



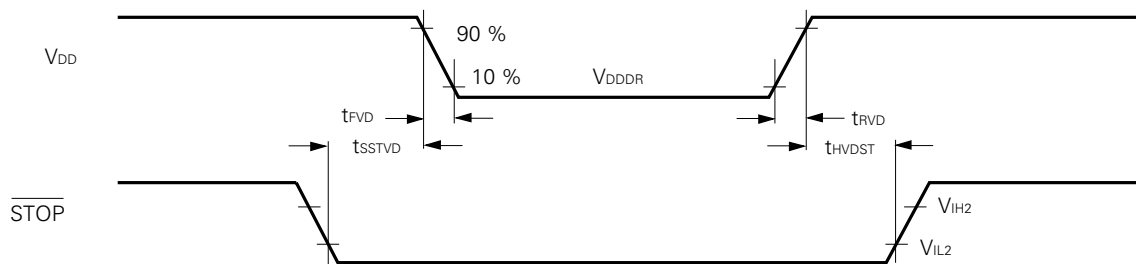
DATA MEMORY STOP MODE LOW POWER SUPPLY VOLTAGE DATA RETENTION CHARACTERISTICS (T_A = -40 to +85 °C)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Data retention power supply voltage	V _{DDDR}		2.5		5.5	V
Data retention power supply current	I _{DDDR}	V _{DDDR} = 2.5 V		1	15	μA
		V _{DDDR} = 5 V ± 10 %		10	50	μA
V _{DD} rise/fall time	t _{RV} D, t _{FV} D		200			μs
STOP setup time (to V _{DD})	t _{SSTV} D		12T + 0.5 Note			μs
STOP hold time (from V _{DD})	t _{HVDST}		12T + 0.5 Note			μs

★

Note T = t_{cy}c = 1/f_{xx}

Data Retention Timing



DC PROGRAMMING CHARACTERISTICS (T_A = 25 ± 5 °C, MODE1 = V_{IL}, MODE0 = V_{IH}, V_{SS} = 0 V)

PARAMETER	SYMBOL	SYMBOL ^{Note}	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input voltage high	V _{IH}	V _{IH}		2.4		V _{DDP} + 0.3	V
Input voltage low	V _{IL}	V _{IL}		-0.3		0.8	V
Input leakage current	I _{LIP}	I _{LI}	0 ≤ V _I ≤ V _{DDP} ; except INT1, T1 (PC3)			±10	μA
Output voltage high	V _{OH}	V _{OH}	I _{OH} = -1.0 mA	V _{DD} - 1.0			V
Output voltage low	V _{OL}	V _{OL}	I _{OL} = 2.0 mA			0.45	V
Output leakage current	I _{LO}	—	0 ≤ V _O ≤ V _{DDP} , \overline{OE} = V _{IH}			±10	μA
V _{DDP} supply voltage	V _{DDP}	V _{DD}	EPROM programming mode	5.75	6.0	6.25	V
			EPROM read mode	4.5	5.0	5.5	V
V _{PP} supply voltage	V _{PP}	V _{PP}	EPROM programming mode	12.2	12.5	12.8	V
			EPROM read mode	V _{PP} = V _{DDP}			V
V _{DDP} supply current	I _{DD}	I _{DD}	EPROM programming mode		5	50	mA
			EPROM read mode CE = V _{IL} , V _I = V _{IH}		5	50	mA
V _{PP} supply current	I _{PP}	I _{PP}	EPROM programming mode CE = V _{IL} , \overline{OE} = V _{IH}		5	30	mA
			EPROM read mode		1	100	μA

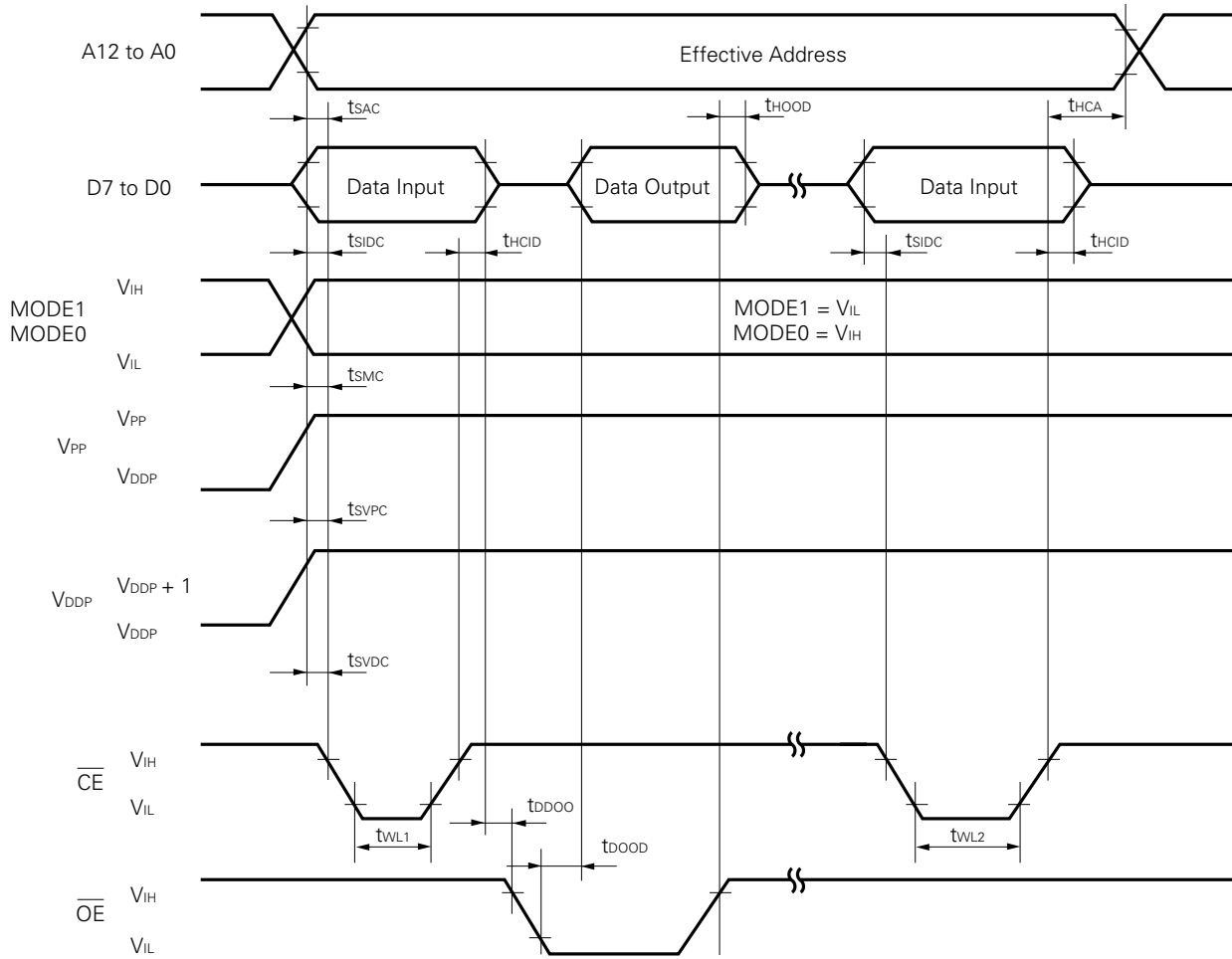
Note Corresponding μPD27C256A symbol

AC PROGRAMMING CHARACTERISTICS (T_A = 25 ± 5 °C, MODE1 = V_{IL}, MODE0 = V_{IH}, V_{SS} = 0 V)

PARAMETER	SYMBOL	SYMBOL ^{Note1}	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Address setup time (to $\overline{CE}\downarrow$)	t _{SAC}	t _{AS}		2			μs
$\overline{OE}\downarrow$ delay time from data	t _{DDO0}	t _{OES}		2			μs
Input data setup time (to $\overline{CE}\downarrow$)	t _{SIDC}	t _{DS}		2			μs
Address hold time (from $\overline{CE}\uparrow$)	t _{HCA}	t _{AH}		2			μs
Input data hold time (from $\overline{CE}\uparrow$)	t _{HCID}	t _{DH}		2			μs
Output data hold time (from $\overline{OE}\uparrow$)	t _{HOOD}	t _{DF}		0		130	ns
V _{PP} setup time (to $\overline{CE}\downarrow$)	t _{SVPC}	t _{VPS}		2			μs
V _{DDP} setup time (to $\overline{CE}\downarrow$)	t _{SVDC}	t _{VDS}		2			μs
Initial program pulse width	t _{WL1}	t _{PW}		0.95	1.0	1.05	ms
Additional program pulse width	t _{WL2}	t _{OPW}		2.85		78.75	ms
EPROM programming/read mode setup time (to $\overline{CE}\downarrow$) ^{Note2}	t _{SMC}	—		2			μs
Data output time from address	t _{DAOD}	t _{ACC}	$\overline{OE} = V_{IL}$			1	μs
Data output time from $\overline{CE}\downarrow$	t _{DCOD}	t _{CCE}				1	μs
Data output time from $\overline{OE}\downarrow$	t _{DOOD}	t _{OEE}				1	μs
Data hold time (from $\overline{OE}\uparrow$)	t _{HCOD}	t _{DF}		0		130	ns
Data hold time (from address)	t _{HAOD}	t _{OH}	$\overline{OE} = V_{IL}$	0			ns

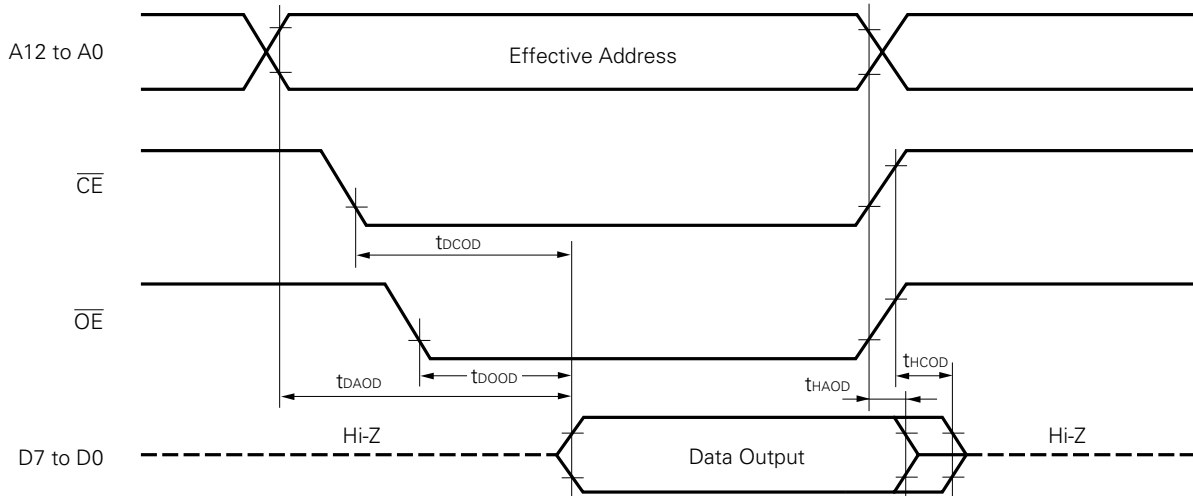
- Notes**
1. Corresponding μPD27C256A symbol
 2. Indicates state in which MODE1 = V_{IL} and MODE0 = V_{IH}.

PROM Programming Mode Timing



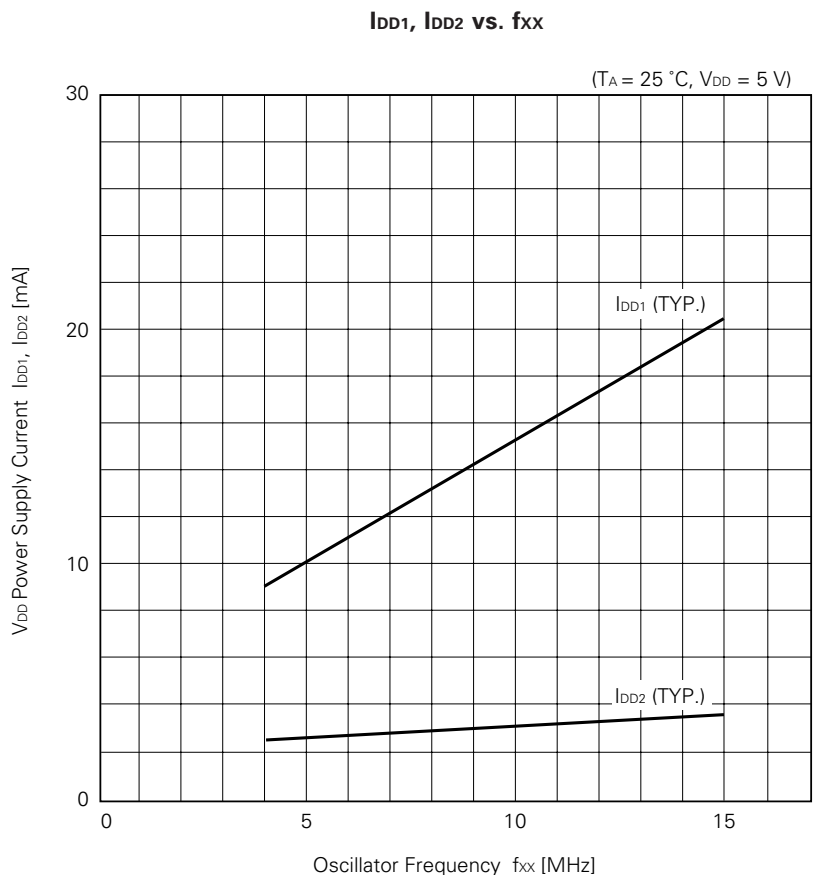
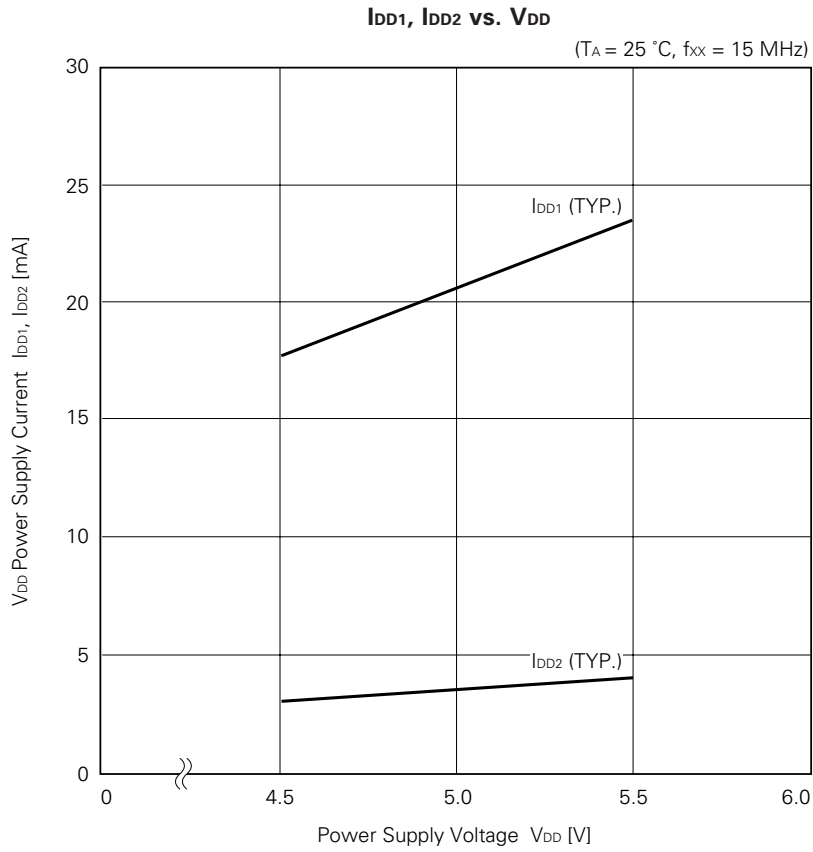
- Cautions**
1. Ensure that V_{DDP} is applied before V_{PP} , and cut after V_{PP} .
 2. Ensure that V_{PP} does not exceed +13 V including overshoot.

PROM Read Mode Timing

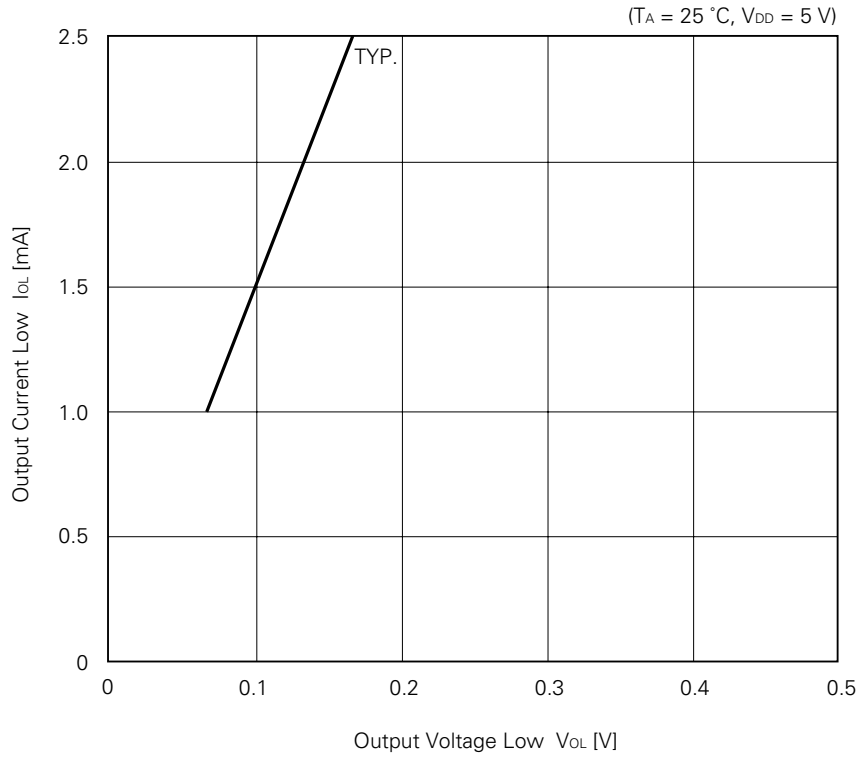


- Cautions**
1. If you wish to read within the t_{DAOD} range, the \overline{OE} input delay time from the fall of \overline{CE} should be a maximum of $t_{DAOD} - t_{DOOD}$.
 2. t_{HCOD} is the time from the point at which \overline{OE} or \overline{CE} (whichever is first) reaches V_{IH} .

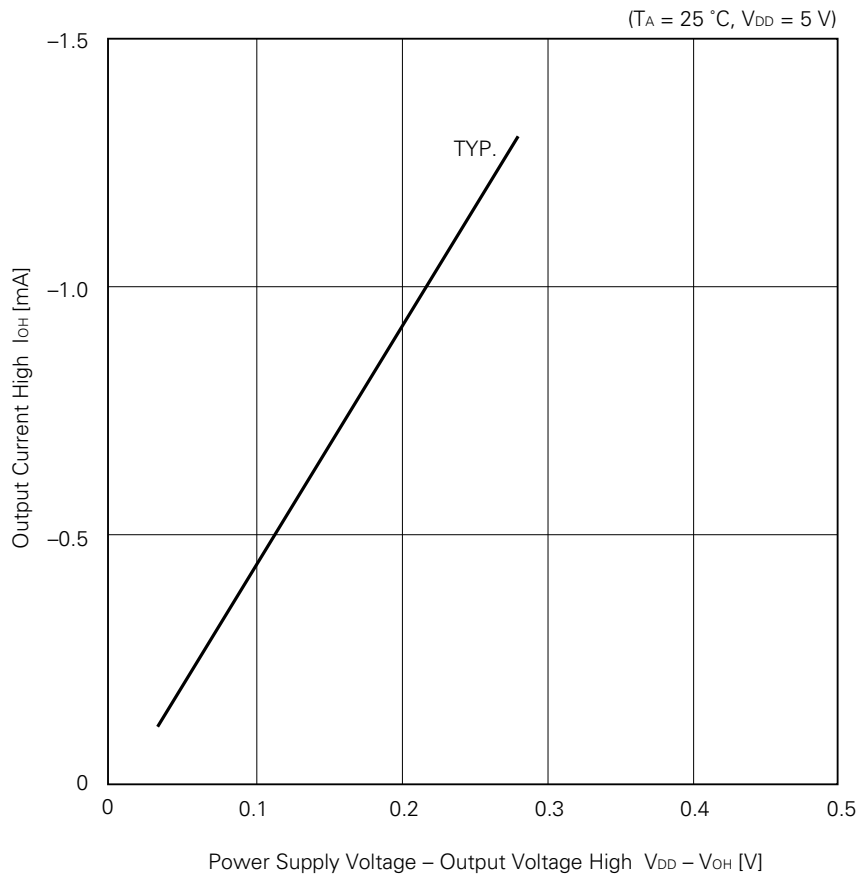
7. CHARACTERISTIC CURVES (REFERENCE VALUE)



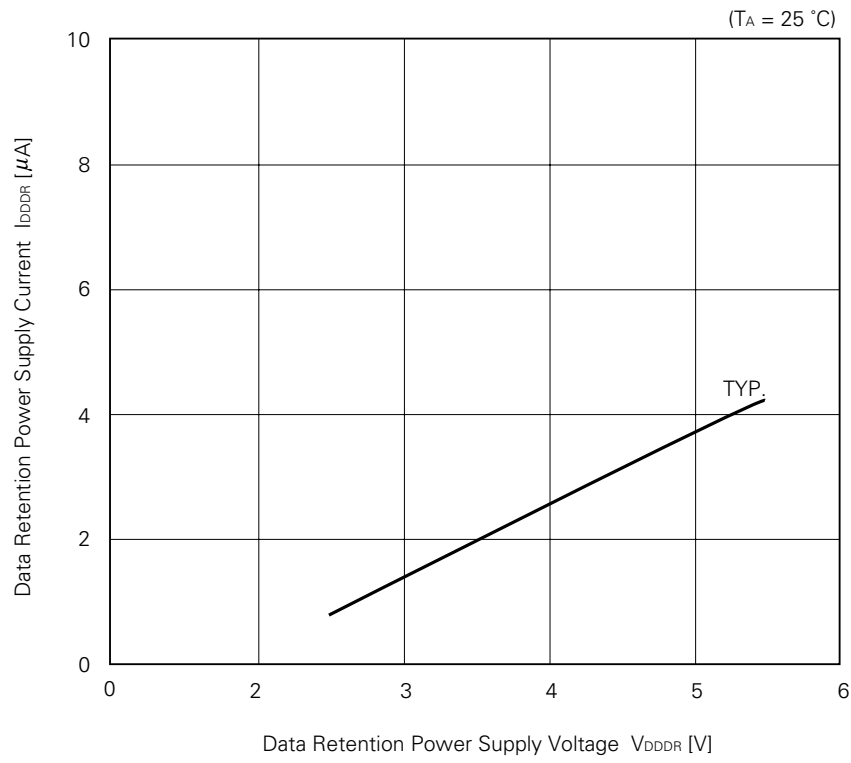
I_{OL} vs. V_{OL}



I_{OH} vs. V_{OH}

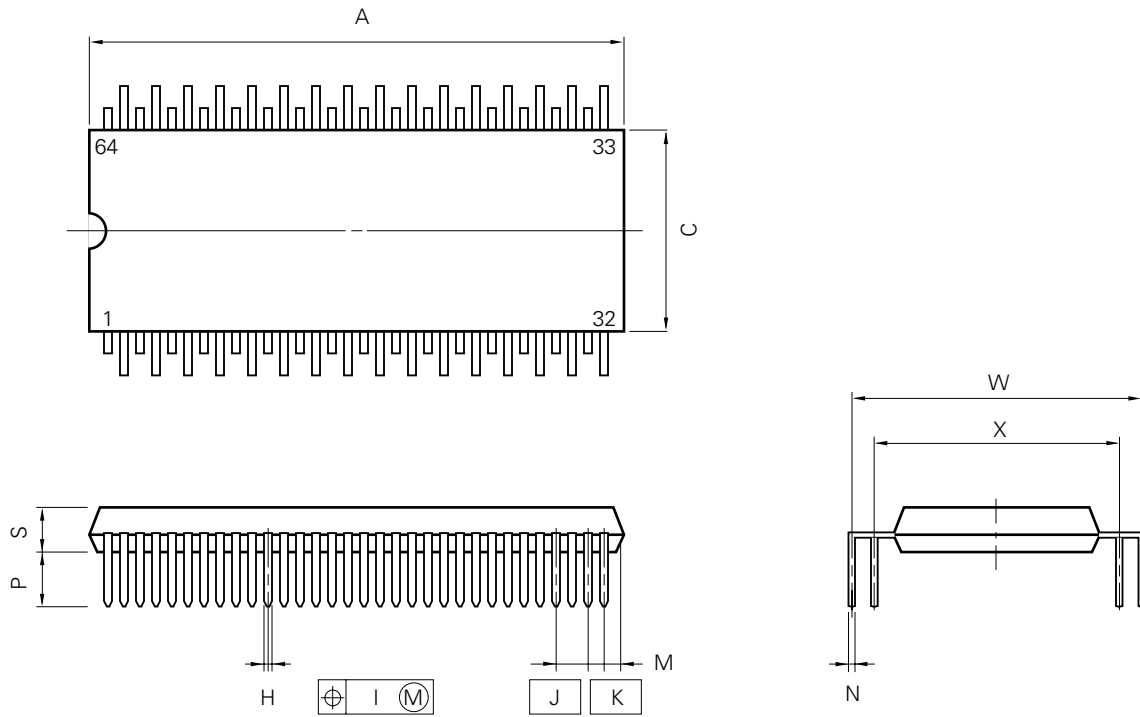


I_{DDDR} vs. V_{DDDR}



8. PACKAGE DRAWINGS

64 PIN PLASTIC QUIP



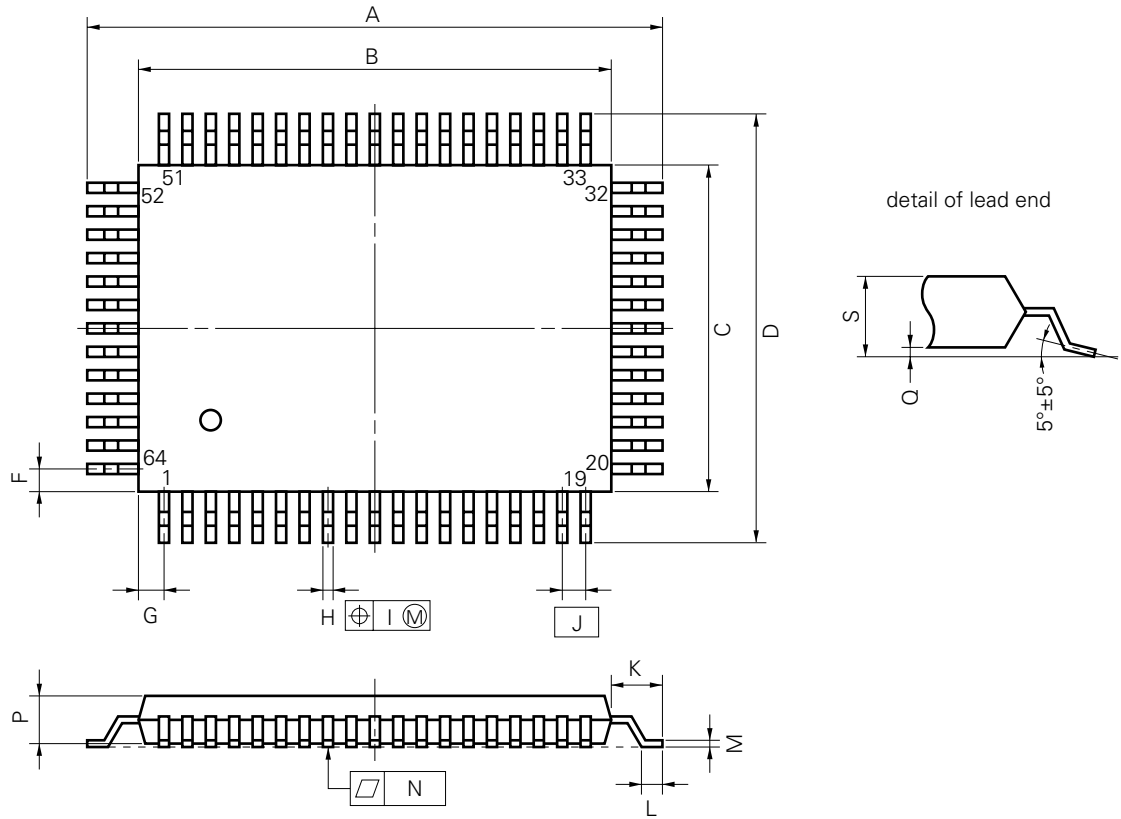
NOTE

Each lead centerline is located within 0.25 mm (0.010 inch) of its true position (T.P.) at maximum material condition.

P64GQ-100-36

ITEM	MILLIMETERS	INCHES
A	41.5 ^{+0.3} _{-0.2}	1.634 ^{+0.012} _{-0.008}
C	16.5	0.650
H	0.50 ^{±0.10}	0.020 ^{+0.004} _{-0.005}
I	0.25	0.010
J	2.54 (T.P.)	0.100 (T.P.)
K	1.27 (T.P.)	0.050 (T.P.)
M	1.1 ^{+0.25} _{-0.15}	0.043 ^{+0.011} _{-0.006}
N	0.25 ^{+0.10} _{-0.05}	0.010 ^{+0.004} _{-0.003}
P	4.0 ^{±0.3}	0.157 ^{+0.013} _{-0.012}
S	3.6 ^{±0.1}	0.142 ^{+0.004} _{-0.005}
W	24.13 ^{±1.05}	0.950 ^{±0.042}
X	19.05 ^{±1.05}	0.750 ^{±0.042}

64 PIN PLASTIC QFP (14x20)



NOTE

Each lead centerline is located within 0.20 mm (0.008 inch) of its true position (T.P.) at maximum material condition.

P64GF-100-3B8,3BE,3BR-1

ITEM	MILLIMETERS	INCHES
A	23.6±0.4	0.929±0.016
B	20.0±0.2	0.795 ^{+0.009} _{-0.008}
C	14.0±0.2	0.551 ^{+0.009} _{-0.008}
D	17.6±0.4	0.693±0.016
F	1.0	0.039
G	1.0	0.039
H	0.40±0.10	0.016 ^{+0.004} _{-0.005}
I	0.20	0.008
J	1.0 (T.P.)	0.039 (T.P.)
K	1.8±0.2	0.071 ^{+0.008} _{-0.009}
L	0.8±0.2	0.031 ^{+0.009} _{-0.008}
M	0.15 ^{+0.10} _{-0.05}	0.006 ^{+0.004} _{-0.003}
N	0.12	0.005
P	2.7	0.106
Q	0.1±0.1	0.004±0.004
S	3.0 MAX.	0.119 MAX.

★ 9. RECOMMENDED SOLDERING CONDITIONS

The μPD78CP18(A) should be soldered and mounted under the following recommended conditions.

For details of recommended soldering conditions, refer to the information document "Semiconductor Device Mounting Technology Manual (IEI-1207)".

For soldering methods and conditions other than those recommended below, contact an NEC representative.

Table 9-1. Surface Mount Type Soldering Conditions

μPD78CP18GF(A)-3BE: 64-Pin Plastic QFP (14 × 20 mm)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235 °C, Duration: 30 sec. max. (at 210 °C or higher), Count: Twice or less <Attention> (1) Perform the second reflow at the time the device temperature is lowered to the room temperature from the heating by the first reflow. (2) Do not wash the soldered portion with the flux following the first reflow.	IR35-00-2
VPS	Package peak temperature: 215 °C, Duration: 40 sec. max. (at 200 °C or higher), Count: Twice or less <Attention> (1) Perform the second reflow at the time the device temperature is lowered to the room temperature from the heating by the first reflow. (2) Do not wash the soldered portion with the flux following the first reflow.	VP15-00-2
Wave soldering	Solder bath temperature: 260 °C max., Duration: 10 sec. max., Count: Once Preheating temperature: 120 °C max. (package surface temperature)	WS60-00-1
Partial heating	Pin temperature: 300 °C max., Duration: 3 sec. max. (per device side row of pins)	—

Caution Use of more than one soldering method should be avoided (except in the case of pin part heating).

Table 9-2. Through-Hole Type Soldering Conditions

μPD78CP18GQ(A)-36: 64-Pin Plastic QUIP

Soldering Method	Soldering Conditions
Wave soldering (pin part only)	Solder bath temperature: 260 °C max., Duration: 10 sec. max.
Partial heating	Pin temperature: 300 °C max., Duration: 3 sec. max. (per pin)

Caution Wave soldering is used on the pin only, and care must be taken to prevent solder from coming into direct contact with the body.

10. DIFFERENCES BETWEEN THE μPD78CP18(A) AND μPD78C18(A)

Item \ Part Number	μPD78CP18(A)	μPD78C18(A)
Internal ROM	32 K × 8 bits (PROM)	32 K × 8 bits (mask ROM)
Internal RAM	1 K × 8 bits	1 K × 8 bits
Pin connection	PB7/ \overline{OE}	PB7
	PB6/ \overline{CE}	PB6
	STOP/ V_{PP}	STOP
	$\overline{NMI}/A9$	\overline{NMI}
	PA7/A7 to PA0/A0	PA7 to PA0
	PF6/A14 to PF2/A10	PF6 to PF2
	PF0/A8	PF0
	PD7/O7 to PD0/O0	PD7 to PD0
Mode set by MODE pins (when MODE0 is set to 1, and MODE1 to 0)	PROM programming mode	<ul style="list-style-type: none"> Operates as the μPD78C17(A) (ROM-less mode) External memory 16 K extension mode
MODE0 pin input/output function	Input only ^{Note}	Input/output
Internal memory access area setting by MM register	Yes	No
Port A to Port C	Pull-up resistors not incorporated	Pull-up resistor incorporation selectable bit-wise by mask option

Note An emulation control signal is not output even if the MODE0 pin is pulled high.

★ APPENDIX DEVELOPMENT TOOLS

The following development tools are available to develop a system which uses the μPD78CP18(A).

Language Processor

87AD series relocatable assembler (RA87)	This is a program which converts a program written in mnemonic to an object code for which microcomputer execution is possible. Moreover, it contains a function to automatically create a symbol/table, and optimize branch instructions.			
	Host Machine	OS	Supply Medium	Ordering Code (Product Name)
	PC-9800 series	MS-DOS™ [Ver. 2.11 to Ver. 5.00A ^{Note}]	3.5-inch 2HD	μS5A13RA87
			5-inch 2HD	μS5A10RA87
	IBM PC/AT™	PC DOS™ (Ver. 3.1)	3.5-inch 2HC	μS7B13RA87
			5-inch 2HC	μS7B10RA87

PROM Write Tools

Hardware	PG-1500	With a provided board and an optional programmer adapter connected, this PROM programmer can manipulate from a stand-alone or host machine to perform programming on a single-chip microcomputer which incorporates PROM. It is also capable of programming a typical PROM ranging from 256 K to 4 M bits.		
	PA-78CP14GF/ GQ	PROM programmer adapter for the μPD78CP18(A). Used by connecting to the PG-1500.		
	PA-78CP14GF	For the μPD78CP18GF(A)-3BE		
	PA-78CP14GQ	For the μPD78CP18GQ(A)-36		
Software	PG-1500 controller	Connects the PG-1500 to a host machine by using serial and parallel interface, to control the PG-1500 on a host machine.		
		Host Machine	OS	Supply Medium
	PC-9800 series	MS-DOS [Ver. 2.11 to Ver. 5.00A ^{Note}]	3.5-inch 2HD	μS5A13PG1500
			5-inch 2HD	μS5A10PG1500
IBM PC/AT	PC DOS (Ver. 3.1)	5-inch 2HC	μS7B10PG1500	

Note Versions 5.00 and 5.00A have a task swap function, but this function cannot be used with this software.

Remark The operations of the assembler and the PG-1500 controller are guaranteed only on the above host machines and operating systems.

Debugging Tools

An in-circuit emulator (IE-78C11-M) is available as a program debugging tool for the μPD78CP18(A). The following table shows its system configuration.

Hardware	IE-78C11-M	The IE-78C11-M is an in-circuit emulator which works with the 87AD series. It can be connected to a host machine to perform efficient debugging.			
Software	IE-78C11-M control program (IE controller)	Connects the IE-78C11-M to host machine by using the RS-233C, to control the IE-78C11-M on host machine.			
		Host Machine	OS	Supply Medium	Ordering Code (Product Name)
		PC-9800 series	MS-DOS [Ver. 2.11 to Ver. 3.30D]	3.5-inch 2HD	μS5A13IE78C11
				5-inch 2HD	μS5A10IE78C11
IBM PC/AT	PC DOS (Ver. 3.1)	5-inch 2HC	μS7B10IE78C11		

Remark The operations of the IE controller are guaranteed only on the above host machines and operating systems.

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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Special: Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)

Specific: Aircrafts, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems or medical equipment for life support, etc.

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