NEC

MOS INTEGRATED CIRCUIT

μPD780031AY, 780032AY, 780033AY, 780034AY

8-BIT SINGLE-CHIP MICROCONTROLLERS

DESCRIPTION

The μPD780031AY, 780032AY, 780033AY, and 780034AY are members of the μPD780034AY Subseries of the 78K/0 Series. This is a μPD780034A Subseries product with an added multimaster-supporting I^2C bus interface, and is suitable for AV equipment applications.

A flash memory version, the μPD78F0034AY, that can operate in the same power supply voltage range as the mask ROM version, and various development tools, are available.

Detailed function descriptions are provided in the following user's manuals. Be sure to read them before designing.

μPD780024A, 780034A, 780024AY, 780034AY Subseries User's Manual:	**U14046E**
78K/0 Series User's Manual Instructions:	**U12326E**

FEATURES

- Internal ROM and RAM

Item / Part Number	Program Memory (Internal ROM)	Data Memory (Internal High-Speed RAM)	Package
μPD780031AY	8 Kbytes	512 bytes	• 64-pin plastic shrink DIP (750 mils) • 64-pin plastic QFP (14 × 14 mm) • 64-pin plastic LQFP (12 × 12 mm)
μPD780032AY	16 Kbytes		
μPD780033AY	24 Kbytes	1024 bytes	
μPD780034AY	32 Kbytes		

- External memory expansion space: 64 Kbytes
- Minimum instruction execution time: 0.24 μs (@ f_X = 8.38-MHz operation)
- I/O ports: 51 (5-V-tolerant N-ch open-drain: 4)
- 10-bit resolution A/D converter: 8 channels (AV_{DD} = 1.8 to 5.5 V)
- Serial interface: 3 channels (multimaster-supporting I^2C bus mode, UART mode, 3-wire serial I/O mode)
- Timer: 5 channels
- Power supply voltage: V_{DD} = 1.8 to 5.5 V

APPLICATIONS

Telephones, home electric appliances, pagers, AV equipment, car audios, office automation equipment, etc.

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ORDERING INFORMATION

Part Number	Package
μPD780031AYCW-×××	64-pin plastic shrink DIP (750 mils)
μPD780031AYGC-×××-AB8	64-pin plastic QFP (14 × 14 mm)
μPD780031AYGK-×××-8A8	64-pin plastic LQFP (12 × 12 mm)
μPD780032AYCW-×××	64-pin plastic shrink DIP (750 mils)
μPD780032AYGC-×××-AB8	64-pin plastic QFP (14 × 14 mm)
μPD780032AYGK-×××-8A8	64-pin plastic LQFP (12 × 12 mm)
μPD780033AYCW-×××	64-pin plastic shrink DIP (750 mils)
μPD780033AYGC-×××-AB8	64-pin plastic QFP (14 × 14 mm)
μPD780033AYGK-×××-8A8	64-pin plastic LQFP (12 × 12 mm)
μPD780034AYCW-×××	64-pin plastic shrink DIP (750 mils)
μPD780034AYGC-×××-AB8	64-pin plastic QFP (14 × 14 mm)
μPD780034AYGK-×××-8A8	64-pin plastic LQFP (12 × 12 mm)

Remark ××× indicates ROM code suffix.

78K/0 SERIES LINEUP

The products in the 78K/0 Series are listed below. The names enclosed in boxes are subseries names.

Products in mass production

Products under development

Y subseries products are compatible with I²C bus.

78K/0 Series

Control

Pins	Subseries	Y subseries	Description
100-pin	μPD78075B		EMI-noise reduced version of the μPD78078
100-pin	μPD78078	μPD78078Y	μPD78054 with added timer and enhanced external interface
100-pin	μPD78070A	μPD78070AY	ROM-less version of the μPD78078
100-pin		μPD780018AY	μPD78078Y with enhanced serial I/O and limited functions
80-pin	μPD780058	μPD780058Y	μPD78054 with enhanced serial I/O
80-pin	μPD78058F	μPD78058FY	EMI-noise reduced version of the μPD78054
80-pin	μPD78054	μPD78054Y	μPD78018F with added UART and D/A converter and enhanced I/O
80-pin	μPD780065		μPD780024A with increased RAM capacity
64-pin	μPD780078	μPD780078Y	A μPD780034A with added timer and enhanced serial I/O
64-pin	μPD780034A	μPD780034AY	μPD780024A with enhanced A/D converter
64-pin	μPD780024A	μPD780024AY	μPD78018F with enhanced serial I/O
64-pin	μPD78014H		EMI-noise reduced version of the μPD78018F
64-pin	μPD78018F	μPD78018FY	Basic subseries for control
42/44-pin	μPD78083		On-chip UART, capable of operating at low voltage (1.8 V)

Inverter control

Pins	Subseries	Y subseries	Description
64-pin	μPD780988		On-chip inverter control circuit and UART. EMI-noise reduced.

FIP™ drive

Pins	Subseries	Y subseries	Description
100-pin	μPD780208		μPD78044F with enhanced I/O and FIP C/D. Display output total: 53
100-pin	μPD780228		μPD78044H with enhanced I/O and FIP C/D. Display output total: 48
80-pin	μPD780232		For panel control. On-chip FIP C/D. Display output total: 53
80-pin	μPD78044H		μPD78044F with added N-ch open drain I/O. Display output total: 34
80-pin	μPD78044F		Basic subseries for driving FIP. Display output total: 34

LCD drive

Pins	Subseries	Y subseries	Description
100-pin	μPD780308	μPD780308Y	μPD78064 with enhanced SIO, and increased ROM, RAM capacity.
100-pin	μPD78064B		EMI-noise reduced version of the μPD78064
100-pin	μPD78064	μPD78064Y	Basic subseries for driving LCDs, on-chip UART

Call ID supported

Pins	Subseries	Y subseries	Description
80-pin	μPD780841		On-chip Call ID and simple DTMF. EMI-noise reduced.

Bus interface supported

Pins	Subseries	Y subseries	Description
100-pin	μPD780948		On-chip D-CAN controller
80-pin	μPD78098B		μPD78054 with IEBus™ controller added. EMI-noise reduced.
80-pin		μPD780701Y	On-chip D-CAN/IEBus controller
80-pin		μPD780833Y	On-chip controller compliant with J1850 (Class 2)

Meter control

Pins	Subseries	Y subseries	Description
100-pin	μPD780958		For industrial meter control
80-pin	μPD780955		Ultra low-power consumption. On-chip UART.
80-pin	μPD780973		On-chip automobile meter controller/driver
80-pin	μPD780824		For automobile meter. On-chip D-CAN controller.

The major functional differences among the Y subseries are shown below.

Subseries Name \ Function		ROM Capacity	Configuration of Serial Interface	I/O	V_{DD} MIN. Value
Control	μPD78078Y	48 K to 60 K	3-wire/2-wire/I^2C: 1 ch 3-wire with automatic transmit/receive function: 1 ch 3-wire/UART: 1 ch	88	1.8 V
	μPD78070AY	—		61	2.7 V
	μPD780018AY	48 K to 60 K	3-wire with automatic transmit/receive function: 1 ch Time-division 3-wire: 1 ch I^2C bus (multimaster supported): 1 ch	88	
	μPD780058Y	24 K to 60 K	3-wire/2-wire/I^2C: 1 ch 3-wire with automatic transmit/receive function: 1 ch 3-wire/time-division UART: 1 ch	68	1.8 V
	μPD78058FY	48 K to 60 K	3-wire/2-wire/I^2C: 1 ch 3-wire with automatic transmit/receive function: 1 ch 3-wire/UART: 1 ch	69	2.7 V
	μPD78054Y	16 K to 60 K			2.0 V
	μPD780078Y	48 K to 60 K	3-wire: 1 ch UART: 1 ch 3-wire/UART: 1 ch I^2C bus (multimaster supported): 1 ch	52	1.8 V
	μPD780034AY	8 K to 32 K	UART: 1 ch 3-wire: 1 ch I^2C bus (multimaster supported): 1 ch	51	1.8 V
	μPD780024AY				
	μPD78018FY	8 K to 60 K	3-wire/2-wire/I^2C: 1 ch 3-wire with automatic transmit/receive function: 1 ch	53	
LCD drive	μPD780308Y	48 K to 60 K	3-wire/2-wire/I^2C: 1 ch 3-wire/time-division UART: 1 ch 3-wire: 1 ch	57	2.0 V
	μPD78064Y	16 K to 32 K	3-wire/2-wire/I^2C: 1 ch 3-wire/UART: 1 ch		

Remark Functions other than the serial interface are common to the non-Y subseries.

OVERVIEW OF FUNCTIONS

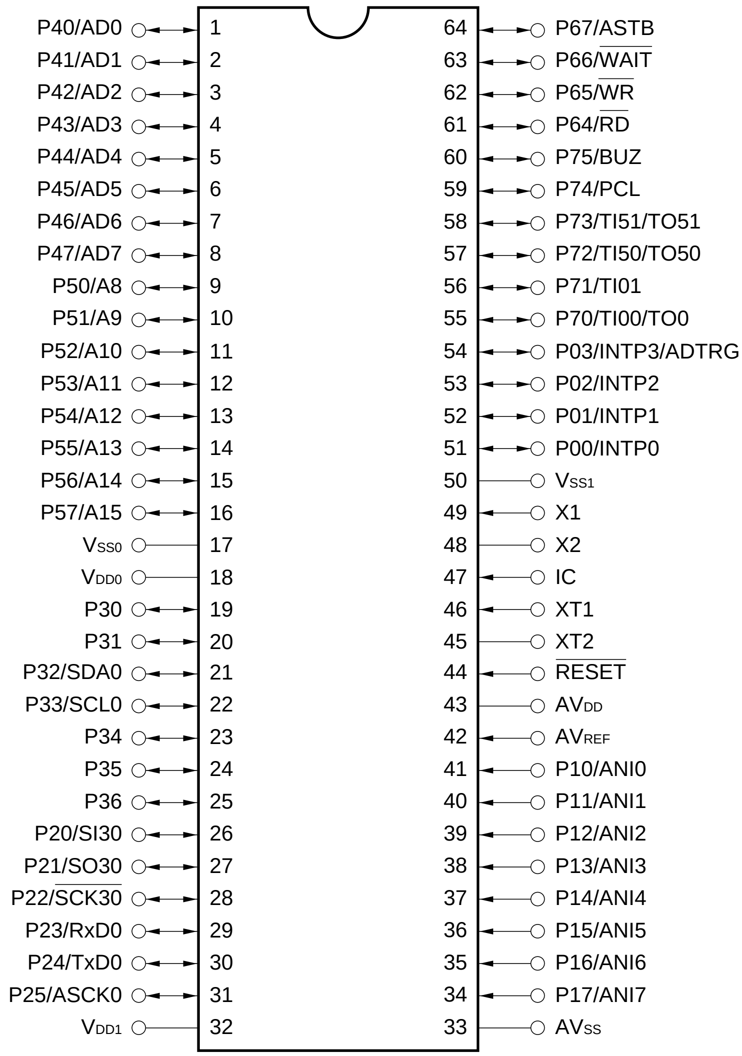
Item		μPD780031AY	μPD780032AY	μPD780033AY	μPD780034AY
Internal memory	ROM	8 Kbytes	16 Kbytes	24 Kbytes	32 Kbytes
	High-speed RAM	512 bytes		1024 bytes	
Memory space		64 Kbytes			
General-purpose registers		8 bits × 32 registers (8 bits × 8 registers × 4 banks)			
Minimum instruction execution time		On-chip minimum instruction execution time cycle variable function			
	When main system clock selected	0.24 μs/0.48 μs/0.95 μs/1.91 μs/3.81 μs (@ 8.38-MHz operation)			
	When subsystem clock selected	122 μs (@ 32.768-kHz operation)			
Instruction set		• 16-bit operation • Multiply/divide (8 bits × 8 bits,16 bits ÷ 8 bits) • Bit manipulation (set, reset, test, Boolean operation) • BCD adjust, etc.			
I/O ports		Total: 51 • CMOS input: 8 • CMOS I/O: 39 • 5-V-tolerant N-ch open-drain I/O: 4			
A/D converter		• 10-bit resolution x 8 channels • Low-voltage operation available: AV_{DD} = 1.8 to 5.5 V			
Serial interface		• 3-wire serial I/O mode: 1 channel • UART mode: 1 channel • I^2C bus mode (multimaster supported): 1 channel			
Timer		• 16-bit timer/event counter: 1 channel • 8-bit timer/event counter: 2 channels • Watch timer: 1 channel • Watchdog timer: 1 channel			
Timer output		3 (8-bit PWM output capable: 2)			
Clock output		• 65.5 kHz, 131 kHz, 262 kHz, 524 kHz, 1.05 MHz, 2.10 MHz, 4.19 MHz, 8.38 MHz (@ 8.38-MHz operation with main system clock) • 32.768 kHz (@ 32.768-kHz operation with subsystem clock)			
Buzzer output		1.02 kHz, 2.05 kHz, 4.10 kHz, 8.19 kHz (@ 8.38-MHz operation with main system clock)			
Vectored interrupt sources	Maskable	Internal: 13, external: 5			
	Non-maskable	Internal: 1			
	Software	1			
Power supply voltage		V_{DD} = 1.8 to 5.5 V			
Operating ambient temperature		T_A = –40 to +85°C			
Package		• 64-pin plastic shrink DIP (750 mils) • 64-pin plastic QFP (14 × 14 mm) • 64-pin plastic LQFP (12 × 12 mm)			

CONTENTS

1. PIN CONFIGURATION (Top View)

- **64-pin plastic shrink DIP (750 mils)**

  μPD780031AYCW-×××, 780032AYCW-×××, 780033AYCW-×××, 780034AYCW-×××

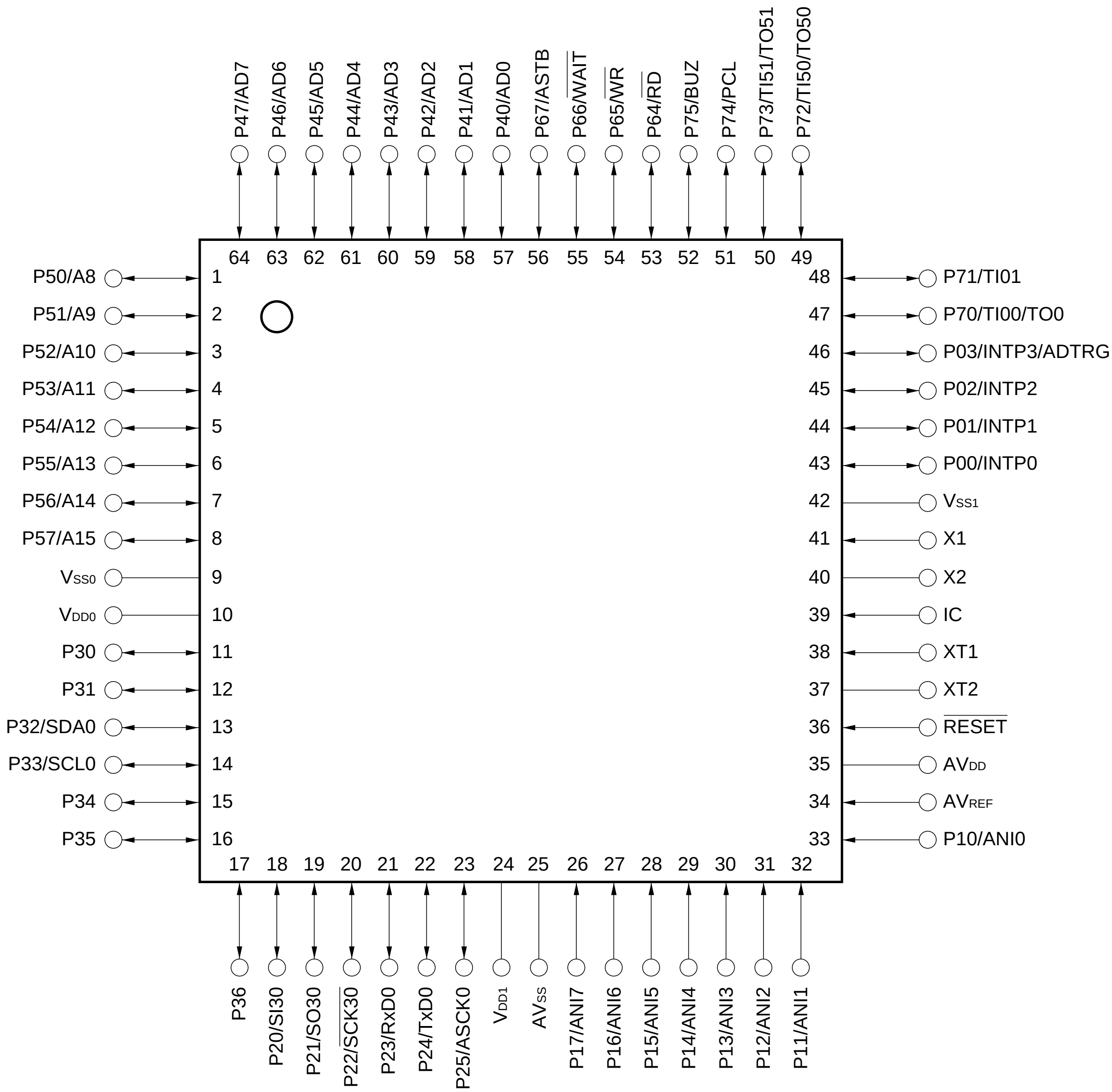


Cautions 1. Connect the IC (Internally Connected) pin directly to V_{SS0} or V_{SS1}.

2. Connect the AV_{SS} pin to V_{SS0}.

Remark When the μPD780031AY, 780032AY, 780033AY, and 780034AY are used in applications where the noise generated inside the microcontroller needs to be reduced, the implementation of noise reduction measures, such as supplying voltage to V_{DD0} and V_{DD1} individually and connecting V_{SS0} and V_{SS1} to different ground lines, is recommended.

- **64-pin plastic QFP (14 × 14 mm)**
  µPD780031AYGC-×××-AB8, 780032AYGC-×××-AB8, 780033AYGC-×××-AB8, 780034AYGC-×××-AB8
- **64-pin plastic LQFP (12 × 12 mm)**
  µPD780031AYGK-×××-8A8, 780032AYGK-×××-8A8, 780033AYGK-×××-8A8, 780034AYGK-×××-8A8



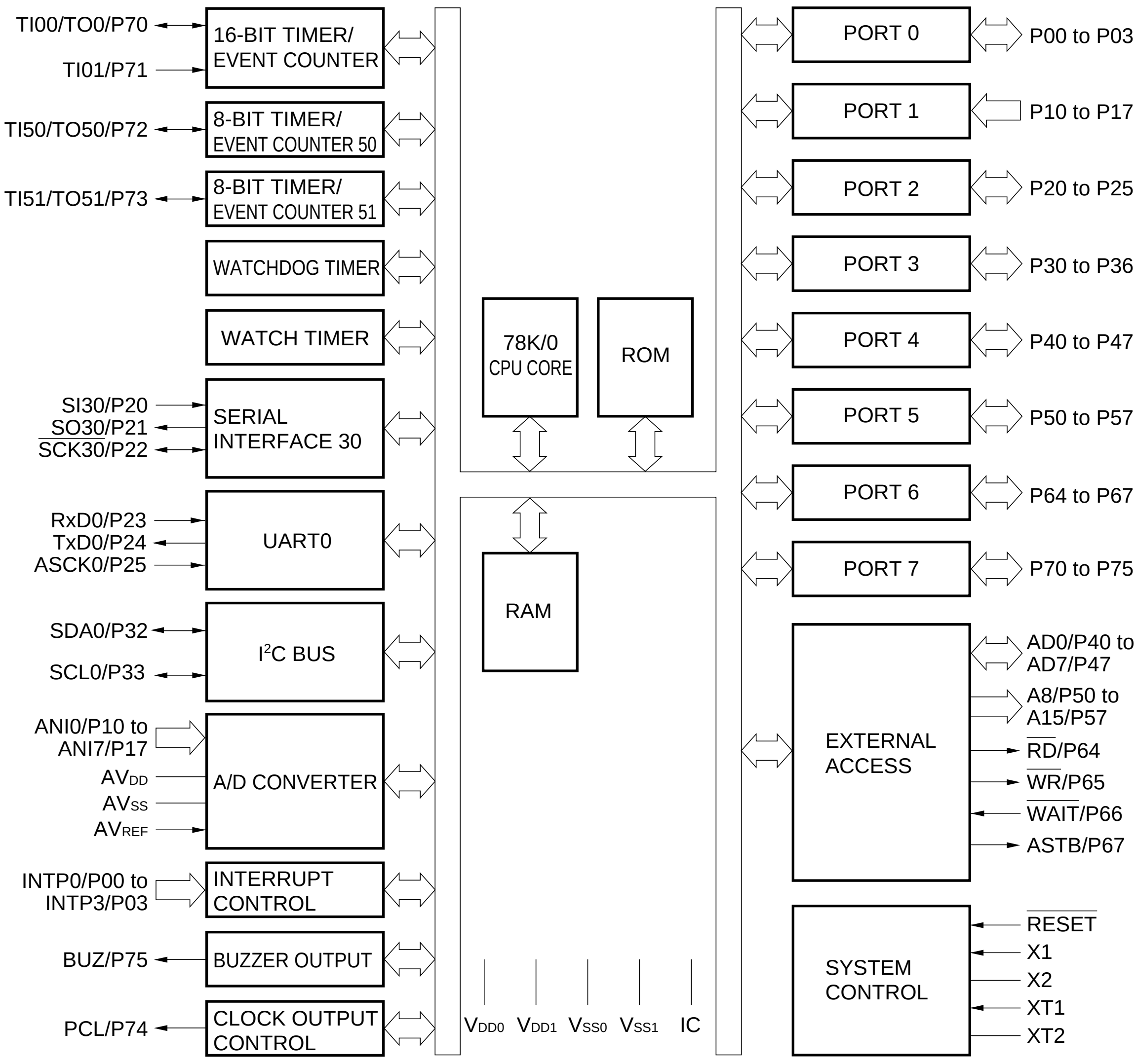
Cautions 1. Connect the IC (Internally Connected) pin directly to V_{SS0} or V_{SS1}.

2. Connect the AV_{SS} pin to V_{SS0}.

Remark When the µPD780031AY, 780032AY, 780033AY, and 780034AY are used in applications where the noise generated inside the microcontroller needs to be reduced, the implementation of noise reduction measures, such as supplying voltage to V_{DD0} and V_{DD1} individually and connecting V_{SS0} and V_{SS1} to different ground lines, is recommended.

A8 to A15:	Address Bus
AD0 to AD7:	Address/Data Bus
ADTRG:	AD Trigger Input
ANI0 to ANI7:	Analog Input
ASCK0:	Asynchronous Serial Clock
ASTB:	Address Strobe
AV_{DD}:	Analog Power Supply
AV_{REF}:	Analog Reference Voltage
AV_{SS}:	Analog Ground
BUZ:	Buzzer Clock
IC:	Internally Connected
INTP0 to INTP3:	External Interrupt Input
P00 to P03:	Port 0
P10 to P17:	Port 1
P20 to P25:	Port 2
P30 to P36:	Port 3
P40 to P47:	Port 4
P50 to P57:	Port 5
P64 to P67:	Port 6
P70 to P75:	Port 7
PCL:	Programmable Clock
$\overline{RD}$:	Read Strobe
$\overline{RESET}$:	Reset
RxD0:	Receive Data
$\overline{SCK30}$, SCL0:	Serial Clock
SDA0:	Serial Data
SI30:	Serial Input
SO30:	Serial Output
TI00, TI01, TI50, TI51:	Timer Input
TO0, TO50, TO51:	Timer Output
TxD0:	Transmit Data
V_{DD0}, V_{DD1}:	Power Supply
V_{SS0}, V_{SS1}:	Ground
$\overline{WAIT}$:	Wait
$\overline{WR}$:	Write Strobe
X1, X2:	Crystal (Main System Clock)
XT1, XT2:	Crystal (Subsystem Clock)

2. BLOCK DIAGRAM



Remark The internal ROM and RAM capacities differ depending on the product.

3. PIN FUNCTIONS

3.1 Port Pins (1/2)

Pin Name	I/O	Function		After Reset	Alternate Function
P00	I/O	Port 0 4-bit input/output port Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be connected by means of software.		Input	INTP0
P01					INTP1
P02					INTP2
P03					INTP3/ADTRG
P10 to P17	Input	Port 1 8-bit input-only port		Input	ANI0 to ANI7
P20	I/O	Port 2 6-bit input/output port Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be connected by means of software.		Input	SI30
P21					SO30
P22					$\overline{\text{SCK30}}$
P23					RxD0
P24					TxD0
P25					ASCK0
P30	I/O	Port 3 7-bit input/output port Input/output can be specified in 1-bit units.	N-ch open-drain input/output port The mask option can be used to specify the connection of an on-chip pull-up resistor to P30, P31. LEDs can be driven directly.	Input	—
P31					
P32					SDA0
P33					SCL0
P34			An on-chip pull-up resistor can be connected by means of software.		—
P35					
P36					
P40 to P47	I/O	Port 4 8-bit input/output port Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be connected by means of software. The interrupt request flag (KRIF) is set to 1 by falling edge detection.		Input	AD0 to AD7
P50 to P57	I/O	Port 5 8-bit input/output port LEDs can be driven directly. Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be connected by means of software.		Input	A8 to A15
P64	I/O	Port 6 4-bit input/output port Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be connected by means of software.		Input	$\overline{\text{RD}}$
P65					$\overline{\text{WR}}$
P66					$\overline{\text{WAIT}}$
P67					ASTB

3.1 Port Pins (2/2)

Pin Name	I/O	Function	After Reset	Alternate Function
P70	I/O	Port 7 6-bit input/output port Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be connected by means of software.	Input	TI00/TO0
P71				TI01
P72				TI50/TO50
P73				TI51/TO51
P74				PCL
P75				BUZ

3.2 Non-Port Pins (1/2)

Pin Name	I/O	Function	After Reset	Alternate Function
INTP0	Input	External interrupt request input for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified	Input	P00
INTP1				P01
INTP2				P02
INTP3				P03/ADTRG
SI30	Input	Serial interface serial data input	Input	P20
SO30	Output	Serial interface serial data output	Input	P21
SDA0	I/O	Serial interface serial data input/output	Input	P32
$\overline{\text{SCK30}}$	I/O	Serial interface serial clock input/output	Input	P22
SCL0				P33
RxD0	Input	Serial data input for asynchronous serial interface	Input	P23
TxD0	Output	Serial data output for asynchronous serial interface	Input	P24
ASCK0	Input	Serial clock input for asynchronous serial interface	Input	P25
TI00	Input	External count clock input to 16-bit timer (TM0) Capture trigger input to capture register (CR01) of 16-bit timer (TM0)	Input	P70/TO0
TI01		Capture trigger input to capture register (CR00) of 16-bit timer (TM0)		P71
TI50		External count clock input to 8-bit timer (TM50)		P72/TO50
TI51		External count clock input to 8-bit timer (TM51)		P73/TO51
TO0	Output	16-bit timer (TM0) output	Input	P70/TI00
TO50		8-bit timer (TM50) output (also used for 8-bit PWM output)	Input	P72/TI50
TO51		8-bit timer (TM51) output (also used for 8-bit PWM output)		P73/TI51
PCL	Output	Clock output (for trimming of main system clock and subsystem clock)	Input	P74
BUZ	Output	Buzzer output	Input	P75
AD0 to AD7	I/O	Lower address/data bus for expanding memory externally	Input	P40 to P47
A8 to A15	Output	Higher address bus for expanding memory externally	Input	P50 to P57
$\overline{\text{RD}}$	Output	Strobe signal output for reading from external memory	Input	P64
$\overline{\text{WR}}$		Strobe signal output for writing to external memory		P65
$\overline{\text{WAIT}}$	Input	Wait insertion at external memory access	Input	P66
ASTB	Output	Strobe output that externally latches address information output to ports 4 and 5 to access external memory	Input	P67

3.2 Non-Port Pins (2/2)

Pin Name	I/O	Function	After Reset	Alternate Function
ANI0 to ANI7	Input	A/D converter analog input	Input	P10 to P17
ADTRG	Input	A/D converter trigger signal input	Input	P03/INTP3
AV_{REF}	Input	A/D converter reference voltage input	—	—
AV_{DD}	—	A/D converter analog power supply. Set potential to that of V_{DD0} or V_{DD1}.	—	—
AV_{SS}	—	A/D converter ground potential. Set potential to that of V_{SS0} or V_{SS1}.	—	—
$\overline{RESET}$	Input	System reset input	—	—
X1	Input	Connecting crystal resonator for main system clock oscillation	—	—
X2	—		—	—
XT1	Input	Connecting crystal resonator for subsystem clock oscillation	—	—
XT2	—		—	—
V_{DD0}	—	Positive power supply for ports	—	—
V_{SS0}	—	Ground potential of ports	—	—
V_{DD1}	—	Positive power supply (except ports)	—	—
V_{SS1}	—	Ground potential (except ports)	—	—
IC	—	Internally connected. Connect directly to V_{SS0} or V_{SS1}.	—	—

3.3 Pin I/O Circuits and Recommended Connection of Unused Pins

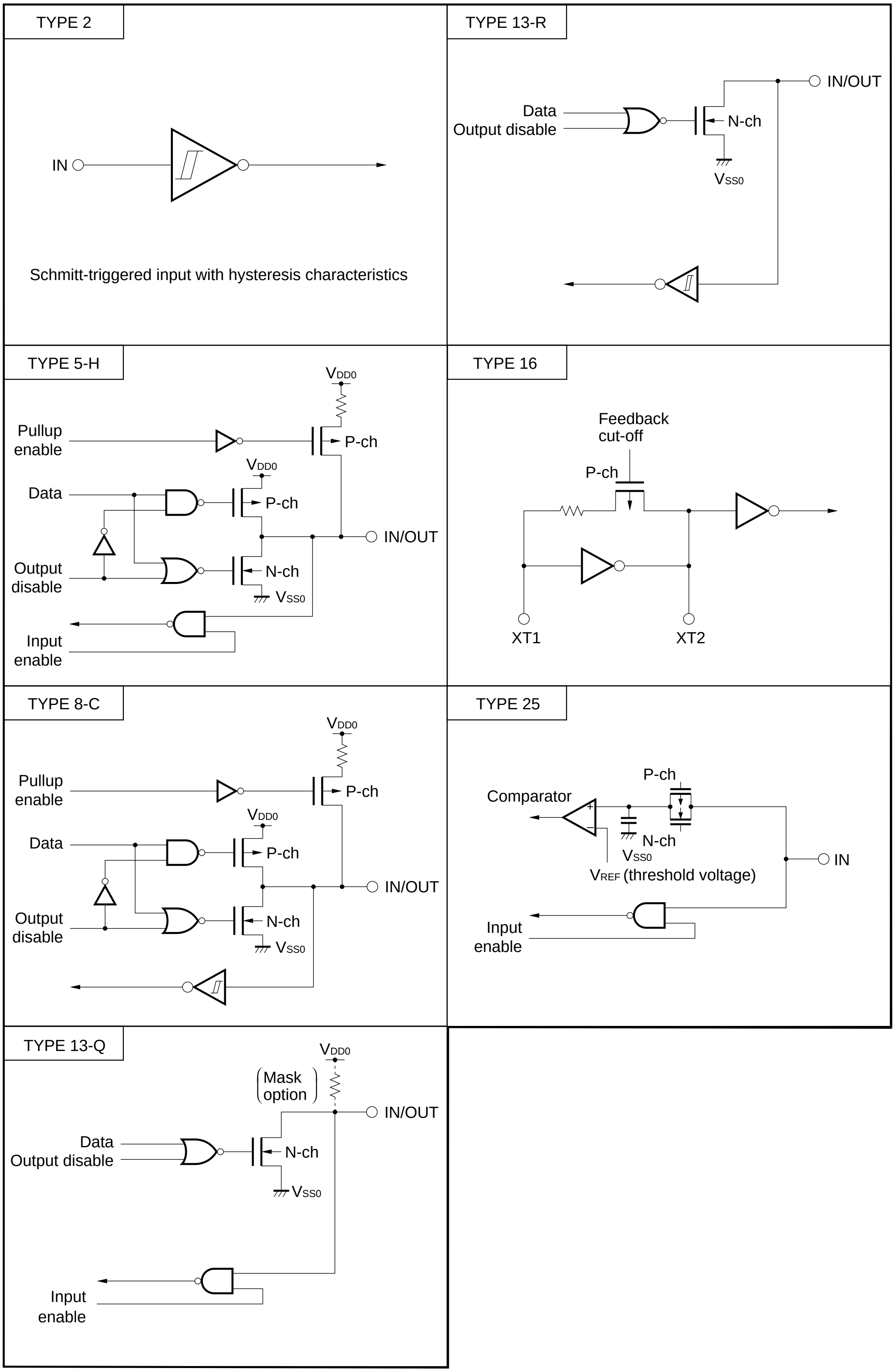
The input/output circuit type of each pin and recommended connection of unused pins are shown in Table 3-1.

For the input/output circuit configuration of each type, see Figure 3-1.

Table 3-1. Types of Pin Input/Output Circuits

Pin Name	Input/Output Circuit Type	I/O	Recommended Connection of Unused Pins
P00/INTP0 to P02/INTP2	8-C	Input	Independently connect to V_{SS0} via a resistor.
P03/INTP3/ADTRG			
P10/ANI0 to P17/ANI7	25	Input	Independently connect to V_{DD0} or V_{SS0} via a resistor.
P20/SI30	8-C	I/O	
P21/SO30	5-H		
P22/$\overline{SCK30}$	8-C		
P23/RxD0			
P24/TxD0	5-H		
P25/ASCK0	8-C		
P30, P31	13-Q	I/O	Independently connect to V_{DD0} via a resistor.
P32/SDA0	13-R		
P33/SCL0			
P34	8-C		Independently connect to V_{DD0} or V_{SS0} via a resistor.
P35	5-H		
P36	8-C		
P40/AD0 to P47/AD7	5-H	I/O	Independently connect to V_{DD0} via a resistor.
P50/A8 to P57/A15		I/O	Independently connect to V_{DD0} or V_{SS0} via a resistor.
P64/$\overline{RD}$		I/O	
P65/$\overline{WR}$			
P66/$\overline{WAIT}$			
P67/ASTB			
P70/TI00/TO0	8-C		
P71/TI01			
P72/TI50/TO50			
P73/TI51/TO51			
P74/PCL	5-H		
P75/BUZ			
$\overline{RESET}$	2	Input	—
XT1	16		Connect to V_{DD0}.
XT2		—	Leave open.
AV_{DD}	—		Connect to V_{DD0}.
AV_{REF}			Connect to V_{SS0}.
AV_{SS}			
IC			Connect directly to V_{SS0} or V_{SS1}.

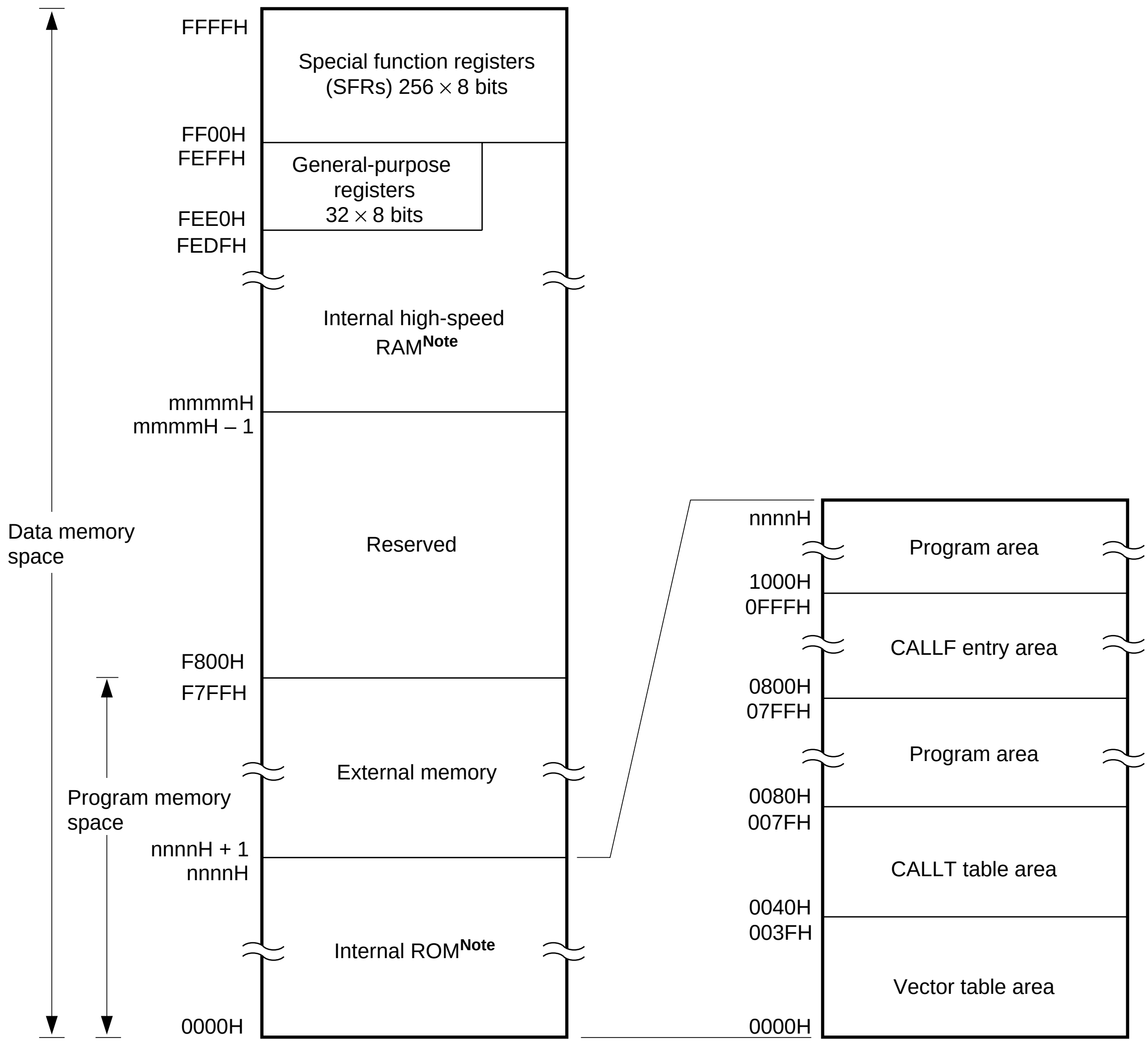
Figure 3-1. Pin Input/Output Circuits



4. MEMORY SPACE

Figure 4-1 shows the memory map of the μPD780031AY, 780032AY, 780033AY, and 780034AY.

Figure 4-1. Memory Map



Note The internal ROM and internal high-speed RAM capacities differ depending on the product (see the following table).

Part Number	Last Address of Internal ROM nnnnH	Start Address of Internal High-Speed RAM mmmmH
μPD780031AY	1FFFH	FD00H
μPD780032AY	3FFFH	
μPD780033AY	5FFFH	FB00H
μPD780034AY	7FFFH	

5. PERIPHERAL HARDWARE FUNCTION FEATURES

5.1 Ports

The following 3 types of I/O ports are available.

- CMOS input (Port 1): 8
- CMOS input/output (Ports 0, 2 to 7, P34 to P36): 39
- N-ch open-drain input/output (P30 to P33): 4

Total: 51

Table 5-1. Port Functions

Name	Pin Name	Function
Port 0	P00 to P03	I/O port pins. Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be connected by means of software.
Port 1	P10 to P17	Dedicated input port pins.
Port 2	P20 to P25	I/O port pins. Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be connected by means of software.
Port 3	P30 to P33	N-ch open-drain I/O port pins. Input/output can be specified in 1-bit units. The mask option can be used to specify the connection of an on-chip pull-up resistor to P30, P31. LEDs can be driven directly.
	P34 to P36	I/O port pins. Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be connected by means of software.
Port 4	P40 to P47	I/O port pins. Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be connected by means of software. The interrupt request flag (KRIF) is set to 1 by falling edge detection.
Port 5	P50 to P57	I/O port pins. Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be connected by means of software. LEDs can be driven directly.
Port 6	P64 to P67	I/O port pins. Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be connected by means of software.
Port 7	P70 to P75	I/O port pins. Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be connected by means of software.

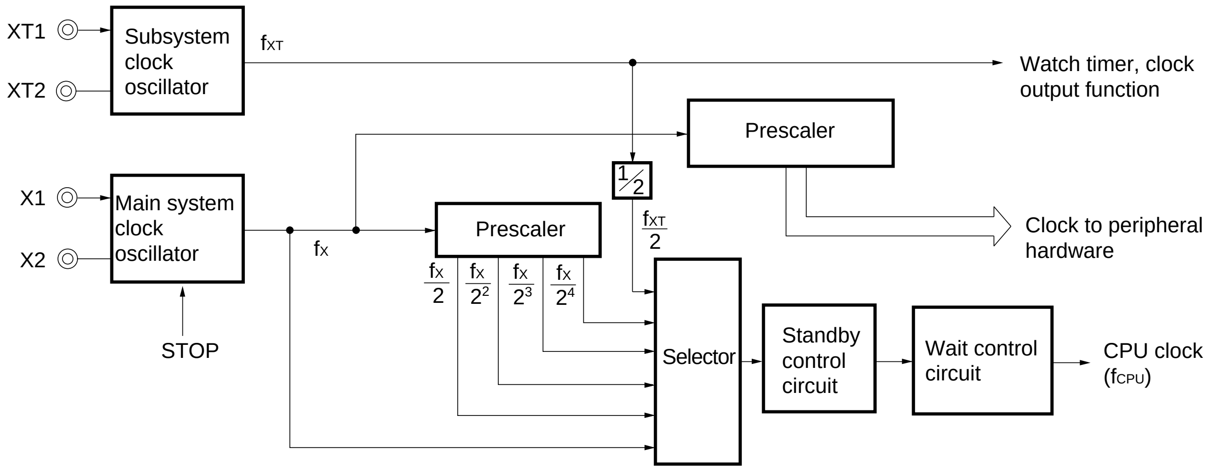
5.2 Clock Generator

A system clock generator is incorporated.

The minimum instruction execution time can be changed.

- 0.24 μs/0.48 μs/0.95 μs/1.91 μs/3.81 μs (@ 8.38-MHz operation with main system clock)
- 122 μs (@ 32.768-kHz operation with subsystem clock)

Figure 5-1. Clock Generator Block Diagram



5.3 Timer/Counter

Five timer/counter channels are incorporated.

- 16-bit timer/event counter: 1 channel
- 8-bit timer/event counter: 2 channels
- Watch timer: 1 channel
- Watchdog timer: 1 channel

Table 5-2. Operations of Timer/Event Counters

		16-Bit Timer/ Event Counter TM0	8-Bit Timer/ Event Counters TM50, TM51	Watch Timer	Watchdog Timer
Operation mode					
	Interval timer	1 channel	2 channels	1 channel[Note 1]	1 channel[Note 2]
	External event counter	1 channel	2 channels	—	—
Function					
	Timer output	1 output	2 outputs	—	—
	PPG output	1 output	—	—	—
	PWM output	—	2 outputs	—	—
	Pulse width measurement	2 inputs	—	—	—
	Square wave output	1 output	2 outputs	—	—
	One-shot pulse output	1 output	—	—	—
	Interrupt source	2	2	2	1

Notes 1. The watch timer can perform both watch timer and interval timer functions at the same time.

2. The watchdog timer has watchdog timer and interval timer functions. However, use the watchdog timer by selecting either the watchdog timer function or the interval timer function.

Figure 5-2. Block Diagram of 16-Bit Timer/Event Counter TM0

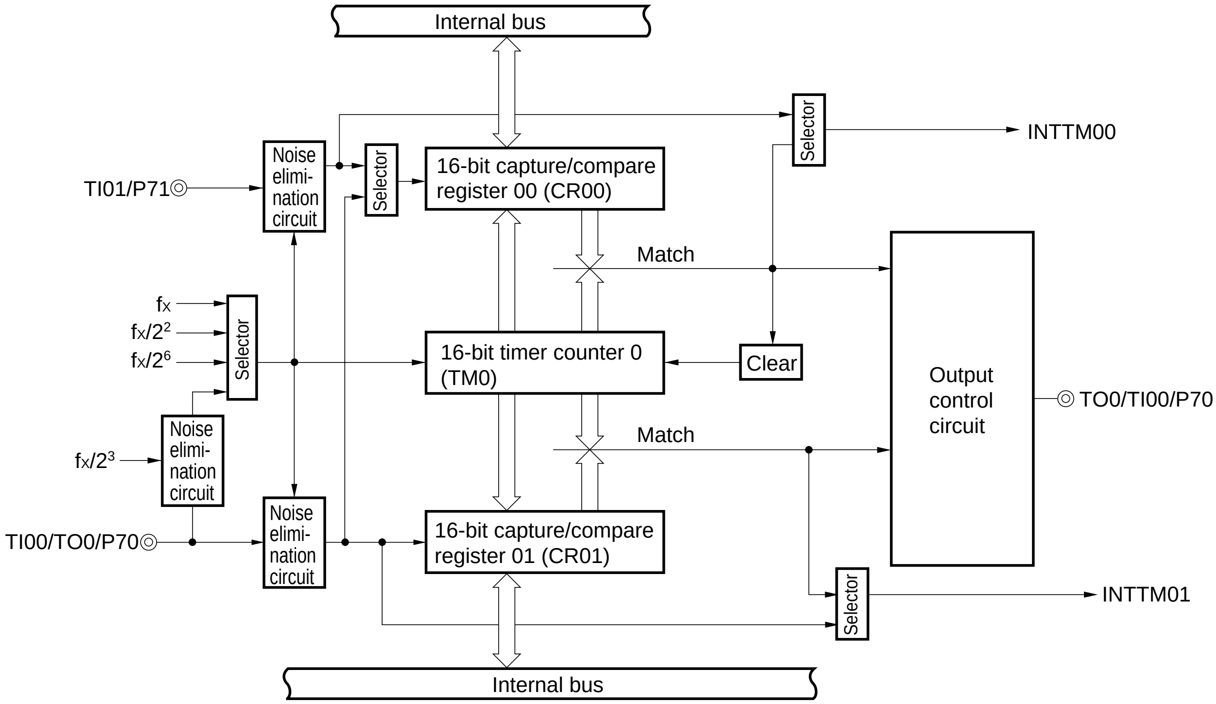


Figure 5-3. Block Diagram of 8-Bit Timer/Event Counter TM50

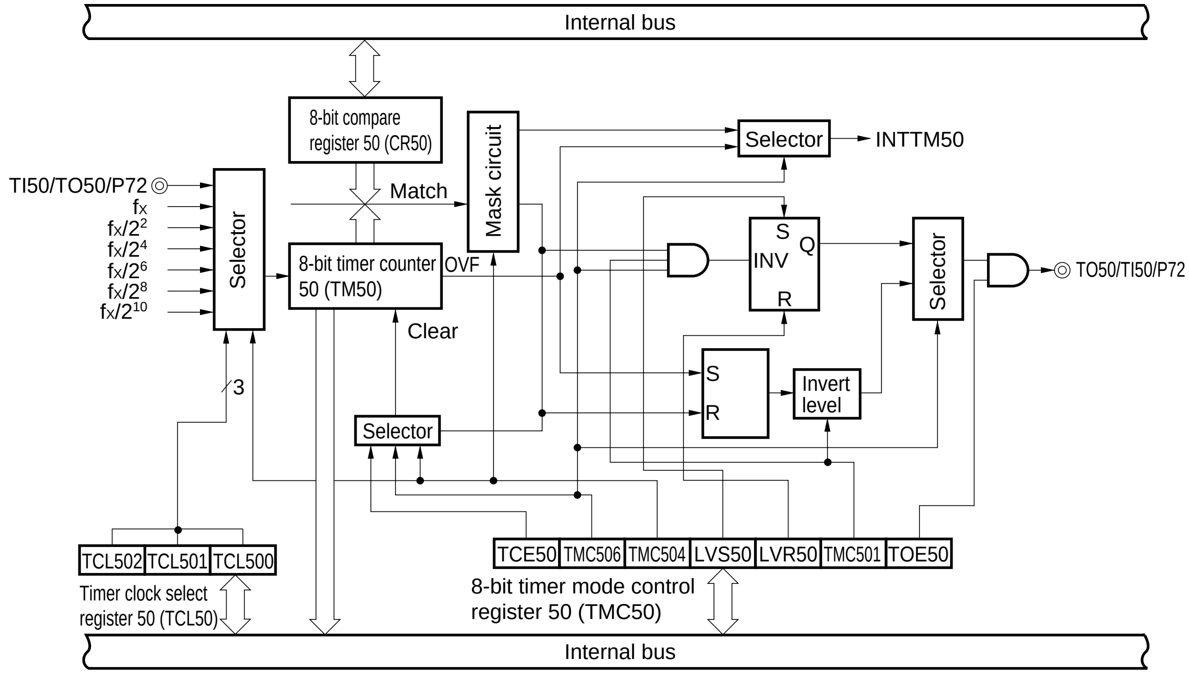


Figure 5-4. Block Diagram of 8-Bit Timer/Event Counter TM51

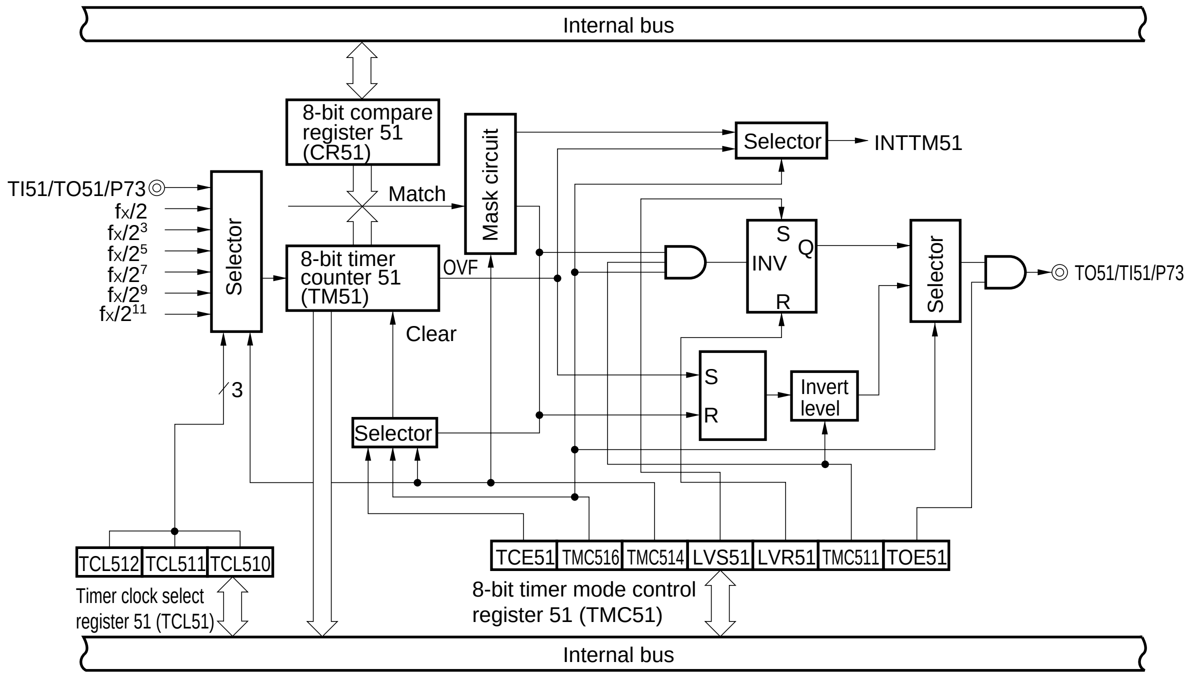


Figure 5-5. Watch Timer Block Diagram

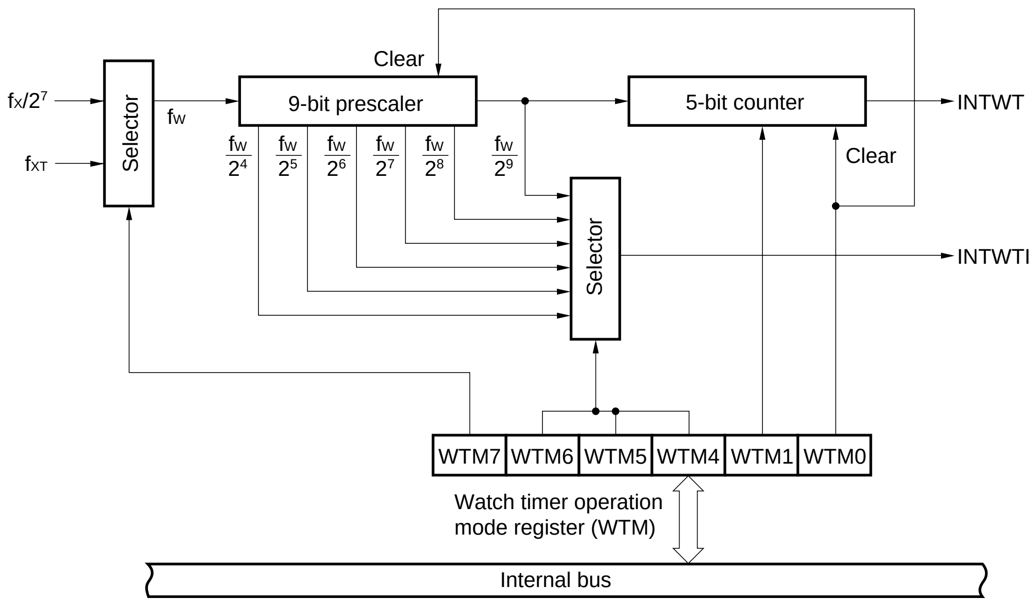
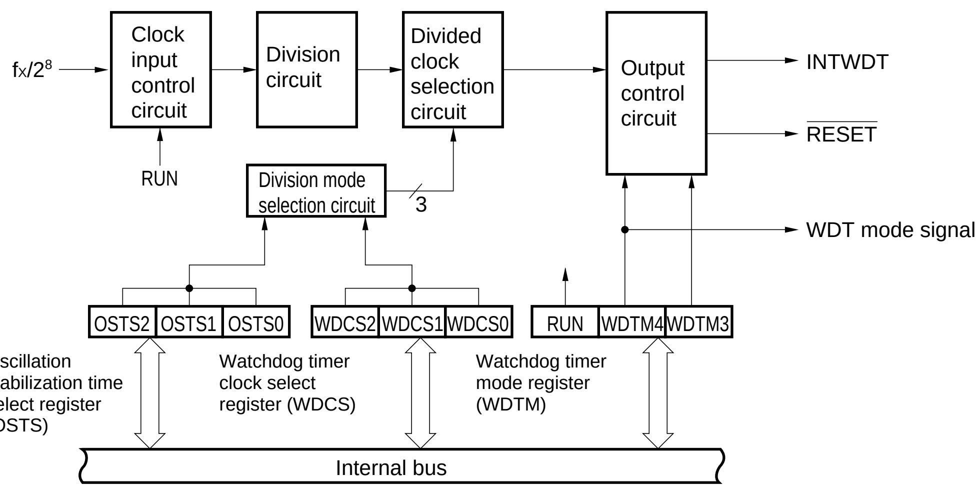


Figure 5-6. Watchdog Timer Block Diagram



5.4 Clock Output/Buzzer Output Control Circuit

A clock output/buzzer output control circuit (CKU) is incorporated.

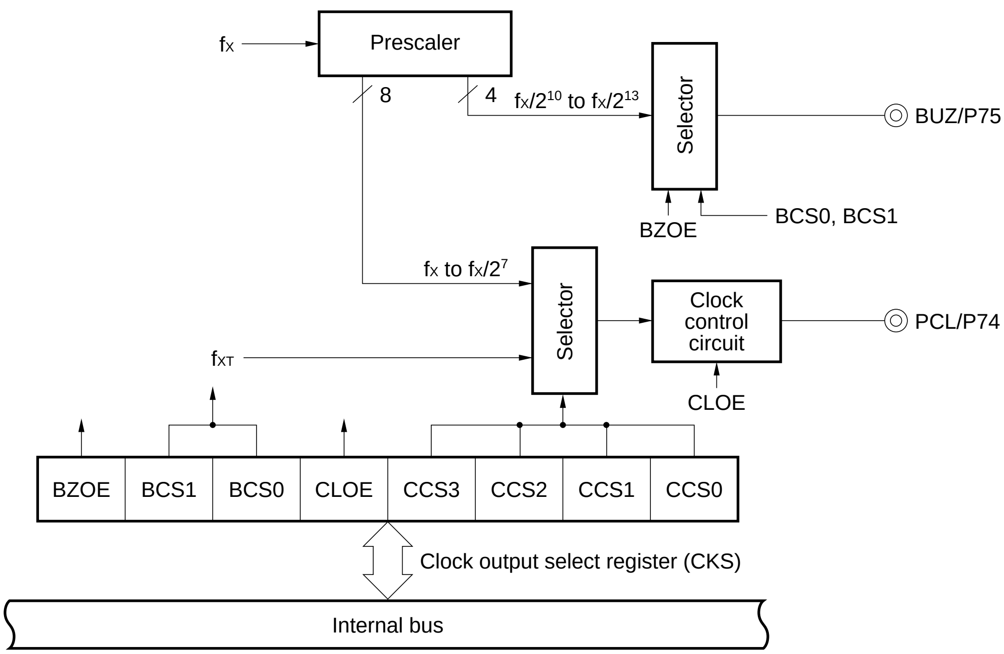
Clocks with the following frequencies can be output as clock output.

- 65.5 kHz/131 kHz/262 kHz/524 kHz/1.05 MHz/2.10 MHz/4.19 MHz/8.38 MHz (@ 8.38-MHz operation with main system clock)
- 32.768 kHz (@ 32.768-kHz operation with subsystem clock)

Clocks with the following frequencies can be output as buzzer output.

- 1.02 kHz/2.05 kHz/4.10 kHz/8.19 kHz (@ 8.38-MHz operation with main system clock)

Figure 5-7. Block Diagram of Clock Output/Buzzer Output Control Circuit CKU



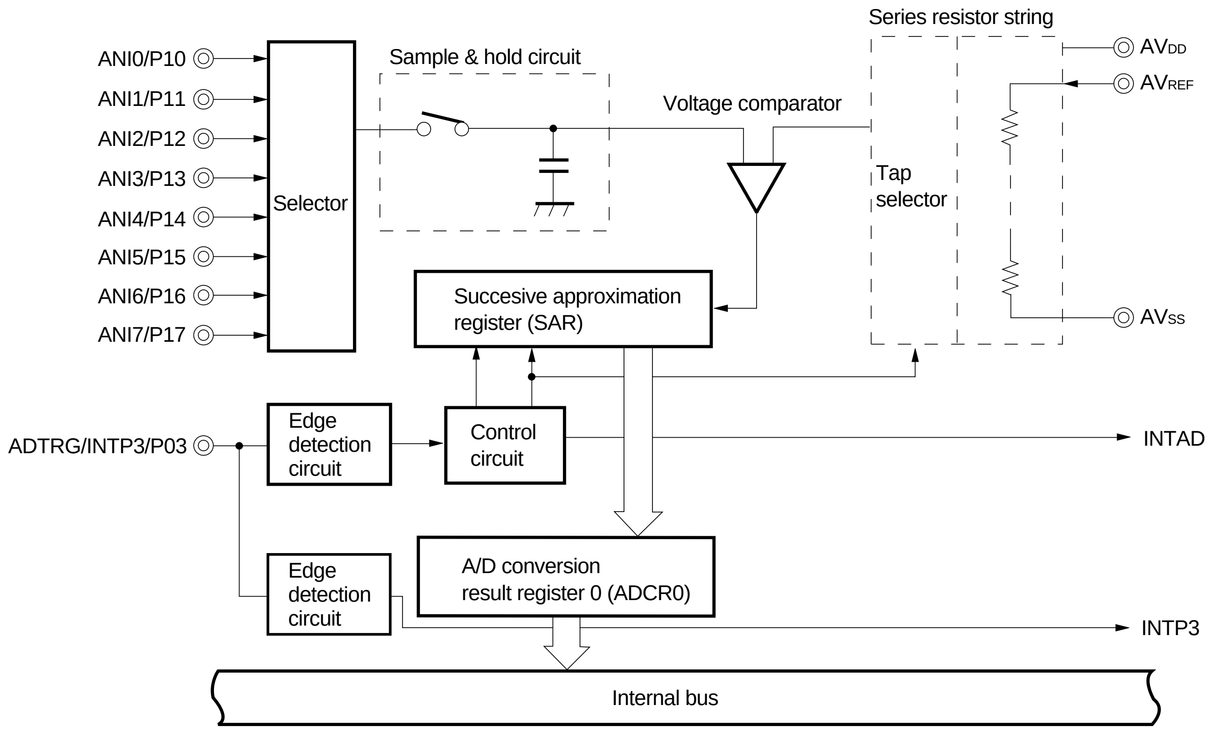
5.5 A/D Converter

An A/D converter consisting of eight 10-bit resolution channels is incorporated.

The following two A/D conversion operation start-up methods are available.

- Hardware start
- Software start

Figure 5-8. A/D Converter Block Diagram



5.6 Serial Interface

Three serial interface channels are incorporated.

- Serial interface UART0: 1 channel
- Serial interface SIO30: 1 channel
- Serial interface IIC0: 1 channel

(1) Serial interface UART0

The serial interface UART0 has two modes: asynchronous serial interface (UART) mode and infrared data transfer mode.

- **Asynchronous serial interface (UART) mode**

  This mode enables full-duplex operation wherein one byte of data starting from the start bit is transmitted and received.

  The on-chip UART-dedicated baud-rate generator enables communication using a wide range of selectable baud rates. In addition, a baud rate can be also defined by dividing the clock input to the ASCK0 pin.

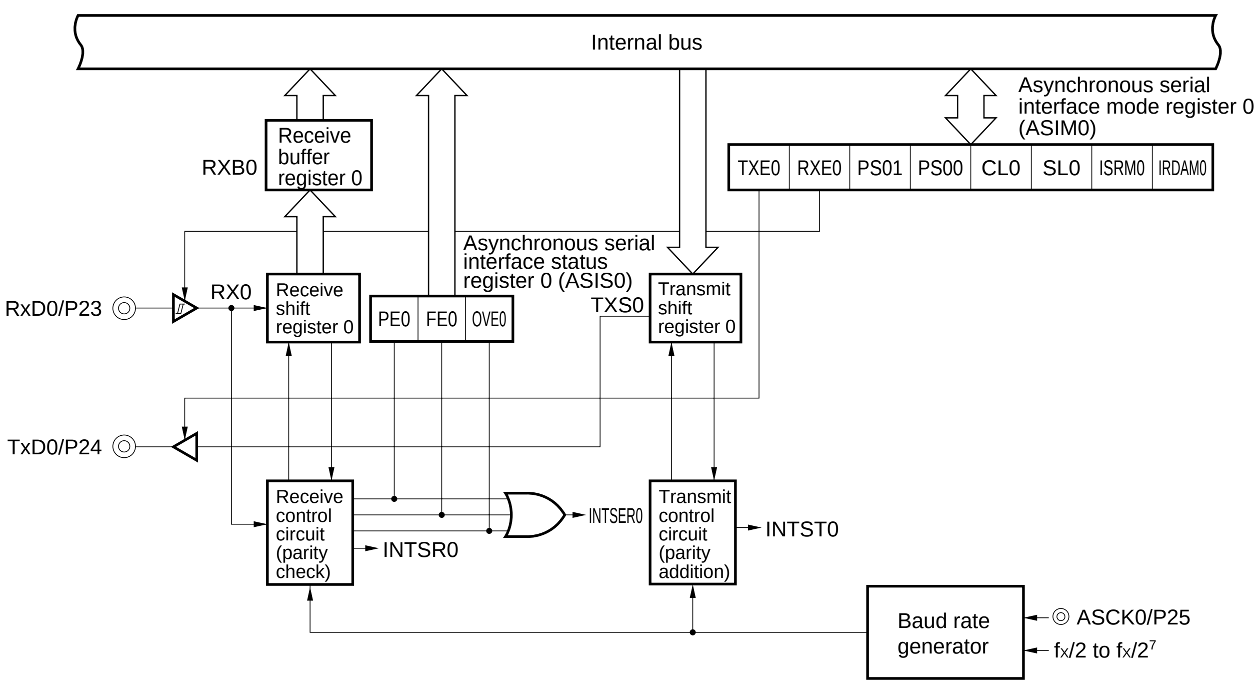
  The UART-dedicated baud-rate generator can also be used to generate a MIDI-standard baud rate (31.25 kbps).

- **Infrared data transfer mode**

  This mode enables pulse output and pulse reception in data format.

  This mode can be used for office equipment applications such as personal computers.

Figure 5-9. Block Diagram of Serial Interface UART0



(2) Serial interface SIO30

The serial interface SIO30 has one mode: 3-wire serial I/O mode.

- **3-wire serial I/O mode (fixed as MSB first)**

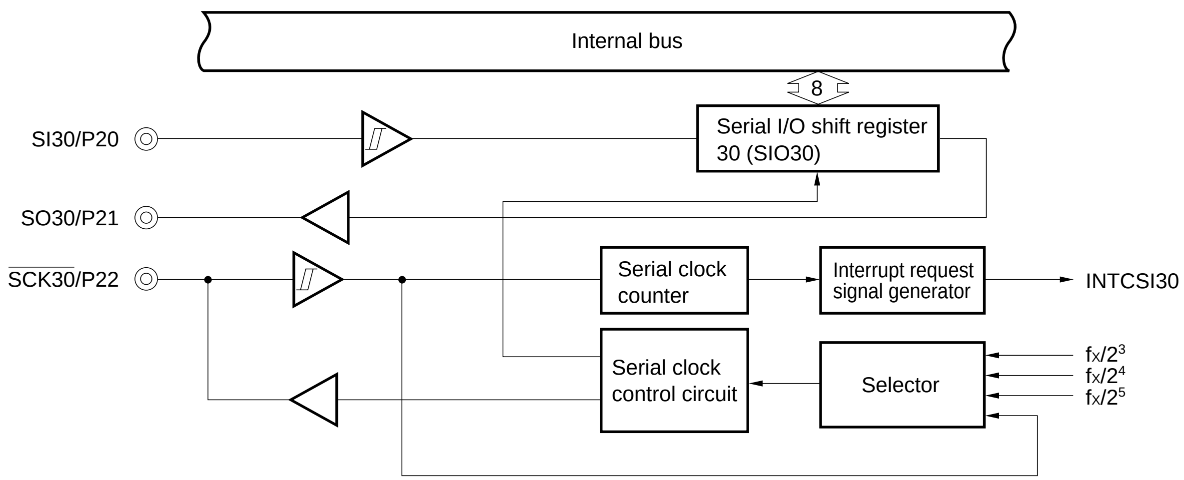
  This is an 8-bit data transfer mode using three lines: a serial clock line ($\overline{\text{SCK30}}$), serial output line (SO30), and serial input line (SI30).

  Since simultaneous transmit and receive operations are enabled in the 3-wire serial I/O mode, the processing time for data transfer is reduced.

  The first bit in 8-bit data in the serial transfer is fixed as MSB.

  The 3-wire serial I/O mode is useful for connection to peripheral I/O devices, display controllers, etc. that include a clocked serial interface.

Figure 5-10. Block Diagram of Serial Interface SIO30



(3) Serial interface IIC0

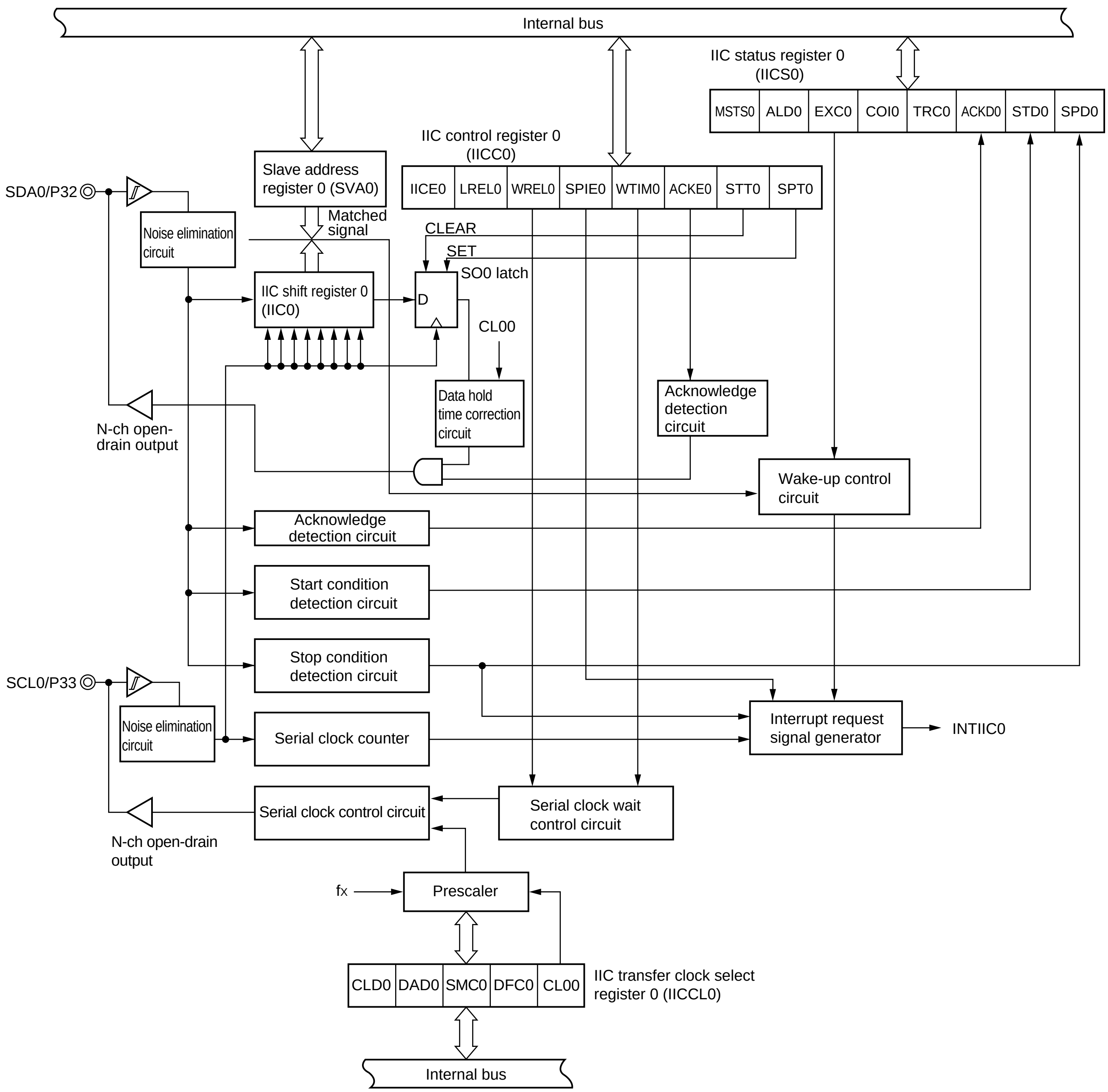
The serial interface IIC0 has the I^2C (Inter IC) bus mode (multimaster supported).

- **I^2C bus mode (multimaster supported)**

  This is an 8-bit data transfer mode using two lines: a serial clock line (SCL0) and serial data bus line (SDA0). This mode complies with the I^2C bus format, and can output "start condition", "data", and "stop condition" during transmission via the serial data bus. This data is automatically detected by hardware during reception.

  Since the SCL0 and SDA0 are open-drain outputs in IIC0, pull-up resistors for the serial clock line and the serial data bus line are required.

Figure 5-11. Block Diagram of Serial Interface IIC0



6. INTERRUPT FUNCTION

A total of 20 interrupt sources are provided, divided into the following three types.

- Non-maskable: 1
- Maskable: 18
- Software: 1

Table 6-1. Interrupt Source List

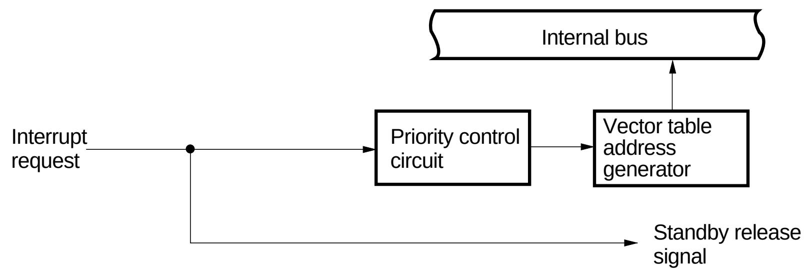
Interrupt Type	Default Priority[Note 1]	Interrupt Source Name	Interrupt Source Trigger	Internal/ External	Vector Table Address	Basic Configuration Type[Note 2]
Non-maskable	—	INTWDT	Watchdog timer overflow (with watchdog timer mode 1 selected)	Internal	0004H	(A)
Maskable	0	INTWDT	Watchdog timer overflow (with interval timer mode selected)			(B)
	1	INTP0	Pin input edge detection	External	0006H	(C)
	2	INTP1			0008H	
	3	INTP2			000AH	
	4	INTP3			000CH	
	5	INTSER0	Generation of serial interface UART0 reception error	Internal	000EH	(B)
	6	INTSR0	End of serial interface UART0 reception		0010H	
	7	INTST0	End of serial interface UART0 transmission		0012H	
	8	INTCSI30	End of serial interface SIO30 transfer		0014H	
	9	INTIIC0	End of serial interface IIC0 transfer		0016H	
	10	INTWTI	Reference time interval signal from watch timer		001AH	
	11	INTTM00	Matching of TM0 and CR00 (when CR00 is specified as a compare register) Detection of TI01 pin valid edge (when CR00 is specified as a capture register)		001CH	
	12	INTTM01	Matching of TM0 and CR01 (when CR01 is specified as a compare register) Detection of TI00 pin valid edge (when CR00 is specified as a capture register)		001EH	
	13	INTTM50	Matching of TM50 and CR50		0020H	
	14	INTTM51	Matching of TM51 and CR51		0022H	
	15	INTAD0	End of conversion by A/D converter		0024H	
	16	INTWT	Watch timer overflow		0026H	
	17	INTKR	Detection of port 4 falling edge	External	0028H	(D)
Software	—	BRK	Execution of BRK instruction	—	003EH	(E)

Notes 1. Default priority is the priority order when several maskable interrupt requests are generated at the same time. 0 is the highest and 17 is the lowest.

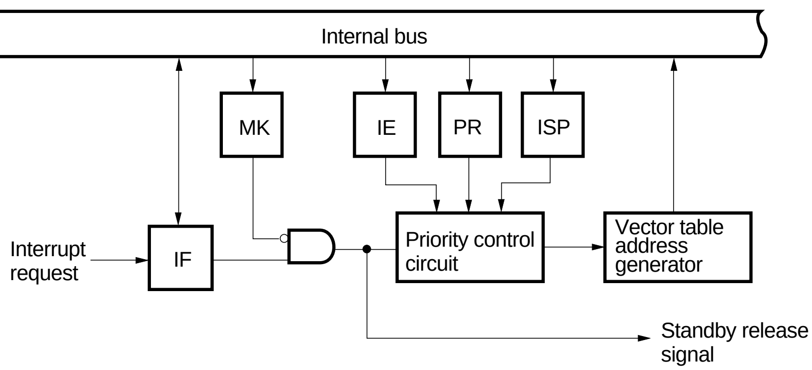
2. Basic configuration types (A) to (E) correspond to (A) to (E) in Figure 6-1.

Figure 6-1. Basic Configuration of Interrupt Function (1/2)

(A) Internal non-maskable interrupt



(B) Internal maskable interrupt



(C) External maskable interrupt (INTP0 to INTP3)

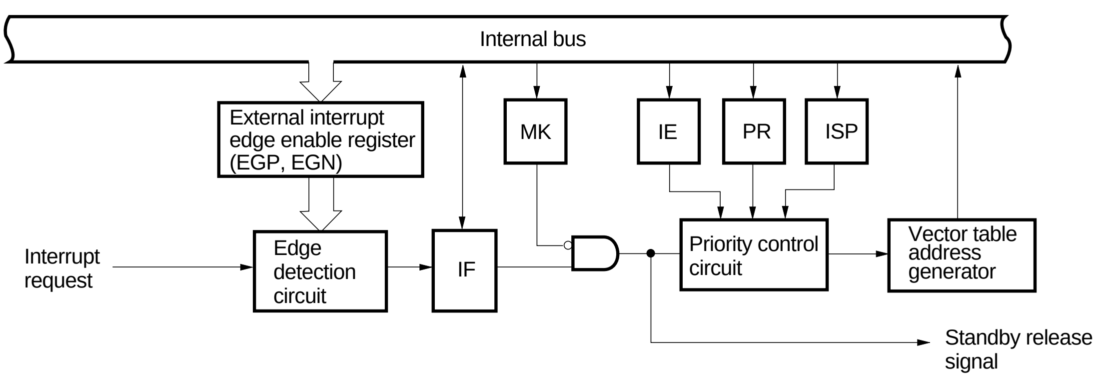
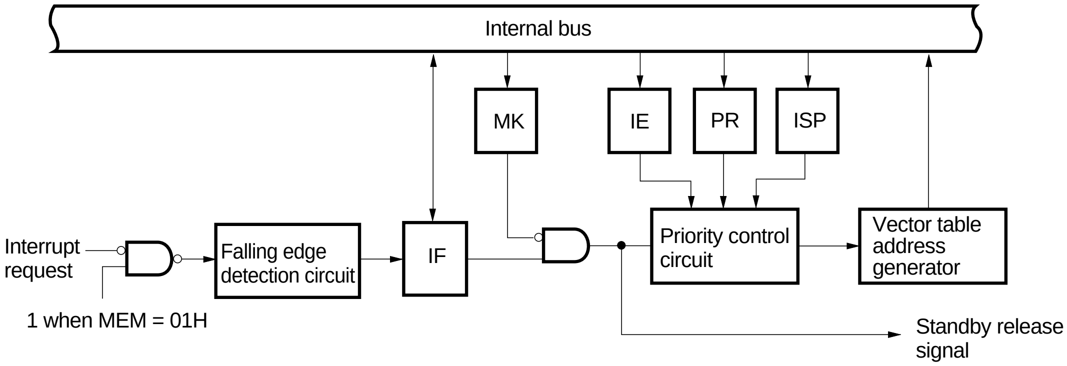
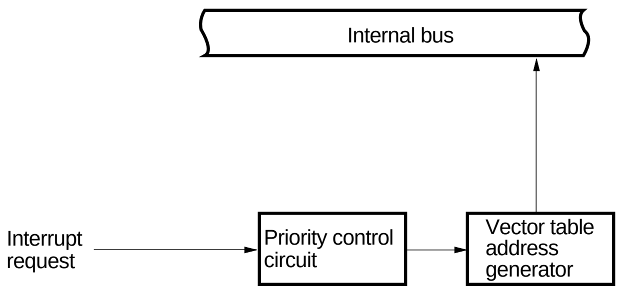


Figure 6-1. Basic Configuration of Interrupt Function (2/2)

(D) External maskable interrupt (INTKR)



(E) Software interrupt



IF: Interrupt request flag
IE: Interrupt enable flag
ISP: In-service priority flag
MK: Interrupt mask flag
PR: Priority specification flag
MEM: Memory expansion mode register

7. EXTERNAL DEVICE EXPANSION FUNCTION

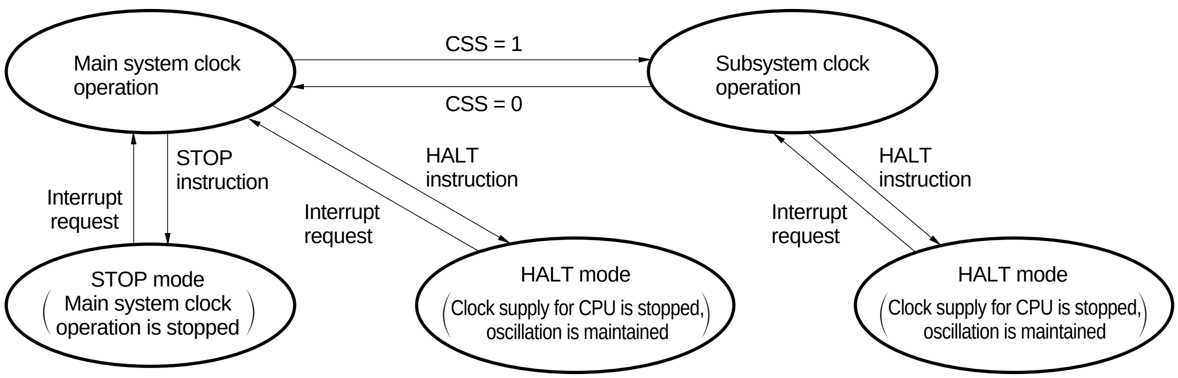
The external device expansion function is for connecting external devices to areas other than the internal ROM, RAM, and SFR. Ports 4 to 6 are used for external device connection.

8. STANDBY FUNCTION

The following two standby modes are available for further reduction of system current consumption.

- HALT mode: In this mode, the CPU operation clock is stopped. The average current consumption can be reduced by intermittent operation by combining this mode with the normal operation mode.
- STOP mode: In this mode, oscillation of the main system clock is stopped. All the operations performed on the main system clock are suspended, and only the subsystem clock is used, resulting in extremely small power consumption. This can be used only when the main system clock is operating (the subsystem clock oscillation cannot be stopped).

Figure 8-1. Standby Function



9. RESET FUNCTION

The following two reset methods are available.

- External reset by $\overline{\text{RESET}}$ signal input
- Internal reset by watchdog timer runaway time detection

10. MASK OPTION

Table 10.1 Pin Mask Option Selection

Pins	Mask Option
P30, P31	An on-chip pull-up resistor can be specified in 1-bit units.

The mask option can be used to specify the connection of an on-chip pull-up resistor to P30, P31, in 1-bit units.

11. INSTRUCTION SET

(1) 8-bit instructions

MOV, XCH, ADD, ADDC, SUB, SUBC, AND, OR, XOR, CMP, MULU, DIVUW, INC, DEC, ROR, ROL, RORC, ROLC, ROR4, ROL4, PUSH, POP, DBNZ

2nd Operand / 1st Operand	#byte	A	r[Note]	sfr	saddr	!addr16	PSW	[DE]	[HL]	[HL + byte] [HL + B] [HL + C]	$addr16	1	None
A	ADD ADDC SUB SUBC AND OR XOR CMP		MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP		ROR ROL RORC ROLC	
r	MOV	MOV ADD ADDC SUB SUBC AND OR XOR CMP											INC DEC
B, C											DBNZ		
sfr	MOV	MOV											
saddr	MOV ADD ADDC SUB SUBC AND OR XOR CMP	MOV									DBNZ		INC DEC
!addr16		MOV											
PSW	MOV	MOV											PUSH POP
[DE]		MOV											
[HL]		MOV											ROR4 ROL4
[HL + byte] [HL + B] [HL + C]		MOV											
X													MULU
C													DIVUW

Note Except r = A

(2) 16-bit instructions

MOVW, XCHW, ADDW, SUBW, CMPW, PUSH, POP, INCW, DECW

2nd Operand / 1st Operand	#word	AX	rp[Note]	sfrp	saddrp	!addr16	SP	None
AX	ADDW SUBW CMPW		MOVW XCHW	MOVW	MOVW	MOVW	MOVW	
rp	MOVW	MOVW[Note]						INCW, DECW PUSH, POP
sfrp	MOVW	MOVW						
saddrp	MOVW	MOVW						
!addr16		MOVW						
SP	MOVW	MOVW						

Note Only when rp = BC, DE or HL

(3) Bit manipulation instructions

MOV1, AND1, OR1, XOR1, SET1, CLR1, NOT1, BT, BF, BTCLR

2nd Operand / 1st Operand	A.bit	sfr.bit	saddr.bit	PSW.bit	[HL].bit	CY	$addr16	None
A.bit						MOV1	BT BF BTCLR	SET1 CLR1
sfr.bit						MOV1	BT BF BTCLR	SET1 CLR1
saddr.bit						MOV1	BT BF BTCLR	SET1 CLR1
PSW.bit						MOV1	BT BF BTCLR	SET1 CLR1
[HL].bit						MOV1	BT BF BTCLR	SET1 CLR1
CY	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1			SET1 CLR1 NOT1

(4) Call instructions/branch instructions

CALL, CALLF, CALLT, BR, BC, BNC, BZ, BNZ, BT, BF, BTCLR, DBNZ

2nd Operand / 1st Operand	AX	!addr16	!addr11	[addr5]	$addr16
Basic instruction	BR	CALL BR	CALLF	CALLT	BR, BC, BNC BZ, BNZ
Compound instruction					BT, BF BTCLR DBNZ

(5) Other instructions

ADJBA, ADJBS, BRK, RET, RETI, RETB, SEL, NOP, EI, DI, HALT, STOP

12. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbol	Test Conditions			Ratings	Unit
Supply voltage	V_{DD}				–0.3 to +6.5	V
	AV_{DD}				–0.3 to V_{DD} + 0.3 Note	V
	AV_{REF}				–0.3 to V_{DD} + 0.3 Note	V
	AV_{SS}				–0.3 to +0.3	V
Input voltage	V_{I1}	P00 to P03, P10 to P17, P20 to P25, P34 to P36, P40 to P47, P50 to P57, P64 to P67, P70 to P75, X1, X2, XT1, XT2, $\overline{RESET}$			–0.3 to V_{DD} + 0.3 Note	V
	V_{I2}	P30 to P33	N-ch open-drain	Without pull-up resistor	–0.3 to +6.5	V
				With pull-up resistor	–0.3 to V_{DD} + 0.3 Note	V
Output voltage	V_O				–0.3 to V_{DD} + 0.3 Note	V
Analog input voltage	V_{AN}	P10 to P17		Analog input pin	AV_{SS} – 0.3 to AV_{REF} + 0.3 Note and –0.3 to V_{DD} + 0.3 Note	V
Output current, high	I_{OH}	Per pin			–10	mA
		Total for P00 to P03, P40 to P47, P50 to P57, P64 to P67, P70 to P75			–15	mA
		Total for P20 to P25, P30 to P36			–15	mA
Output current, low	I_{OL}	Per pin for P00 to P03, P20 to P25, P34 to P36, P40 to P47, P64 to P67, P70 to P75			20	mA
		Per pin for P30 to P33, P50 to P57			30	mA
		Total for P00 to P03, P40 to P47, P64 to P67, P70 to P75			50	mA
		Total for P20 to P25			20	mA
		Total for P30 to P36			100	mA
		Total for P50 to P57			100	mA
Operating ambient temperature	T_A				–40 to +85	°C
Storage temperature	T_{stg}				–65 to +150	°C

Note 6.5 V or below

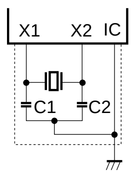
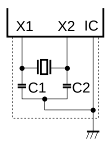
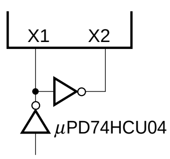
Caution **Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.**

Capacitance (T_A = 25°C, V_{DD} = V_{SS} = 0 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	f = 1 MHz Unmeasured pins returned to 0 V.				15	pF
I/O capacitance	C_{IO}	f = 1 MHz Unmeasured pins returned to 0 V.	P00 to P03, P20 to P25, P34 to P36, P40 to P47, P50 to P57, P64 to P67, P70 to P75			15	pF
			P30 to P33			20	pF

Remark Unless otherwise specified, the characteristics of alternate-function pins are the same as those of port pins.

Main System Clock Oscillator Characteristics (T_A = –40 to 85°C, V_{DD} = 1.8 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Test Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency (f_X)Note 1	V_{DD} = 4.0 to 5.5 V	1.0		8.38	MHz
				1.0		5.0	
		Oscillation stabilization timeNote 2	After V_{DD} reaches oscillation voltage range MIN.			4	ms
Crystal resonator		Oscillation frequency (f_X)Note 1	V_{DD} = 4.0 to 5.5 V	1.0		8.38	MHz
				1.0		5.0	
		Oscillation stabilization timeNote 2	V_{DD} = 4.0 to 5.5 V			10	ms
						30	
External clock		X1 input frequency (f_X)Note 1	V_{DD} = 4.0 to 5.5 V	1.0		8.38	MHz
				1.0		5.0	
		X1 input high-/low-level width (t_{XH}, t_{XL})	V_{DD} = 4.0 to 5.5 V	50		500	ns
				85		500	

Notes 1. Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

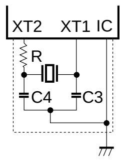
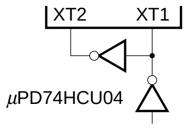
2. Time required to stabilize oscillation after reset or STOP mode release.

Cautions 1. When using the main system clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS1}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. When the main system clock is stopped and the system is operating on the subsystem clock, wait until the oscillation stabilization time has been secured by the program before switching back to the main system clock.

Subsystem Clock Oscillator Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Test Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator		Oscillation frequency (f_{XT})Note 1		32	32.768	35	kHz
		Oscillation stabilization timeNote 2	V_{DD} = 4.0 to 5.5 V		1.2	2	s
						10	
External clock		XT1 input frequency (f_{XT})Note 1		32		38.5	kHz
		XT1 input high-/low-level width (t_{XTH}, t_{XTL})		5		15	μs

Notes 1. Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

2. Time required to stabilize oscillation after V_{DD} reaches oscillation voltage range MIN.

Cautions 1. When using the subsystem clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS1}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. The subsystem clock oscillator is designed as a low-amplitude circuit for reducing current consumption, and is more prone to malfunction due to noise than the main system clock oscillator. Particular care is therefore required with the wiring method when the subsystem clock is used.

Recommended Oscillator Constant

Main system clock: Ceramic resonator (T_A = –40 to +85°C)

Manufacturer	Part Number	Frequency (MHz)	Recommended Circuit Constant		Oscillation Voltage Range	
			C1 (pF)	C2 (pF)	MIN. (V)	MAX. (V)
Murata Mfg. Co., Ltd.	CSB1000J	1.00	100	100	1.8	5.5
	CSA2.00MG040	2.00	100	100	1.8	5.5
	CST2.00MG040	2.00	On-chip	On-chip	1.8	5.5
	CSA3.58MG	3.58	30	30	1.8	5.5
	CST3.58MGW	3.58	On-chip	On-chip	1.8	5.5
	CSA4.19MG	4.19	30	30	1.8	5.5
	CST4.19MGW	4.19	On-chip	On-chip	1.8	5.5
	CSA5.00MG	5.00	30	30	1.8	5.5
	CST5.00MGW	5.00	On-chip	On-chip	1.8	5.5
	CSA8.00MTZ	8.00	30	30	4.0	5.5
	CST8.00MTW	8.00	On-chip	On-chip	4.0	5.5
	CSA8.00MTZ093	8.00	30	30	4.0	5.5
	CST8.00MTW093	8.00	On-chip	On-chip	4.0	5.5
	CSA8.38MTZ	8.38	30	30	4.0	5.5
	CST8.38MTW	8.38	On-chip	On-chip	4.0	5.5
	CSA8.38MTZ093	8.38	30	30	4.0	5.5
	CST8.38MTW093	8.38	On-chip	On-chip	4.0	5.5
TDK	CCR3.58MC3	3.58	On-chip	On-chip	1.8	5.5
	CCR4.19MC3	4.19	On-chip	On-chip	1.8	5.5
	CCR5.0MC3	5.00	On-chip	On-chip	1.8	5.5
	CCR8.0MC5	8.00	On-chip	On-chip	4.0	5.5
	CCR8.38MC5	8.38	On-chip	On-chip	4.0	5.5

Caution The oscillator constant and oscillation voltage range indicate conditions of stable oscillation. Oscillation frequency precision is not guaranteed. For applications requiring oscillation frequency precision, the oscillation frequency must be adjusted on the implementation circuit. For details, please contact directly the manufacturer of the resonator you will use.

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Output current, high	I_{OH}	Per pin				–1	mA
		All pins				–15	mA
Output current, low	I_{OL}	Per pin for P00 to P03, P20 to P25, P34 to P36, P40 to P47, P64 to P67, P70 to P75				10	mA
		Per pin for P30 to P33, P50 to P57				15	mA
		Total for P00 to P03, P40 to P47, P64 to P67, P70 to P75				20	mA
		Total for P20 to P25				10	mA
		Total for P30 to P36				70	mA
		Total for P50 to P57				70	mA
Input voltage, high	V_{IH1}	P10 to P17, P21, P24, P35, P40 to P47, P50 to P57, P64 to P67, P74, P75	V_{DD} = 2.7 to 5.5 V	0.7V_{DD}		V_{DD}	V
				0.8V_{DD}		V_{DD}	V
	V_{IH2}	P00 to P03, P20, P22, P23, P25, P34, P36, P70 to P73, $\overline{\text{RESET}}$	V_{DD} = 2.7 to 5.5 V	0.8V_{DD}		V_{DD}	V
				0.85V_{DD}		V_{DD}	V
	V_{IH3}	P30 to P33 (N-ch open-drain)	V_{DD} = 2.7 to 5.5 V	0.7V_{DD}		5.5	V
				0.8V_{DD}		5.5	V
	V_{IH4}	X1, X2	V_{DD} = 2.7 to 5.5 V	V_{DD} – 0.5		V_{DD}	V
				V_{DD} – 0.2		V_{DD}	V
	V_{IH5}	XT1, XT2	V_{DD} = 4.0 to 5.5 V	0.8V_{DD}		V_{DD}	V
				0.9V_{DD}		V_{DD}	V
Input voltage, low	V_{IL1}	P10 to P17, P21, P24, P35, P40 to P47, P50 to P57, P64 to P67, P74, P75	V_{DD} = 2.7 to 5.5 V	0		0.3V_{DD}	V
				0		0.2V_{DD}	V
	V_{IL2}	P00 to P03, P20, P22, P23, P25, P34, P36, P70 to P73, $\overline{\text{RESET}}$	V_{DD} = 2.7 to 5.5 V	0		0.2V_{DD}	V
				0		0.15V_{DD}	V
	V_{IL3}	P30 to P33	4.0 V ≤ V_{DD} ≤ 5.5 V	0		0.3V_{DD}	V
			2.7 V ≤ V_{DD} < 4.0 V	0		0.2V_{DD}	V
			1.8 V ≤ V_{DD} < 2.7 V	0		0.1V_{DD}	V
	V_{IL4}	X1, X2	V_{DD} = 2.7 to 5.5 V	0		0.4	V
				0		0.2	V
	V_{IL5}	XT1, XT2	V_{DD} = 4.0 to 5.5 V	0		0.2V_{DD}	V
				0		0.1V_{DD}	V
Output voltage, high	V_{OH1}	V_{DD} = 4.0 to 5.5 V, I_{OH} = –1 mA		V_{DD} – 1.0		V_{DD}	V
		I_{OH} = –100 μA		V_{DD} – 0.5		V_{DD}	V
Output voltage, low	V_{OL1}	P30 to P33	V_{DD} = 4.0 to 5.5 V, I_{OL} = 15 mA			2.0	V
		P50 to P57			0.4	2.0	V
		P00 to P03, P20 to P25, P34 to P36, P40 to P47, P64 to P67, P70 to P75	V_{DD} = 4.0 to 5.5 V, I_{OL} = 1.6 mA			0.4	V
	V_{OL2}	I_{OL} = 400 μA				0.5	V

Remark Unless otherwise specified, the characteristics of alternate-function pins are the same as those of port pins.

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Input leakage current, high	I_{LIH1}	$V_{IN} = V_{DD}$	P00 to P03, P10 to P17, P20 to P25, P34 to P36, P40 to P47, P50 to P57, P64 to P67, P70 to P75, $\overline{RESET}$			3	μA
	I_{LIH2}		X1, X2, XT1, XT2			20	μA
	I_{LIH3}	V_{IN} = 5.5 V	P30 to P33 Note			3	μA
Input leakage current, low	I_{LIL1}	V_{IN} = 0 V	P00 to P03, P10 to P17, P20 to P25, P34 to P36, P40 to P47, P50 to P57, P64 to P67, P70 to P75, $\overline{RESET}$			–3	μA
	I_{LIL2}		X1, X2, XT1, XT2			–20	μA
	I_{LIL3}		P30 to P33 Note			–3	μA
Output leakage current, high	I_{LOH}	$V_{OUT} = V_{DD}$				3	μA
Output leakage current, low	I_{LOL}	V_{OUT} = 0 V				–3	μA
Mask option pull-up resistance	R_1	V_{IN} = 0 V, P30, P31		15	30	90	kΩ
Software pull-up resistance	R_2	V_{IN} = 0 V, P00 to P03, P20 to P25, P34 to P36, P40 to P47, P50 to P57, P64 to P67, P70 to P75		15	30	90	kΩ

Note When pull-up resistors are not connected to P30, P31 (specified by the mask option).

Remark Unless otherwise specified, the characteristics of alternate-function pins are the same as those of port pins.

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Test Conditions			MIN.	TYP.	MAX.	Unit
Power supply current Note 1	I_{DD1}	8.38-MHz crystal oscillation operating mode	V_{DD} = 5.0V±10% Note 2	When A/D converter is stopped		5.5	11	mA
				When A/D converter is operating		6.5	13	mA
		5.00-MHz crystal oscillation operating mode	V_{DD} = 3.0V±10% Note 2	When A/D converter is stopped		2	4	mA
				When A/D converter is operating		3	6	mA
			V_{DD} = 2.0V±10% Note 3	When A/D converter is stopped		0.4	1.5	mA
				When A/D converter is operating		1.4	4.2	mA
	I_{DD2}	8.38-MHz crystal oscillation HALT mode	V_{DD} = 5.0V±10% Note 2	When peripheral functions are stopped		1.1	2.2	mA
				When peripheral functions are operating			4.7	mA
		5.00-MHz crystal oscillation HALT mode	V_{DD} = 3.0V±10% Note 2	When peripheral functions are stopped		0.35	0.7	mA
				When peripheral functions are operating			1.7	mA
			V_{DD} = 2.0V±10% Note 3	When peripheral functions are stopped		0.15	0.4	mA
				When peripheral functions are operating			1.1	mA
	I_{DD3}	32.768-kHz crystal oscillation operating mode Note 4		V_{DD} = 5.0 V ±10%		40	80	μA
				V_{DD} = 3.0 V ±10%		20	40	μA
				V_{DD} = 2.0 V ±10%		10	20	μA
	I_{DD4}	32.768-kHz crystal oscillation HALT mode Note 4		V_{DD} = 5.0 V ±10%		30	60	μA
				V_{DD} = 3.0 V ±10%		6	18	μA
				V_{DD} = 2.0 V ±10%		2	10	μA
	I_{DD5}	XT1 = 0V STOP mode When feedback resistor is not used		V_{DD} = 5.0 V ±10%		0.1	30	μA
				V_{DD} = 3.0 V ±10%		0.05	10	μA
				V_{DD} = 2.0 V ±10%		0.05	10	μA

Notes 1. Total current through the internal power supply (V_{DD0}, V_{DD1}), including the peripheral operation current (except the current through pull-up resistors of ports and the AV_{REF} pin).

2. When the processor clock control register (PCC) is set to 00H.

3. When PCC is set to 02H.

4. When main system clock operation is stopped.

AC Characteristics

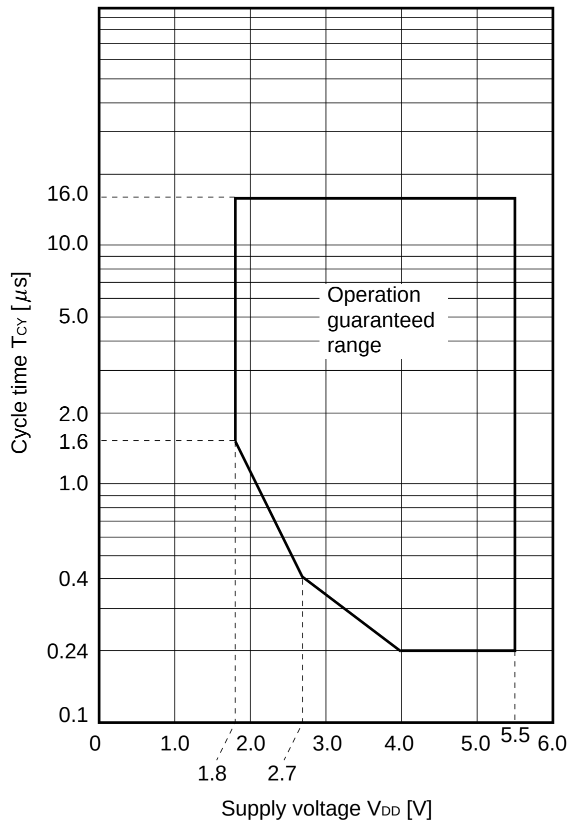
(1) Basic Operation (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Cycle time (Min. instruction execution time)	T_{CY}	Operating with main system clock	4.0 V ≤ V_{DD} ≤ 5.5 V	0.24		16	μs
			2.7 V ≤ V_{DD} < 4.0 V	0.4		16	μs
				1.6		16	μs
		Operating with subsystem clock		103.9 Note 1	122	125	μs
TI00, TI01 input high-/low-level width	t_{TIH0}, t_{TIL0}	4.0 V ≤ V_{DD} ≤ 5.5 V		$2/f_{sam}$ + 0.1 Note 2			μs
		2.7 V ≤ V_{DD} < 4.0 V		$2/f_{sam}$ + 0.2 Note 2			μs
				$2/f_{sam}$ + 0.5 Note 2			μs
TI50, TI51 input frequency	f_{TI5}	V_{DD} = 2.7 to 5.5 V		0		4	MHz
				0		275	kHz
TI50, TI51 input high-/low-level width	t_{TIH5}, t_{TIL5}	V_{DD} = 2.7 to 5.5 V		100			ns
				1.8			ns
Interrupt request input high-/low -level width	t_{INTH}, t_{INTL}	INTP0 to INTP3, P40 to P47	V_{DD} = 2.7 to 5.5 V	1			μs
				2			μs
$\overline{\text{RESET}}$ low-level width	t_{RSL}	V_{DD} = 2.7 to 5.5 V		10			μs
				20			μs

Notes 1. Value when an external clock is used. When a crystal resonator is used, it is 114 μs (MIN.).

2. Selection of f_{sam} = f_X, $f_X/4$, $f_X/64$ is possible using bits 0 and 1 (PRM00, PRM01) of prescaler mode register 0 (PRM0). However, if the TI00 valid edge is selected as the count clock, the value becomes f_{sam} = $f_X/8$.

T_{CY} vs. V_{DD} (main system clock operation)



(2) Read/Write Operation (T_A = –40 to + 85°C, V_{DD} = 4.0 to 5.5 V)

(1/3)

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
ASTB high-level width	t_{ASTH}		$0.3t_{CY}$		ns
Address setup time	t_{ADS}		20		ns
Address hold time	t_{ADH}		6		ns
Data input time from address	t_{ADD1}			$(2 + 2n)t_{CY} – 54$	ns
	t_{ADD2}			$(3 + 2n)t_{CY} – 60$	ns
Address output time from $\overline{\text{RD}}$↓	t_{RDAD}		0	100	ns
Data input time from $\overline{\text{RD}}$↓	t_{RDD1}			$(2 + 2n)t_{CY} – 87$	ns
	t_{RDD2}			$(3 + 2n)t_{CY} – 93$	ns
Read data hold time	t_{RDH}		0		ns
$\overline{\text{RD}}$ low-level width	t_{RDL1}		$(1.5 + 2n)t_{CY} – 33$		ns
	t_{RDL2}		$(2.5 + 2n)t_{CY} – 33$		ns
$\overline{\text{WAIT}}$↓ input time from $\overline{\text{RD}}$↓	t_{RDWT1}			$t_{CY} – 43$	ns
	t_{RDWT2}			$t_{CY} – 43$	ns
$\overline{\text{WAIT}}$↓ input time from $\overline{\text{WR}}$↓	t_{WRWT}			$t_{CY} – 25$	ns
$\overline{\text{WAIT}}$ low-level width	t_{WTL}		$(0.5 + n)t_{CY} + 10$	$(2 + 2n)t_{CY}$	ns
Write data setup time	t_{WDS}		60		ns
Write data hold time	t_{WDH}		6		ns
$\overline{\text{WR}}$ low-level width	t_{WRL1}		$(1.5 + 2n)t_{CY} – 15$		ns
$\overline{\text{RD}}$↓ delay time from ASTB↓	t_{ASTRD}		6		ns
$\overline{\text{WR}}$↓ delay time from ASTB↓	t_{ASTWR}		$2t_{CY} – 15$		ns
ASTB↑ delay time from $\overline{\text{RD}}$↑ at external fetch	t_{RDAST}		$0.8t_{CY} – 15$	$1.2t_{CY}$	ns
Address hold time from $\overline{\text{RD}}$↑ at external fetch	t_{RDADH}		$0.8t_{CY} – 15$	$1.2t_{CY} + 30$	ns
Write data output time from $\overline{\text{RD}}$↑	t_{RDWD}		40		ns
Write data output time from $\overline{\text{WR}}$↓	t_{WRWD}		10	60	ns
Address hold time from $\overline{\text{WR}}$↑	t_{WRADH}		$0.8t_{CY} – 15$	$1.2t_{CY} + 30$	ns
$\overline{\text{RD}}$↑ delay time from $\overline{\text{WAIT}}$↑	t_{WTRD}		$0.8t_{CY}$	$2.5t_{CY} + 25$	ns
$\overline{\text{WR}}$↑ delay time from $\overline{\text{WAIT}}$↑	t_{WTWR}		$0.8t_{CY}$	$2.5t_{CY} + 25$	ns

Remarks **1.** $t_{CY} = T_{CY}/4$

2. n indicates the number of waits.

3. C_L = 100 pF (C_L indicates the load capacitance of the AD0 to AD7, A8 to A15, $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{WAIT}}$, and ASTB pins.)

(2) Read/Write Operation (T_A = –40 to + 85°C, V_{DD} = 2.7 to 4.0 V)

(2/3)

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
ASTB high-level width	t_{ASTH}		0.3t_{CY}		ns
Address setup time	t_{ADS}		30		ns
Address hold time	t_{ADH}		10		ns
Data input time from address	t_{ADD1}			(2 + 2n)t_{CY} – 108	ns
	t_{ADD2}			(3 + 2n)t_{CY} – 120	ns
Address output time from $\overline{RD}$↓	t_{RDAD}		0	200	ns
Data input time from $\overline{RD}$↓	t_{RDD1}			(2 + 2n)t_{CY} – 148	ns
	t_{RDD2}			(3 + 2n)t_{CY} – 162	ns
Read data hold time	t_{RDH}		0		ns
$\overline{RD}$ low-level width	t_{RDL1}		(1.5 + 2n)t_{CY} – 40		ns
	t_{RDL2}		(2.5 + 2n)t_{CY} – 40		ns
$\overline{WAIT}$↓ input time from $\overline{RD}$↓	t_{RDWT1}			t_{CY} – 75	ns
	t_{RDWT2}			t_{CY} – 60	ns
$\overline{WAIT}$↓ input time from $\overline{WR}$↓	t_{WRWT}			t_{CY} – 50	ns
$\overline{WAIT}$ low-level width	t_{WTL}		(0.5 + 2n)t_{CY} + 10	(2 + 2n)t_{CY}	ns
Write data setup time	t_{WDS}		60		ns
Write data hold time	t_{WDH}		10		ns
$\overline{WR}$ low-level width	t_{WRL1}		(1.5 + 2n)t_{CY} – 30		ns
$\overline{RD}$↓ delay time from ASTB↓	t_{ASTRD}		10		ns
$\overline{WR}$↓ delay time from ASTB↓	t_{ASTWR}		2t_{CY} – 30		ns
ASTB↑ delay time from $\overline{RD}$↑ at external fetch	t_{RDAST}		0.8t_{CY} – 30	1.2t_{CY}	ns
Address hold time from $\overline{RD}$↑ at external fetch	t_{RDADH}		0.8t_{CY} – 30	1.2t_{CY} + 60	ns
Write data output time from $\overline{RD}$↑	t_{RDWD}		40		ns
Write data output time from $\overline{WR}$↓	t_{WRWD}		20	120	ns
Address hold time from $\overline{WR}$↑	t_{WRADH}		0.8t_{CY} – 30	1.2t_{CY} + 60	ns
$\overline{RD}$↑ delay time from $\overline{WAIT}$↑	t_{WTRD}		0.5t_{CY}	2.5t_{CY} + 50	ns
$\overline{WR}$↑ delay time from $\overline{WAIT}$↑	t_{WTWR}		0.5t_{CY}	2.5t_{CY} + 50	ns

Remarks **1.** t_{CY} = T_{CY}/4

2. n indicates the number of waits.

3. C_L = 100 pF (C_L indicates the load capacitance of the AD0 to AD7, AD8 to AD15, $\overline{RD}$, $\overline{WR}$, $\overline{WAIT}$, and ASTB pins.)

(2) Read/Write Operation (T_A = –40 to + 85°C, V_{DD} = 1.8 to 2.7 V)

(3/3)

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
ASTB high-level width	t_{ASTH}		$0.3t_{CY}$		ns
Address setup time	t_{ADS}		120		ns
Address hold time	t_{ADH}		20		ns
Data input time from address	t_{ADD1}			$(2 + 2n)t_{CY}$ – 233	ns
	t_{ADD2}			$(3 + 2n)t_{CY}$ – 240	ns
Address output time from $\overline{RD}$↓	t_{RDAD}		0	400	ns
Data input time from $\overline{RD}$↓	t_{RDD1}			$(2 + 2n)t_{CY}$ – 325	ns
	t_{RDD2}			$(3 + 2n)t_{CY}$ – 332	ns
Read data hold time	t_{RDH}		0		ns
$\overline{RD}$ low-level width	t_{RDL1}		$(1.5 + 2n)t_{CY}$ – 92		ns
	t_{RDL2}		$(2.5 + 2n)t_{CY}$ – 92		ns
$\overline{WAIT}$↓ input time from $\overline{RD}$↓	t_{RDWT1}			t_{CY} – 350	ns
	t_{RDWT2}			t_{CY} – 132	ns
$\overline{WAIT}$↓ input time from $\overline{WR}$↓	t_{WRWT}			t_{CY} – 100	ns
$\overline{WAIT}$ low-level width	t_{WTL}		$(0.5 + 2n)t_{CY}$ + 10	$(2 + 2n)t_{CY}$	ns
Write data setup time	t_{WDS}		60		ns
Write data hold time	t_{WDH}		20		ns
$\overline{WR}$ low-level width	t_{WRL1}		$(1.5 + 2n)t_{CY}$ – 60		ns
$\overline{RD}$↓ delay time from ASTB↓	t_{ASTRD}		20		ns
$\overline{WR}$↓ delay time from ASTB↓	t_{ASTWR}		$2t_{CY}$ – 60		ns
ASTB↑ delay time from $\overline{RD}$↑ at external fetch	t_{RDAST}		$0.8t_{CY}$ – 60	$1.2t_{CY}$	ns
Address hold time from $\overline{RD}$↑ at external fetch	t_{RDADH}		$0.8t_{CY}$ – 60	$1.2t_{CY}$ + 120	ns
Write data output time from $\overline{RD}$↑	t_{RDWD}		40		ns
Write data output time from $\overline{WR}$↓	t_{WRWD}		40	240	ns
Address hold time from $\overline{WR}$↑	t_{WRADH}		$0.8t_{CY}$ – 60	$1.2t_{CY}$ + 120	ns
$\overline{RD}$↑ delay time from $\overline{WAIT}$↑	t_{WTRD}		$0.5t_{CY}$	$2.5t_{CY}$ + 100	ns
$\overline{WR}$↑ delay time from $\overline{WAIT}$↑	t_{WTWR}		$0.5t_{CY}$	$2.5t_{CY}$ + 100	ns

Remarks **1.** $t_{CY} = T_{CY}/4$

2. n indicates the number of waits.

3. C_L = 100pF (C_L indicates the load capacitance of the AD0 to AD7, AD8 to AD15, $\overline{RD}$, $\overline{WR}$, $\overline{WAIT}$, and ASTB pins.)

(3) Serial Interface (T_A = –40 to + 85°C, V_{DD} = 1.8 to 5.5 V)

(a) 3-wire serial I/O mode ($\overline{SCK30}$ ... Internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK30}$ cycle time	t_{KCY1}	4.0 V ≤ V_{DD} ≤ 5.5 V	954			ns
		2.7 V ≤ V_{DD} < 4.0 V	1600			ns
			3200			ns
$\overline{SCK30}$ high-/low-level width	t_{KH1}, t_{KL1}	V_{DD} = 4.0 to 5.5 V	t_{KCY1}/2 – 50			ns
			t_{KCY1}/2 – 100			ns
SI30 setup time (to $\overline{SCK30}$↑)	t_{SIK1}	4.0 V ≤ V_{DD} ≤ 5.5V	100			ns
		2.7 V ≤ V_{DD} < 4.0V	150			ns
			300			ns
SI30 hold time (from $\overline{SCK30}$↑)	t_{KSI1}		400			ns
SO30 output delay time from $\overline{SCK30}$↓	t_{KSO1}	C = 100 pF**Note**			300	ns

Note C is the load capacitance of the $\overline{SCK30}$ and SO30 output lines.

(b) 3-wire serial I/O mode ($\overline{SCK30}$ ... External clock input)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK30}$ cycle time	t_{KCY2}	4.0 V ≤ V_{DD} ≤ 5.5 V	800			ns
		2.7 V ≤ V_{DD} < 4.0 V	1600			ns
			3200			ns
$\overline{SCK30}$ high-/low-level width	t_{KH2}, t_{KL2}	4.0 V ≤ V_{DD} ≤ 5.5 V	400			ns
		2.7 V ≤ V_{DD} < 4.0 V	800			ns
			1600			ns
SI30 setup time (to $\overline{SCK30}$↑)	t_{SIK2}		100			ns
SI30 hold time (from $\overline{SCK30}$↑)	t_{KSI2}		400			ns
SO30 output delay time from $\overline{SCK30}$↓	t_{KSO2}	C = 100 pF**Note**			300	ns

Note C is the load capacitance of the SO30 output line.

(c) UART mode (Dedicated baud-rate generator output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		4.0 V ≤ V_{DD} ≤ 5.5 V			131031	bps
		2.7 V ≤ V_{DD} < 4.0 V			78125	bps
					39063	bps

(d) UART mode (External clock input)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
ASCK0 cycle time	t_{KCY3}	4.0 V ≤ V_{DD} ≤ 5.5 V	800			ns
		2.7 V ≤ V_{DD} < 4.0 V	1600			ns
			3200			ns
ASCK0 high-/low-level width	t_{KH3}, t_{KL3}	4.0 V ≤ V_{DD} ≤ 5.5 V	400			ns
		2.7 V ≤ V_{DD} < 4.0 V	800			ns
			1600			ns
Transfer rate		4.0 V ≤ V_{DD} ≤ 5.5 V			39063	bps
		2.7 V ≤ V_{DD} < 4.0 V			19531	bps
					9766	bps

(e) UART mode (Infrared ray data transfer mode)

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
Transfer rate		V_{DD} = 4.0 to 5.5 V		131031	bps
Bit rate allowable error		V_{DD} = 4.0 to 5.5 V		±0.87	%
Output pulse width		V_{DD} = 4.0 to 5.5 V	1.2	0.24/fbr**Note**	μs
Input pulse width		V_{DD} = 4.0 to 5.5 V	4/f_X		μs

Note fbr: Specified baud rate

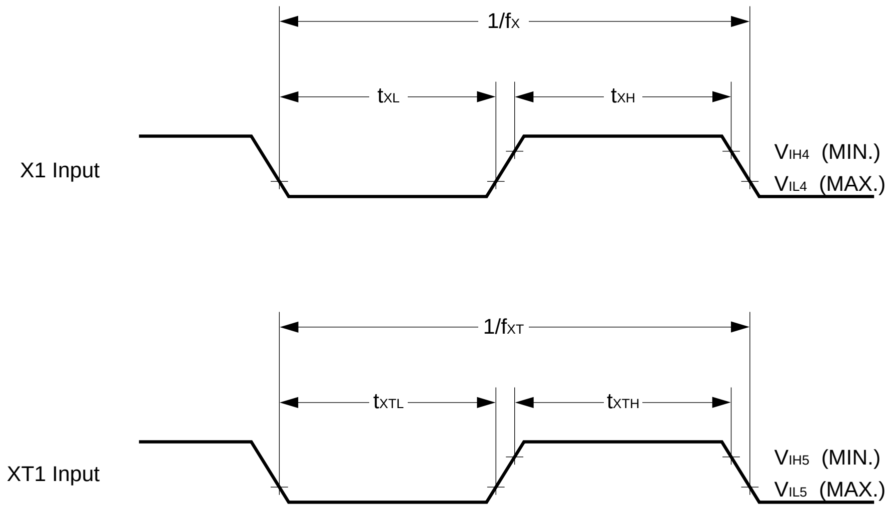
(f) I²C bus Mode

Parameter		Symbol	Standard Mode		High-Speed Mode		Unit
			MIN.	MAX.	MIN.	MAX.	
SCL0 clock frequency		f_{CLK}	0	100	0	400	kHz
Bus-free time (between stop and start condition)		t_{BUF}	4.7	—	1.3	—	μs
Hold time Note 1		$t_{HD:STA}$	4.0	—	0.6	—	μs
SCL0 clock low-level width		t_{LOW}	4.7	—	1.3	—	μs
SCL0 clock high-level width		t_{HIGH}	4.0	—	0.6	—	μs
Start/restart condition setup time		$t_{SU:STA}$	4.7	—	0.6	—	μs
Data hold time	CBUS compatible master	$t_{HD:DAT}$	5.0	—	—	—	μs
	I²C bus		0 Note 2	—	0 Note 2	0.9 Note 3	μs
Data setup time		$t_{SU:DAT}$	250	—	100 Note 4	—	ns
SDA0 and SCL0 signal rise time		t_R	—	1000	20 + 0.1Cb Note 5	300	ns
SDA0 and SCL0 signal fall time		t_F	—	300	20 + 0.1Cb Note 5	300	ns
Stop condition setup time		$t_{SU:STO}$	4.0	—	0.6	—	μs
Spike pulse width controlled by input filter		t_{SP}	—	—	0	50	ns
Capacitive load per bus line		Cb	—	400	—	400	pF

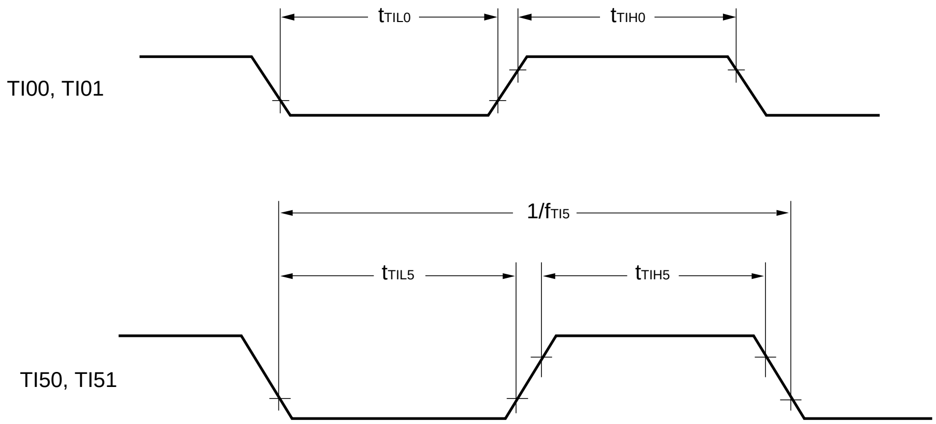
Notes
1. In the start condition, the first clock pulse is generated after this hold time.
2. To fill in the undefined area of the SCL0 falling edge, it is necessary for the device to internally provide at least 300 ns of hold time for the SDA0 signal (which is $V_{IHmin.}$ of the SCL0 signal).
3. If the device does not extend the SCL0 signal low hold time (t_{LOW}), only maximum data hold time $t_{HD:DAT}$ needs to be fulfilled.
4. The high-speed mode I²C bus is available in a standard mode I²C bus system. At this time, the conditions described below must be satisfied.
   - If the device does not extend the SCL0 signal low state hold time
     $t_{SU:DAT} \geq 250$ ns
   - If the device extends the SCL0 signal low state hold time
     Be sure to transmit the next data bit to the SDA0 line before the SCL0 line is released ($t_{Rmax.} + t_{SU:DAT}$ = 1000 + 250 = 1250 ns by standard mode I²C bus specification).
5. Cb: Total capacitance per bus line (unit: pF)

AC Timing Test Points (Excluding X1, XT1 Inputs)

Clock Timing

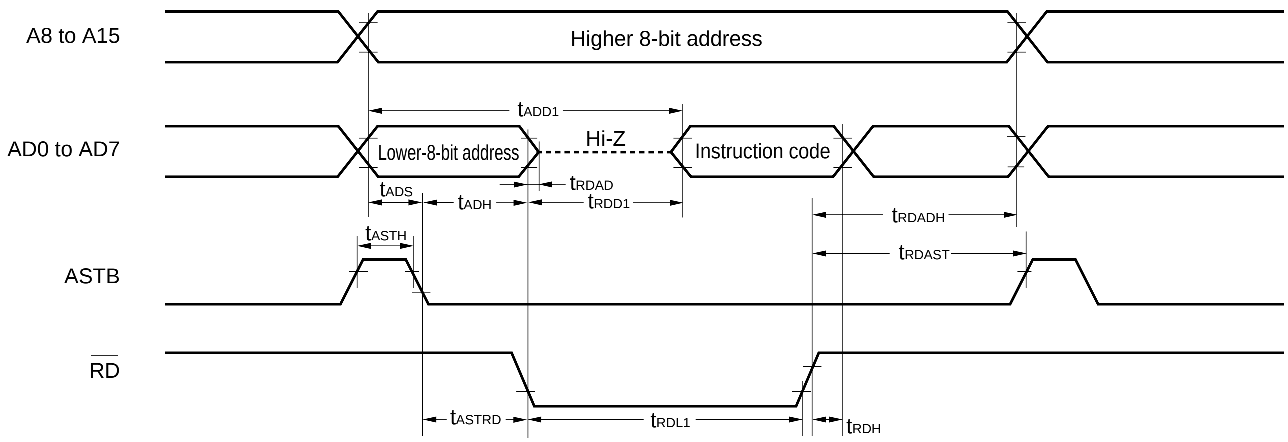


TI Timing

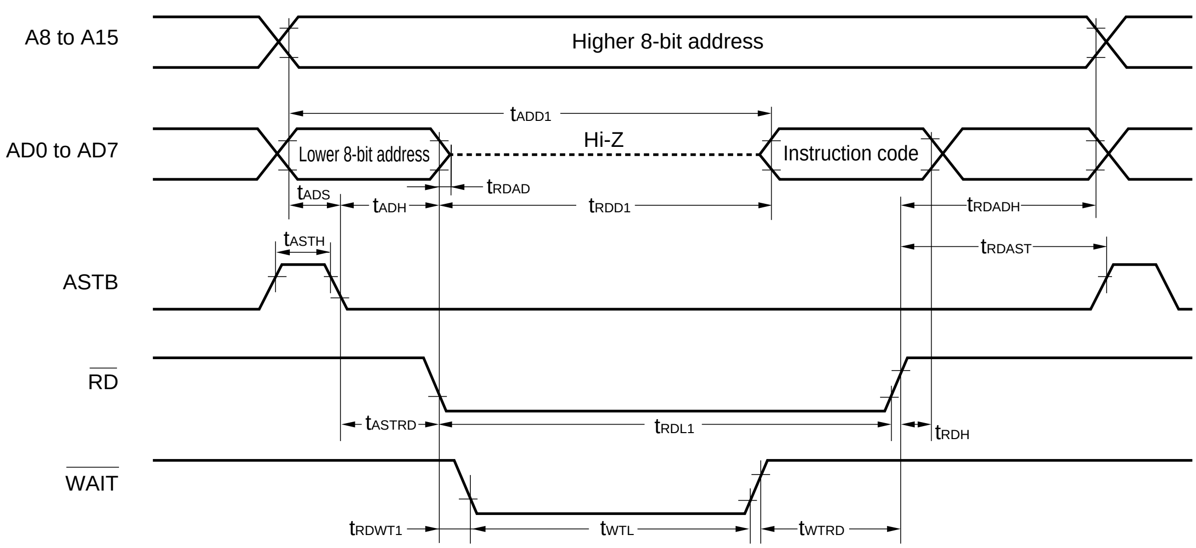


Read/Write Operation

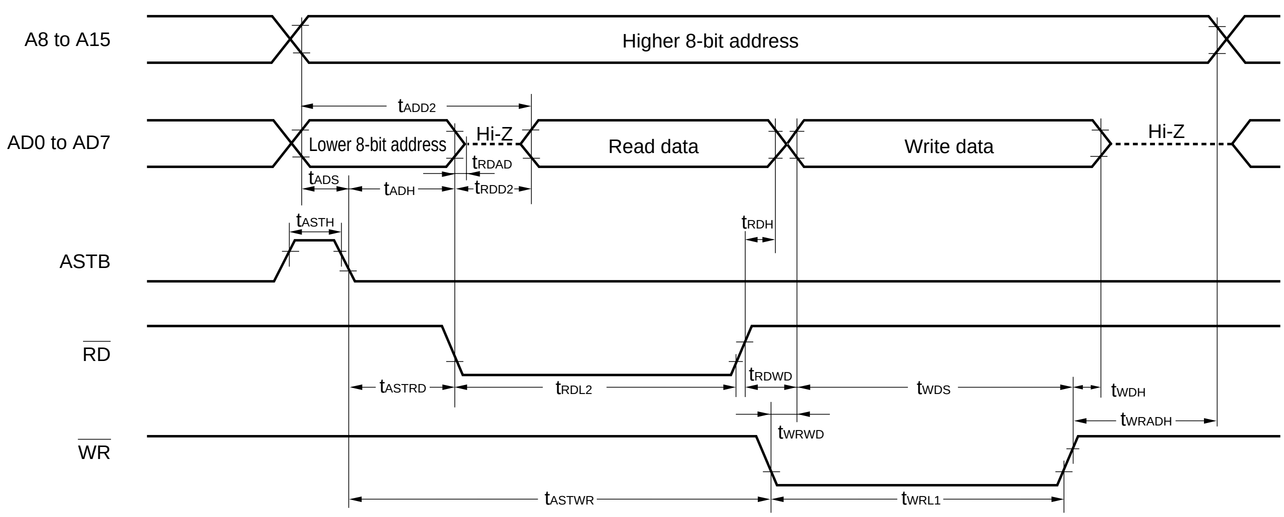
External fetch (no wait):



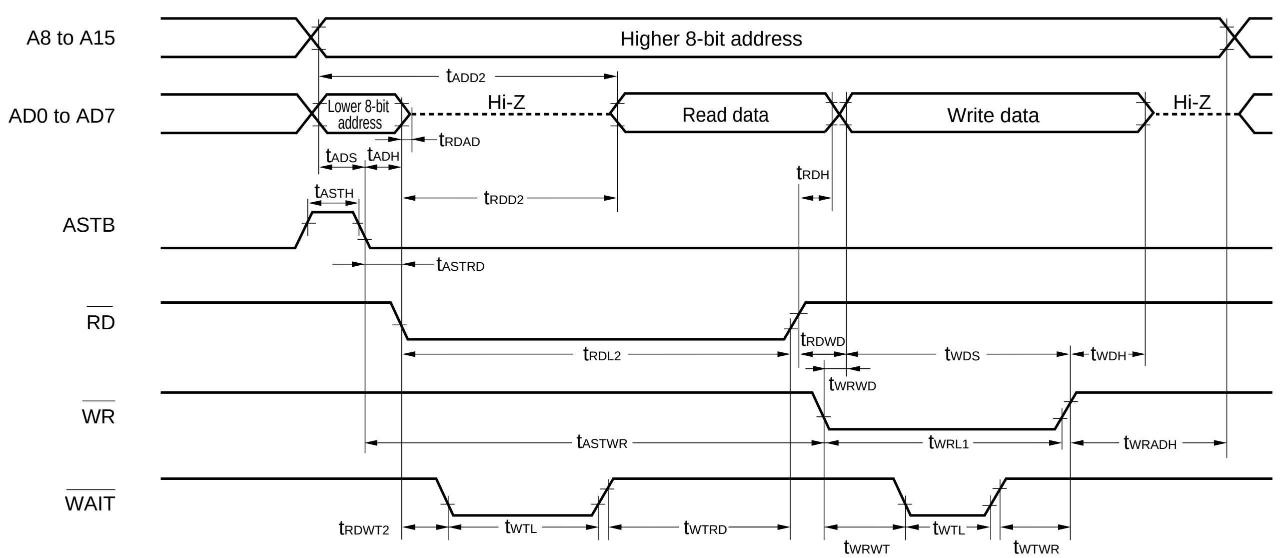
External fetch (wait insertion):



External data access (no wait):

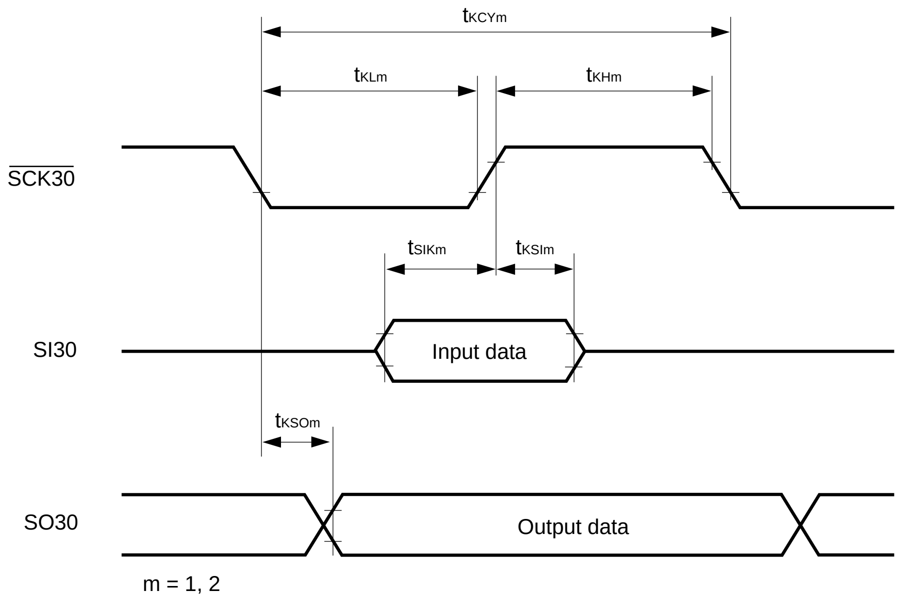


External data access (wait insertion):

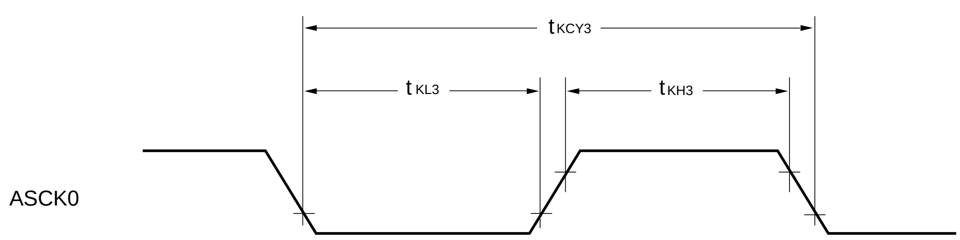


Serial Transfer Timing

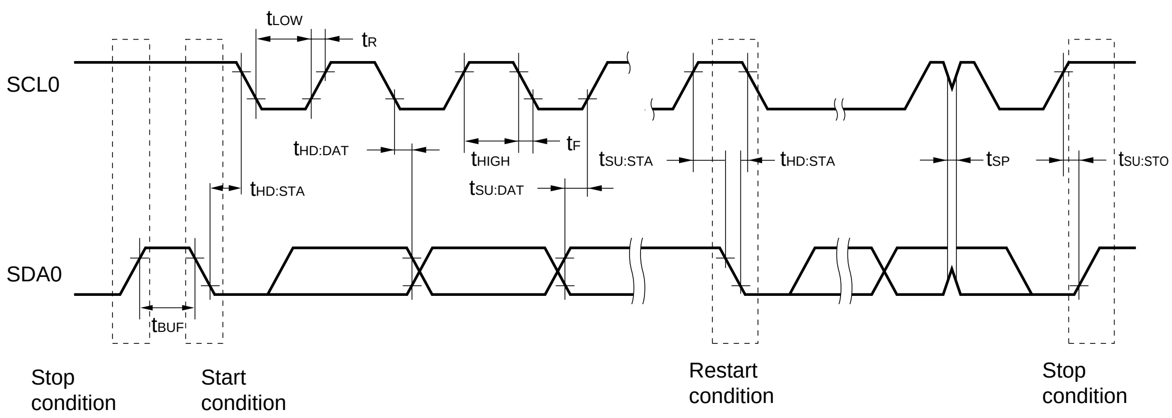
3-wire serial I/O mode:



UART mode (external clock input):



I²C Bus Mode:


tLOW
tR
SCL0
tHD:DAT
tHIGH
tF
tSU:STA
tHD:STA
tSP
tSU:STO
tHD:STA
tSU:DAT
SDA0
tBUF
Stop condition
Start condition
Restart condition
Stop condition

A/D Converter Characteristics (T_A = –40 to +85°C, V_{DD} = AV_{DD} = AV_{REF} = 1.8 to 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution			10	10	10	bit
Overall error[Notes 1, 2]		4.0 V ≤ AV_{REF} ≤ 5.5 V		±0.2	±0.4	%FSR
		2.7 V ≤ AV_{REF} < 4.0 V		±0.3	±0.6	%FSR
		1.8 V ≤ AV_{REF} < 2.7 V		±0.6	±1.2	%FSR
Conversion time	t_{CONV}	4.0 V ≤ AV_{REF} ≤ 5.5 V	14		96	μs
		2.7 V ≤ AV_{REF} < 4.0 V	19		96	μs
		1.8 V ≤ AV_{REF} < 2.7 V	28		96	μs
Zero-scale offset[Notes 1, 2]		4.0 V ≤ AV_{REF} ≤ 5.5 V			±0.4	%FSR
		2.7 V ≤ AV_{REF} < 4.0 V			±0.6	%FSR
		1.8 V ≤ AV_{REF} < 2.7 V			±1.2	%FSR
Full-scale offset[Notes 1, 2]		4.0 V ≤ AV_{REF} ≤ 5.5 V			±0.4	%FSR
		2.7 V ≤ AV_{REF} < 4.0 V			±0.6	%FSR
		1.8 V ≤ AV_{REF} < 2.7 V			±1.2	%FSR
Integral linearity error[Note 1]		4.0 V ≤ AV_{REF} ≤ 5.5 V			±2.5	LSB
		2.7 V ≤ AV_{REF} < 4.0 V			±4.5	LSB
		1.8 V ≤ AV_{REF} < 2.7 V			±8.5	LSB
Differential linearity error[Note 1]		4.0 V ≤ AV_{REF} ≤ 5.5 V			±1.5	LSB
		2.7 V ≤ AV_{REF} < 4.0 V			±2.0	LSB
		1.8 V ≤ AV_{REF} < 2.7 V			±3.5	LSB
Analog input voltage	V_{IAN}		0		AV_{REF}	V
Reference voltage	AV_{REF}		1.8		AV_{DD}	V
Resistance between AV_{REF} and AV_{SS}	R_{REF}	When A/D conversion is not performed	20	40		kΩ

Notes 1. Excludes quantization error (±1/2 LSB).

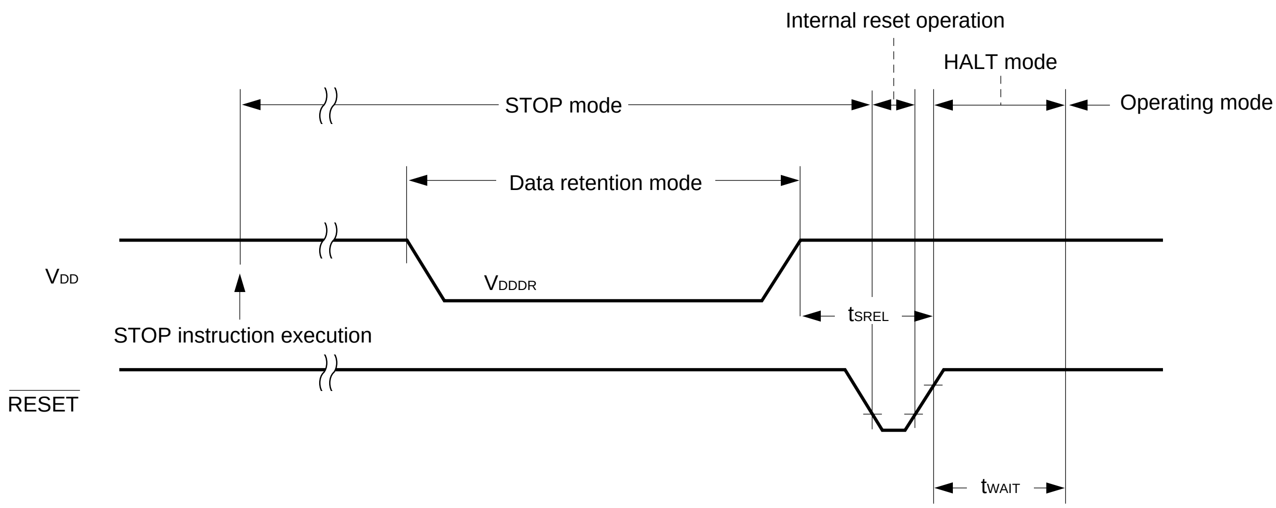
2. Shown as a percentage of the full scale value.

Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics (T_A = –40 to +85°C)

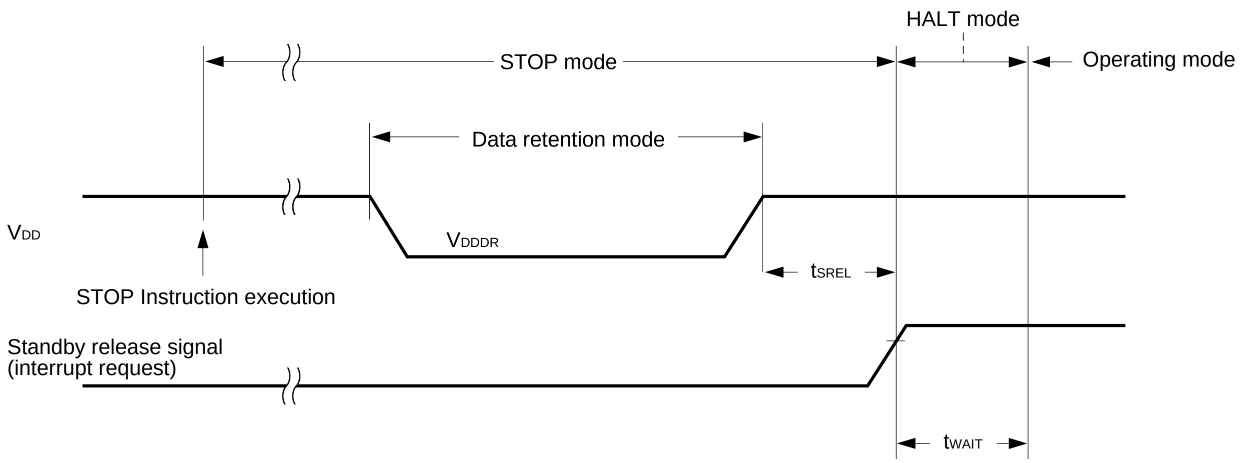
Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Data retention power supply voltage	V_{DDDR}		1.6		5.5	V
Data retention power supply current	I_{DDDR}	V_{DDDR} = 1.6 V Subsystem clock stop (XT1 = V_{DD}) and feed-back resistor disconnected		0.1	30	μA
Release signal set time	t_{SREL}		0			μs
Oscillation stabilization time	t_{WAIT}	Release by $\overline{RESET}$		$2^{17}/f_X$		ms
		Release by interrupt request		**Note**		ms

Note Selection of $2^{12}/f_X$ and $2^{14}/f_X$ to $2^{17}/f_X$ is possible using bits 0 to 2 (OSTS0 to OSTS2) of the oscillation stabilization time select register (OSTS).

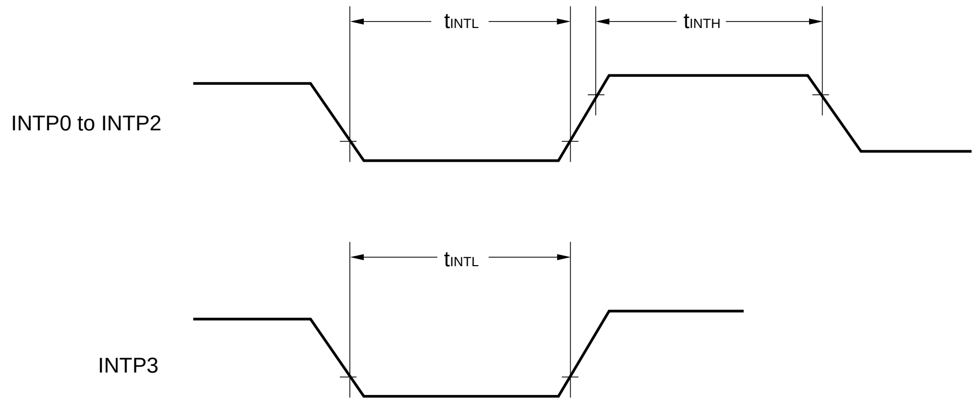
Data Retention Timing (STOP mode release by $\overline{RESET}$)



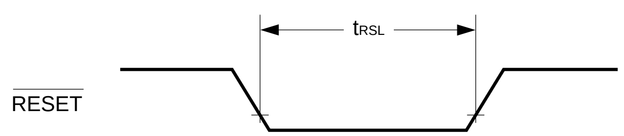
Data Retention Timing (Standby release signal: STOP mode release by interrupt request signal)



Interrupt Request Input Timing

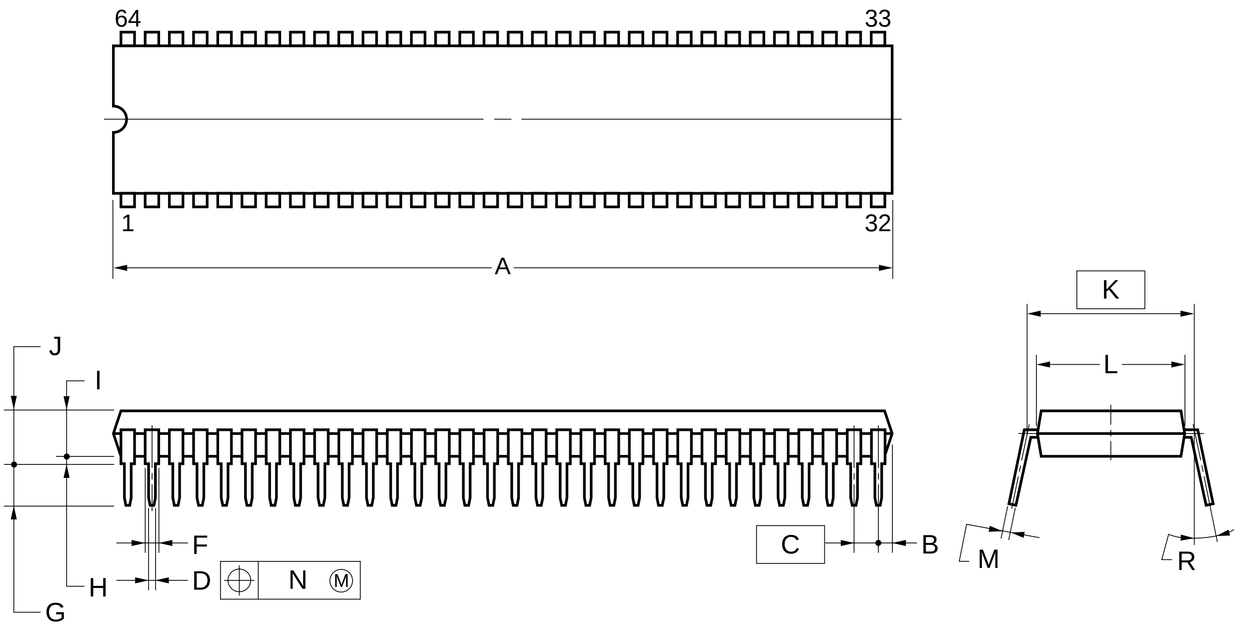


$\overline{\text{RESET}}$ Input Timing



13. PACKAGE DRAWINGS

64 PIN PLASTIC SHRINK DIP (750 mil)



NOTES

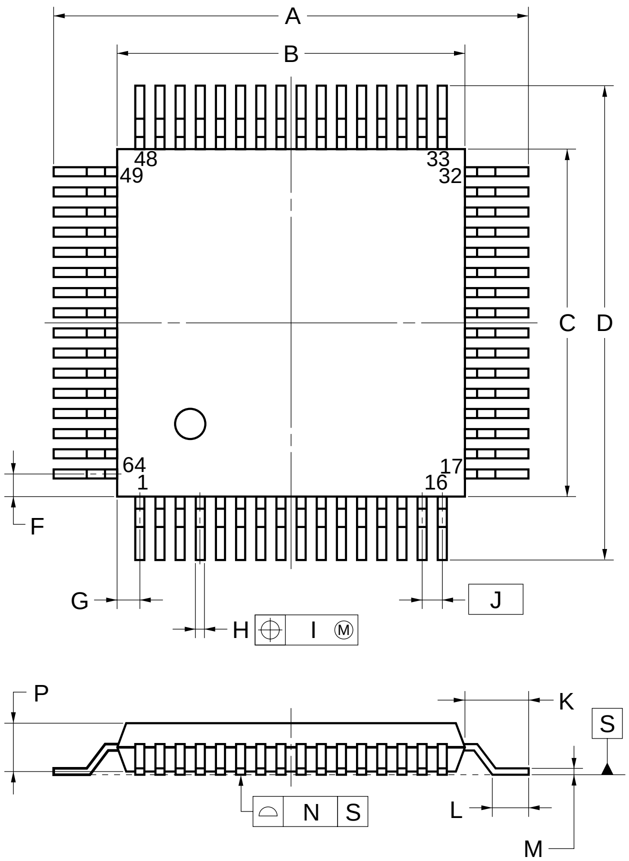
1. Controlling dimension—— millimeter.
2. Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.
3. Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	$58.0^{+0.68}_{-0.20}$	$2.283^{+0.028}_{-0.008}$
B	1.78 MAX.	0.070 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	0.50±0.10	$0.020^{+0.004}_{-0.005}$
F	0.9 MIN.	0.035 MIN.
G	3.2±0.3	0.126±0.012
H	0.51 MIN.	0.020 MIN.
I	$4.05^{+0.26}_{-0.20}$	$0.159^{+0.011}_{-0.008}$
J	5.08 MAX.	0.200 MAX.
K	19.05 (T.P.)	0.750 (T.P.)
L	17.0±0.2	$0.669^{+0.009}_{-0.008}$
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.17	0.007
R	0 to 15°	0 to 15°

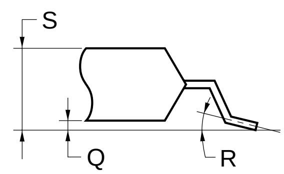
P64C-70-750A,C-3

Remark The external dimensions and materials of the ES version are the same as those of the mass-produced version.

64 PIN PLASTIC QFP (□14)



detail of lead end



NOTE

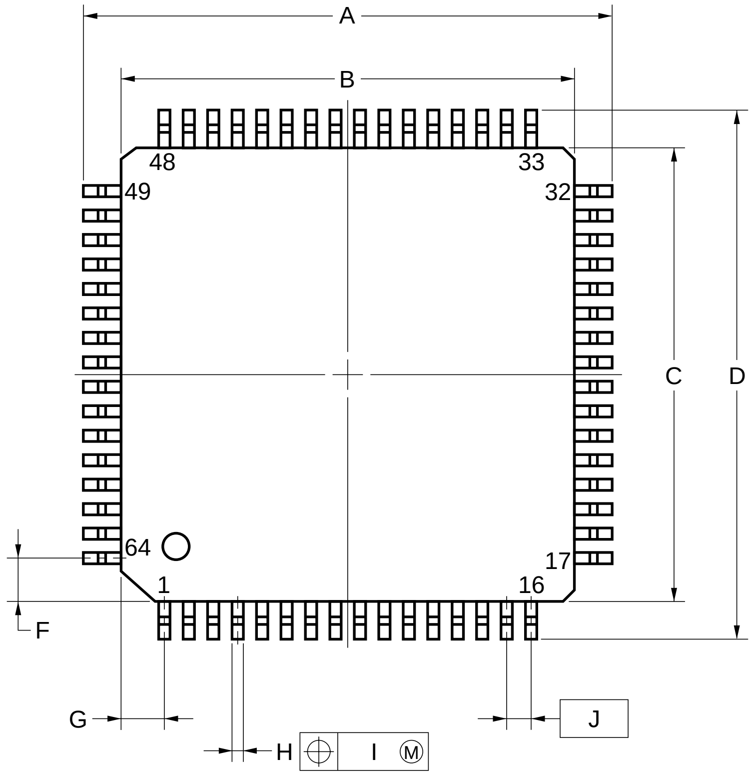
1. Controlling dimension —— millimeter.
2. Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	17.6±0.4	0.693±0.016
B	14.0±0.2	$0.551^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.6±0.4	0.693±0.016
F	1.0	0.039
G	1.0	0.039
H	$0.37^{+0.08}_{-0.07}$	$0.015^{+0.003}_{-0.004}$
I	0.15	0.006
J	0.8 (T.P.)	0.031 (T.P.)
K	1.8±0.2	0.071±0.008
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.17^{+0.08}_{-0.07}$	$0.007^{+0.003}_{-0.004}$
N	0.10	0.004
P	2.55±0.1	0.100±0.004
Q	0.1±0.1	0.004±0.004
R	5°±5°	5°±5°
S	2.85 MAX.	0.113 MAX.

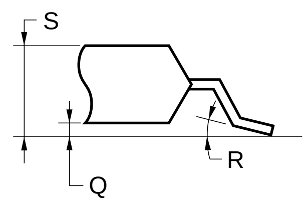
P64GC-80-AB8-4

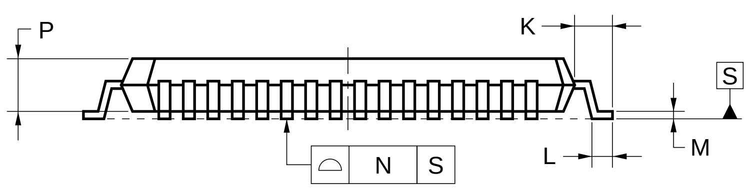
Remark The external dimensions and materials of the ES version are the same as those of the mass-produced version.

64 PIN PLASTIC LQFP (12x12)



detail of lead end





ITEM	MILLIMETERS	INCHES
A	14.8±0.4	0.583±0.016
B	12.0±0.2	$0.472^{+0.009}_{-0.008}$
C	12.0±0.2	$0.472^{+0.009}_{-0.008}$
D	14.8±0.4	0.583±0.016
F	1.125	0.044
G	1.125	0.044
H	0.32±0.08	$0.013^{+0.003}_{-0.004}$
I	0.13	0.005
J	0.65 (T.P.)	0.026
K	1.4±0.2	0.055±0.008
L	0.6±0.2	$0.024^{+0.008}_{-0.009}$
M	$0.17^{+0.08}_{-0.07}$	$0.007^{+0.003}_{-0.004}$
N	0.10	0.004
P	1.4±0.1	$0.055^{+0.004}_{-0.005}$
Q	0.125±0.075	0.005±0.003
R	5°±5°	5°±5°
S	1.7 MAX.	0.067 MAX.

P64GK-65-8A8-2

NOTES

1. Controlling dimension —— millimeter.
2. Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

Remark The external dimensions and materials of the ES version are the same as those of the mass-produced version.

14. RECOMMENDED SOLDERING CONDITIONS

This product should be soldered and mounted under the following recommended conditions.

For the details of the recommended soldering conditions, refer to the document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended below, contact your NEC sales representative.

Table 14-1. Surface Mounting Type Soldering Conditions

(1) μPD780031AYGC-×××-AB8: 64-pin plastic QFP (14 × 14 mm)
μPD780032AYGC-×××-AB8: 64-pin plastic QFP (14 × 14 mm)
μPD780033AYGC-×××-AB8: 64-pin plastic QFP (14 × 14 mm)
μPD780034AYGC-×××-AB8: 64-pin plastic QFP (14 × 14 mm)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds max. (at 210°C or higher), Count: three times or less	IR35-00-3
VPS	Package peak temperature: 215°C, Time: 40 seconds max. (at 200°C or higher), Count: three times or less	VP15-00-3
Wave soldering	Solder bath temperature: 260°C max., Time: 10 seconds max., Count: once, Preheating temperature: 120°C max. (package surface temperature)	WS60-00-1
Partial heating	Pin temperature: 300°C max., Time: 3 seconds max. (per pin row)	—

Caution Do not use different soldering methods together (except for partial heating).

(2) μPD780031AYGK-××× -8A8: 64-pin plastic LQFP (12 × 12 mm)
μPD780032AYGK-××× -8A8: 64-pin plastic LQFP (12 × 12 mm)
μPD780033AYGK-××× -8A8: 64-pin plastic LQFP (12 × 12 mm)
μPD780034AYGK-××× -8A8: 64-pin plastic LQFP (12 × 12 mm)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds max. (at 210°C or higher), Count: two times or less, Exposure limit: 7 days[Note] (after that, prebake at 125°C for 10 hours)	IR35-107-2
VPS	Package peak temperature: 215°C, Time: 40 seconds max. (at 200°C or higher), Count: two times or less, Exposure limit: 7 days[Note] (after that, prebake at 125°C for 10 hours)	VP15-107-2
Wave soldering	Solder bath temperature: 260°C max., Time: 10 seconds max., Count: once, Preheating temperature: 120°C max. (package surface temperature), Exposure limit: 7 days[Note] (after that, prebake at 125°C for 10 hours)	WS60-107-1
Partial heating	Pin temperature: 300°C max., Time: 3 seconds max. (per pin row)	—

Note After opening the dry pack, store it at 25°C or less and 65%RH or less for the allowable storage period.

Caution Do not use different soldering methods together (except for partial heating).

Table 14-2. Insertion Type Soldering Conditions

μPD780031AYCW-×××: 64-pin plastic shrink DIP (750mils)
μPD780032AYCW-×××: 64-pin plastic shrink DIP (750mils)
μPD780033AYCW-×××: 64-pin plastic shrink DIP (750mils)
μPD780034AYCW-×××: 64-pin plastic shrink DIP (750mils)

Soldering Method	Soldering Conditions
Wave soldering (only for pins)	Solder bath temperature: 260°C max., Time: 10 seconds max.
Partial heating	Pin temperature: 300°C max., Time: 3 seconds max. (per pin row)

Caution Apply wave soldering only to the pins and be careful not to bring solder into direct contact with the package.

APPENDIX A. DEVELOPMENT TOOLS

The following development tools are available for system development using the μPD780034AY Subseries.
Also refer to **(5) Cautions on Using Development Tools.**

(1) Language Processing Software

RA78K/0	Assembler package common to 78K/0 Series
CC78K/0	C compiler package common to 78K/0 Series
DF780034	Device file common to μPD780034A Subseries
CC78K/0-L	C compiler library source file common to 78K/0 Series

(2) Flash Memory Writing Tools

Flashpro II (FL-PR2) Flashpro III (FL-PR3, PG-FP3)	Flash programmer dedicated to microcontrollers with on-chip flash memory
FA-64CW FA-64GC FA-64GK	Adapter for flash memory writing

(3) Debugging Tools

- **When using in-circuit emulator IE-78K0-NS**

IE-78K0-NS	In-circuit emulator common to 78K/0 Series
IE-70000-MC-PS-B	Power supply unit for IE-78K0-NS
IE-78K0-NS-PA**Note**	Performance board to enhance and expand the functions of IE-78K0-NS
IE-70000-98-IF-C	Interface adapter when using PC-9800 series as host machine (excluding notebook PCs) (C bus supported)
IE-70000-CD-IF-A	PC card and interface cable when using notebook PC as host machine (PCMCIA socket supported)
IE-70000-PC-IF-C	Interface adapter when using IBM PC/AT™ or compatible as host machine (ISA bus supported)
IE-70000-PCI-IF	Adapter required when using PC in which PCI bus is embedded as host machine
IE-780034-NS-EM1	Emulation board to emulate μPD780034AY Subseries
NP-64CW	Emulation probe for 64-pin plastic shrink DIP (CW type)
NP-64GC NP-64GC-TQ	Emulation probe for 64-pin plastic QFP (GC-AB8 type)
NP-64GK	Emulation probe for 64-pin plastic LQFP (GK-8A8 type)
TGK-064SBW	Conversion adapter to connect NP-64GK and target system board on which a 64-pin plastic LQFP (GK-8A8 type) can be mounted.
EV-9200GC-64	Socket to be mounted on target system board made for 64-pin plastic QFP (GC-AB8 type)
ID78K0-NS	Integrated debugger for IE-78K0-NS
SM78K0	System simulator common to 78K/0 Series
DF780034	Device file common to μPD780034A Subseries

Note Under development

• **When using in-circuit emulator IE-78001-R-A**

IE-78001-R-A	In-circuit emulator common to 78K/0 Series
IE-70000-98-IF-C	Interface adapter when using PC-9800 series as host machine (excluding notebook PCs) (C bus supported)
IE-70000-PC-IF-C	Interface adapter when using IBM PC/AT or compatible as host machine (ISA bus supported)
IE-70000-PCI-IF	Adapter required when using PC in which PCI bus is embedded as host machine
IE-78000-R-SV3	Interface adapter and cable when using EWS as host machine
IE-780034-NS-EM1	Emulation board to emulate μPD780034AY Subseries
IE-78K0-R-EX1	Emulation probe conversion board necessary when using IE-780034-NS-EM1 on IE-78001-R-A
EP-78240CW-R	Emulation probe for 64-pin plastic shrink DIP (CW type)
EP-78240GC-R	Emulation probe for 64-pin plastic QFP (GC-AB8 type)
EP-78012GK-R	Emulation probe for 64-pin plastic LQFP (GK-8A8 type)
TGK-064SBW	Conversion adapter to connect EP-78012GK-R and target system board on which a 64-pin plastic LQFP (GK-8A8 type) can be mounted.
EV-9200GC-64	Socket to be mounted on target system board made for 64-pin plastic QFP (GC-AB8 type)
ID78K0	Integrated debugger for IE-78001-R-A
SM78K0	System simulator common to 78K/0 Series
DF780034	Device file common to μPD780034A Subseries

(4) Real-time OS

RX78K/0	Real-time OS for 78K/0 Series
MX78K0	OS for 78K/0 Series

(5) Cautions on Using Development Tools

- The ID78K0-NS, ID78K0, and SM78K0 are used in combination with the DF780034.
- The CC78K/0 and RX78K/0 are used in combination with the RA78K/0 and the DF780034.
- FL-PR2, FL-PR3, FA-64CW, FA-64GC, FA-64GK, NP-64CW, NP-64GC, NP-64GC-TQ, and NP-64GK are products made by Naito Densei Machida Mfg. Co., Ltd. (+81-44-822-3813).
  Contact an NEC distributor regarding the purchase of these products.
- The TGK-064SBW is a product made by TOKYO ELETECH CORPORATION.
  Refer to: Daimaru Kogyo, Ltd.
  Tokyo Electronic Division (+81-3-3820-7112)
  Osaka Electronic Division (+81-6-6244-6672)
- For third-party development tools, see the **78K/0 Series Selection Guide (U11126E)**.
- The host machines and OSs supporting each software are as follows.

Software \ Host Machine [OS]	PC	EWS
	PC-9800 series [Windows™] IBM PC/AT and compatibles [Japanese/English Windows]	HP9000 series 700™ [HP-UX™] SPARCstation™ [SunOS™, Solaris™] NEWS™ (RISC) [NEWS-OS™]
RA78K/0	√ **Note**	√
CC78K/0	√ **Note**	√
ID78K0-NS	√	–
ID78K0	√	√
SM78K0	√	–
RX78K/0	√ **Note**	√
MX78K0	√ **Note**	√

Note DOS-based software

APPENDIX B. RELATED DOCUMENTS

Documents Related to Devices

Document Name	Document No. (English)	Document No. (Japanese)
μPD780024A, 780034A, 780024AY, 780034AY Subseries User's Manual	U14046E	U14046J
μPD780031AY, 780032AY, 780033AY, 780034AY Data Sheet	This document	U14045J
μPD78F0034AY Data Sheet	U14041E	U14041J
78K/0 Series User's Manual Instructions	U12326E	U12326J
78K/0 Series Instruction Table	—	U10903J
78K/0 Series Instruction Set	—	U10904J

Documents Related to Development Tools (User's Manuals)

Document Name		Document No. (English)	Document No. (Japanese)
RA78K0 Assembler Package	Operation	U11802E	U11802J
	Assembly Language	U11801E	U11801J
	Structured Assembly Language	U11789E	U11789J
RA78K Series Structured Assembler Preprocessor		EEU-1402	U12323J
CC78K0 C Compiler	Operation	U11517E	U11517J
	Language	U11518E	U11518J
CC78K0 C Compiler Application Note	Programming Know-how	U13034E	U13034J
IE-78K0-NS		To be prepared	To be prepared
IE-78001-R-A		To be prepared	To be prepared
IE-780034-NS-EM1		To be prepared	To be prepared
EP-78240		U10332E	EEU-986
EP-78012GK-R		EEU-1538	EEU-5012
SM78K0 System Simulator Windows based	Reference	U10181E	U10181J
SM78K Series System Simulator	External Part User Open Interface Specifications	U10092E	U10092J
ID78K0-NS Integrated Debugger Windows based	Reference	U12900E	U12900J
ID78K0 Integrated Debugger EWS based	Reference	—	U11151J
ID78K0 Integrated Debugger PC based	Reference	U11539E	U11539J
ID78K0 Integrated Debugger Windows based	Guide	U11649E	U11649J

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document for designing.

Documents Related to Embedded Software (User's Manuals)

Document Name		Document No. (English)	Document No. (Japanese)
78K/0 Series Real-time OS	Basics	U11537E	U11537J
	Installation	U11536E	U11536J
78K/0 Series OS MX78K0	Basics	U12257E	U12257J

Other Related Documents

Document Name	Document No. (English)	Document No. (Japanese)
SEMICONDUCTORS SELECTION GUIDE Products & Packages (CD-ROM)	X13769X	
Semiconductor Device Mounting Technology Manual	C10535E	C10535J
Quality Grades on NEC Semiconductor Devices	C11531E	C11531J
NEC Semiconductor Device Reliability/Quality Control System	C10983E	C10983J
Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD)	C11892E	C11892J
Guide to Microcomputer-Related Products by Third Party	—	U11416J

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[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Caution **Purchase of NEC I^2C components conveys a license under the Philips I^2C Patent Rights to use these components in an I^2C system, provided that the system conforms to the I^2C Standard Specification as defined by Philips.**

Regional Information

Some information contained in this document may vary from country to country. Before using any NEC product in your application, please contact the NEC office in your country to obtain a list of authorized representatives and distributors. They will verify:

- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

In addition, trademarks, registered trademarks, export restrictions, and other legal issues may also vary from country to country.

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