NEC

BIPOLAR ANALOG INTEGRATED CIRCUIT

μPC8110GR

1 GHz DIRECT QUADRATURE MODULATOR FOR DIGITAL MOBILE COMMUNICATION

DESCRIPTION

The μPC8110GR is a sillicon monolithic integrated circuit designed as 1 GHz direct quadrature modulator for digital mobile communication systems. This modulator housed in a 20 pin plastic SSOP that easy to install and contributes to miniaturizing the system.

The device has power save function and can operates 2.7 to 3.6 V supply voltage to realize low power consumption.

FEATURES

- Direct modulation range : 800 MHz to 1 GHz
- Supply voltage range : V_{CC} = 2.7 to 3.6 V
- Low operation current : I_{CC} = 24 mA typical @ V_{CC} = 3 V
- Low phase difference due to digital phase shifter is adopted.
- 20 pin SSOP suitable for high density surface mounting.
- Low current sleep mode

APPLICATION

- Digital cellular phone (PDC, IS-54/IS-136, GSM etc..)

ORDERING INFORMATION

PART NUMBER	PACKAGE	PACKING FORM
μPC8110GR-E1	20 pin plastic SSOP	Carrier tape width 12 mm. Q'ty 2.5 kp/Reel Pin 1 indicated pull-out direction of tape.

Remark For evaluation sample order, please contact your local NEC sales office. (Order number: μPC8110GR)

Caution electro-static sensitive device

The information in this document is subject to change without notice. Before using this document, please confirm that this is the latest version.
Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

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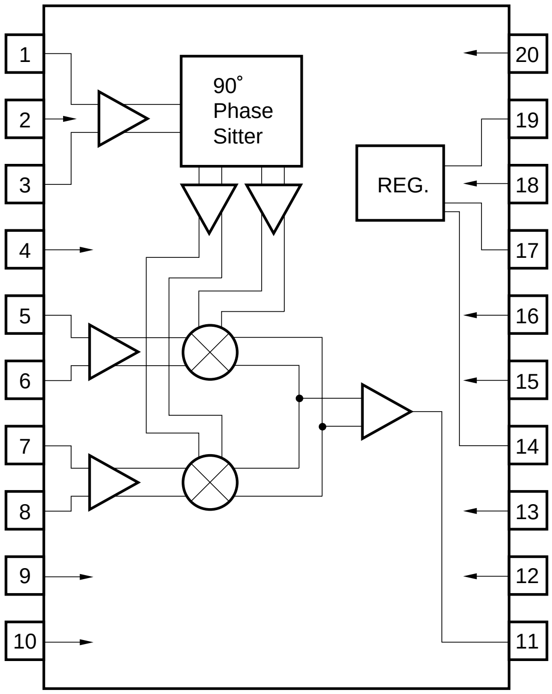
The mark ★ shows major revised points.

INTERNAL BLOCK DIAGRAM AND PIN CONNECTIONS

(Top View)



1. LO_{in}
2. GND
3. $\overline{LO}_{in}$
4. GND
5. Q-INPUT
6. $\overline{Q}$-INPUT
7. $\overline{I}$-INPUT
8. I-INPUT
9. GND
10. GND
11. RF_{out}
12. GND
13. GND
14. V_{CC}
15. GND
16. GND
17. Power Save (V_{PS})
18. GND
19. V_{CC}
20. GND

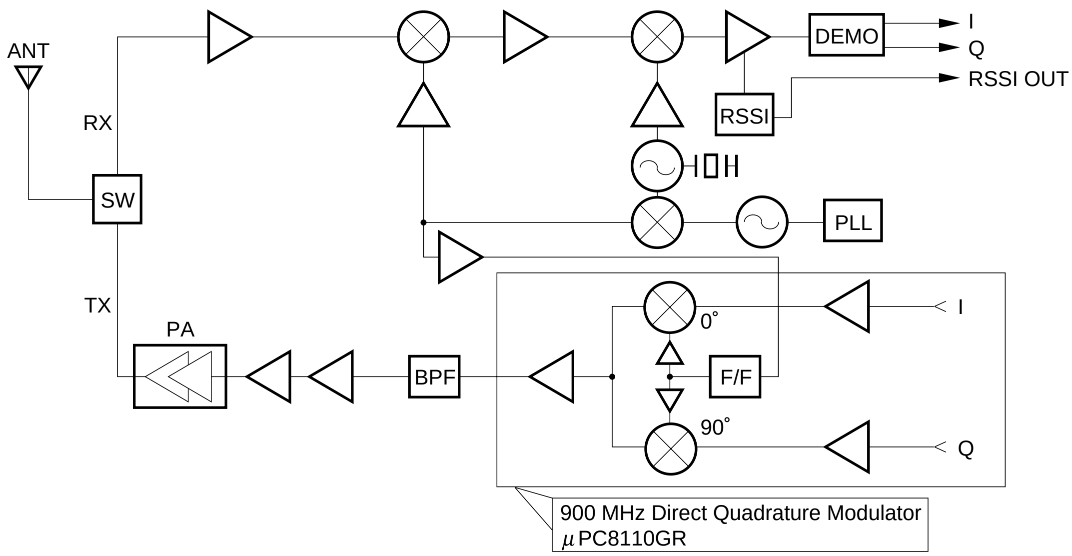
SERIES PRODUCTS

SERIES TYPE	PART NUMBER	f $LO1_{in}$ (MHz)	f MOD_{out} (MHz)	f I/Q (MHz)	Up-Converter f RF_{out} (MHz)	APPLICATION
150 MHz Quadrature MOD	μPC8101GR	100 to 300	50 to 150	DC to 0.5	External	CT2, Digital Comm.
Up-Con+Quadrature MOD	μPC8104GR	100 to 400		DC to 10	900 to 1900	PHS, PDC etc..
400 MHz Quadrature MOD	μPC8105GR	100 to 400		DC to 10	External	PDC, IS-136, GSM, PHS
1 GHz direct Quad MOD	μPC8110GR	800 to 1000		DC to 10	Direct	PDC, IS-136, GSM etc.

Remark As for detail information of series products, please refer to each data sheet.

APPLICATION EXAMPLE

PDC 900 MHz (Direct Modulation Type)



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	TEST CONDITIONS
Supply Voltage	V_{CC}	4.0	V	T_A = +25 °C
Power Save Voltage	V_{PS}	4.0	V	T_A = +25 °C
Power Dissipation	P_D	430	mW	T_A = +85 °C Note 1
Operating Temperature	T_{opt}	–40 to +85	°C	
Storage Temperature	T_{stg}	–55 to +150	°C	

Note 1. Mounted on 50 × 50 × 1.6 mm double copper clad epoxy glass board

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Supply Voltage	V_{CC}	2.7	3.0	3.6	V	
Operating Temperature	T_{opt}	–40	+25	+85	°C	
L_O Input Frequency	f_{LOin}	800	900	1000	MHz	
L_O Input Power Level	P_{LOin}	–15	–10	–7	dBm	
I/Q Input Frequency	$f_{I/Qin}$	DC		10	MHz	
I/Q Input Voltage	$V_{I/Qin}$			500	mV_{p-p}	Single ended input
				250		Differential input

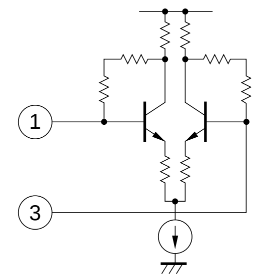
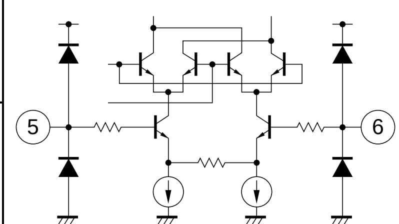
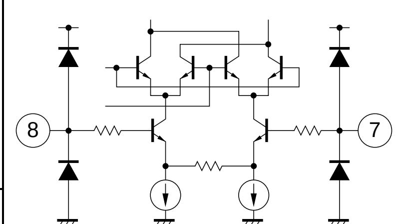
ELECTRICAL CHARACTERISTICS (T_A = 25 °C, V_{CC} = 3.0 V, Unless Otherwise Specified V_{PS} ≥ 2.2 V (High))

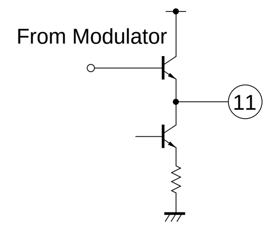
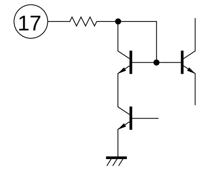
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Circuit Current	I_{CC}	20	24	33	mA	No input signal
Circuit Current at Power Save Mode	$I_{CC(PS)}$			10	uA	V_{PS} ≤ 0.5 V (Low)
Maximum Output Power	$P_{o(sat)}$	–13	–10		dBM	f_{LOin} = 948 MHz P_{LOin} = –10 dBm $f_{I/Q}$ = 2.625 kHz I/Q (DC) = V_{CC}/2 $V_{I/Qin}$ = 500 mV_{p-p} (Single ended)
L_O Carrier Leak	LoL		–35	–30	dBc	
Image Rejection (Side Band Leak)	ImR		–40	–30	dBc	
I/Q 3rd Order Intermodulation Distortion	$IM_{3I/Q}$		–45	–30	dBc	
Power Save Rise Time	$T_{PS(RISE)}$		3	5	μs	V_{PS}: Low → High
Power Save Fall Time	$T_{PS(FALL)}$		2	5	μs	V_{PS}: High → Low

STANDARD CHARACTERISTICS FOR REFERENCE
(T_A = +25 °C, V_{CC} = 3.0 V, Unless Otherwise Specified V_{PS} ≥ 2.2 V (Hgih))

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
I/Q Input Impeadance	$Z_{I/Qin}$		150		kΩ	$f_{I/Q}$ = DC to 10 MHz
L_O Input VSWR	VSWR (Lo)		1.5 : 1		–	f_{LO} = 948 MHz
RF Output VSWR	VSWR (RF)		1.5 : 1		–	f_{LO} = 948 MHz

PIN EXPLANATION

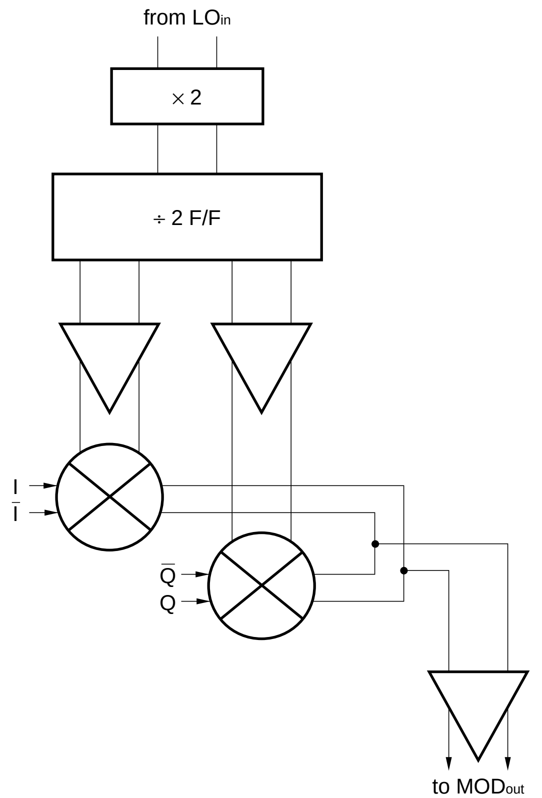
Pin No.	ASSIGNMENT	SUPPLY VOL. (V)	PIN VOL. (V)	FUNCTION AND APPLICATION	EQUIVALENT CIRCUIT
1	L_{Oin}	—	2.6	L_O input for phase shifter. Connect around 50 Ω between 1 and 3 pin to match to 50 Ω.	
2 18	GND (for Local Amp. Block)	0	—	Connect to the ground with minimum inductance. Track length should be kept as short as possible.	
3	$\overline{L_{Oin}}$	—	2.6	Bypass of L_O input. This pin is grounded through around 33 pF capacitor.	
5	Q	$V_{CC}/2$	—	Input for Q signal. This input impedance is 150 kΩ. In case of that I/Q input signals are single ended, amplitude of the signal is 500 mVp-p max. **Note 2**	
6	$\overline{Q}$	$V_{CC}/2$	—	Input for Q signal. This input impedance is 150 kΩ. In case of that I/Q input signals are single ended, $V_{CC}/2$ biased DC signal should be input. In case of that I/Q input signals are differential, amplitude of the signal is 250 mVp-p max. **Note 2**	
7	$\overline{I}$	$V_{CC}/2$	—	Input for I signal. This input impedance is 150 kΩ. In case of that I/Q input signals are single ended, $V_{CC}/2$ biased DC signal should be input. In case of that I/Q input signals are differential, amplitude of the signal is 250 mVp-p max. **Note 2**	
8	I	$V_{CC}/2$	—	Input for I signal. This input impedance is 150 kΩ. In case of that I/Q input signals are single ended, amplitude of the signal is 500 mVp-p max. **Note 2**	
9 13 16	GND (for Quadrature Modulator Block)	0	—	Connect to the ground with minimum inductance. Track length should be kept as short as possible.	—

Pin No.	ASSIGNMENT	SUPPLY VOL. (V)	PIN VOL. (V)	FUNCTION AND APPLICATION	EQUIVALENT CIRCUIT
11	RF_{out}	—	1.6	Output from modulator. This is single-end push-pull amplifier. So this output impedance is Low.	
12	GND (for Output Push-pull Amplifier)	0	—	Connect to the ground with minimum inductance. Track length should be kept as short as possible.	
14	V_{CC} (for Output Amplifier of Modulator)	2.7 to 3.6	—	Supply voltage pin for Output Amplifier of modulator. Internal regulator can be kept stable condition of supply bias against the variable temperature or V_{CC}.	
17	Power Save	$V_{P/S}$	—	Power save control pin can be controlled ON/SLEEP state with bias as follows; $V_{P/S}$ / STATE 2.2 to 3.6 / ON 0 to 0.5 / SLEEP	
19	V_{CC}	2.7 to 3.6	—	Supply voltage pin for modulator except output Amplifier. Internal regulator can be kept stable condition of supply bias against the variable temperature or V_{CC}.	—
4 10 15 20	GND	0	—	Connect to the ground with minimum inductance. Track length should be kept as short as possible.	—

Note 2. Relations between amplitude and $V_{CC}/2$ bias of input signal are following.

Supply Voltage V_{CC} (V)	I/Q DC Voltage (V) $V_{CC}/2 = I = \overline{I} = Q = \overline{Q}$	$P_{I/Qin}$ - I/Q Input Signal - mVp-p	
		Single ended input I = Q	Differential input $I = \overline{I} = Q = \overline{Q}$
2.7 to 3.6	1.35 to 1.8	≤ 500	≤ 250

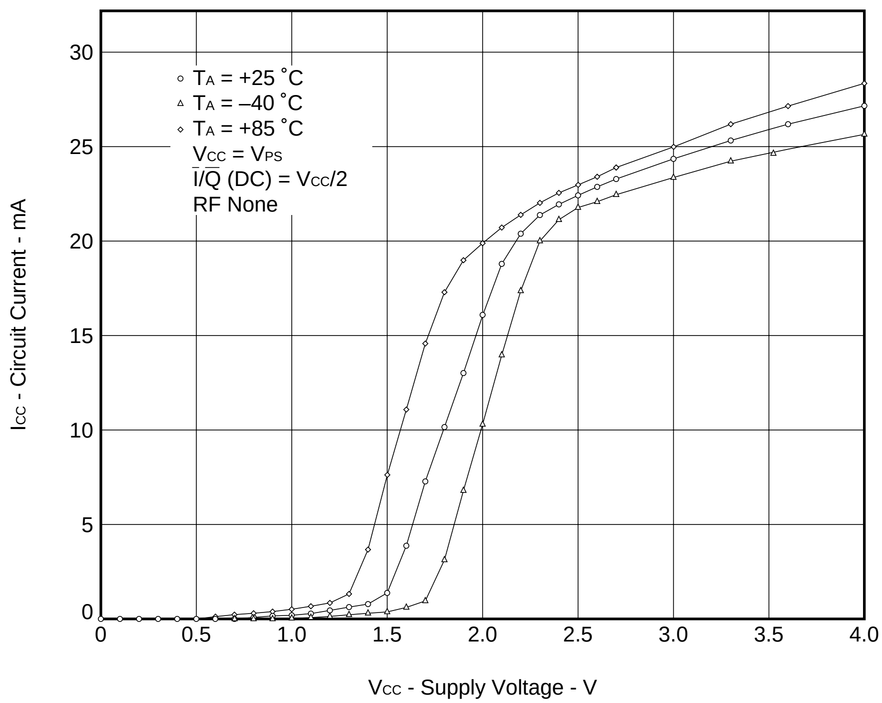
EXPLANATION OF INTERNAL FUNCTION

BLOCK	FUNCTION/OPERATION	BLOCK DIAGRAM
90 ° PHASE SHIFTER	Input signal from LO is send to digital circuit of T-type flip-flop through frequency doubler. Output signal from T-type F/F is changed to same frequency as LO input and that have quadrature phase shift, 0 °, 90 °, 180 °, 270 °. These circuits have function of self phase correction to make correctly quadrature signals.	
BUFFER AMP.	Buffer amplifiers for each phase signals to send to each mixers.	
MIXER	Each signals from buffer amp. are quadrature modulated with two double-balanced mixers. High accurate phase and amplitude inputs are realized to good performance for image rejection.	
ADDER	Output signals from each mixers are added with adder and send to final amplifier.	

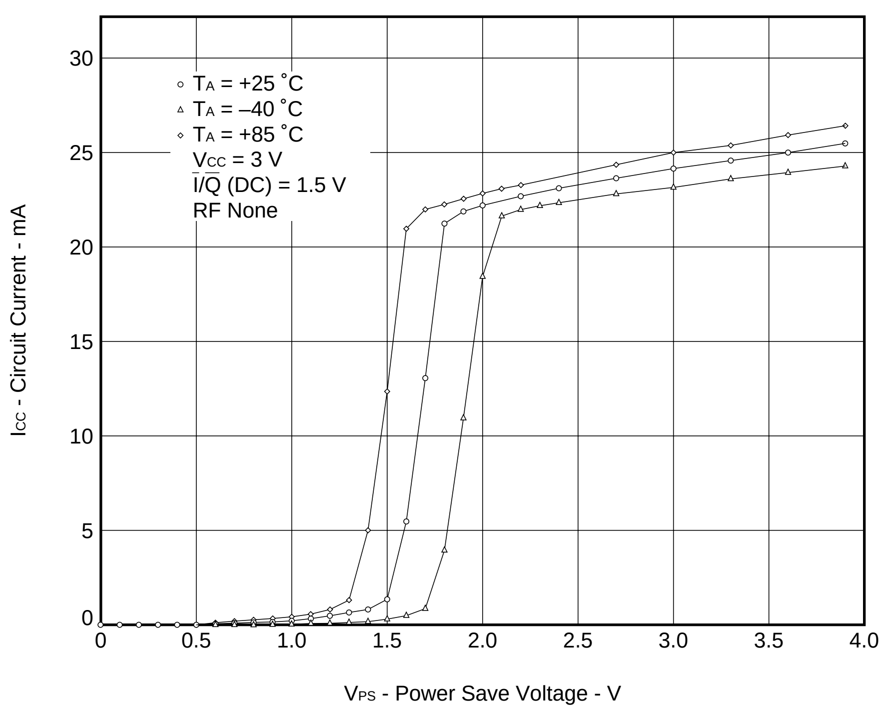
TYPICAL CHARACTERISTICS

Unless otherwise specified T_A = +25 °C, V_{CC} = V_{PS} = 3 V, I/Q DC/offset = $\overline{I}/\overline{Q}$ DC offset = 1.5 V, I/Q Input signal = 500 m$V_{p\text{-}p}$ (Single ended), $f_{I/Q}$ = 2.625 kHz, f_{LOin} = 948 MHz, P_{LOin} = –10 dBm, <PDC> Transmission speed: 42 kbps, RNYQ: a = 0.5.

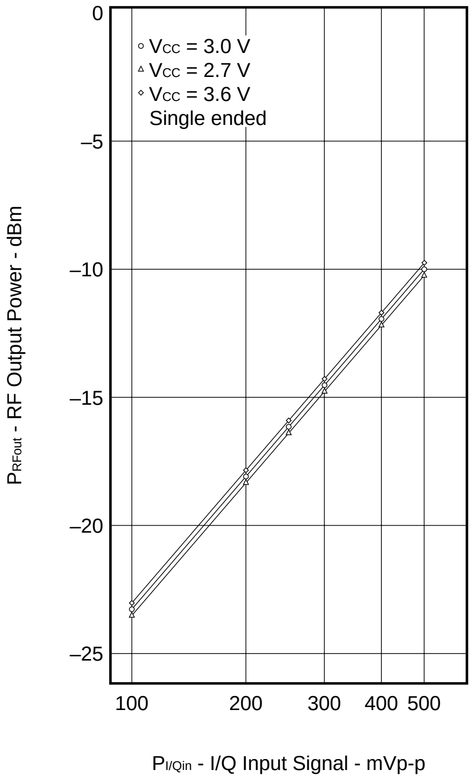
CIRCUIT CURRENT vs SUPPLY VOLTAGE



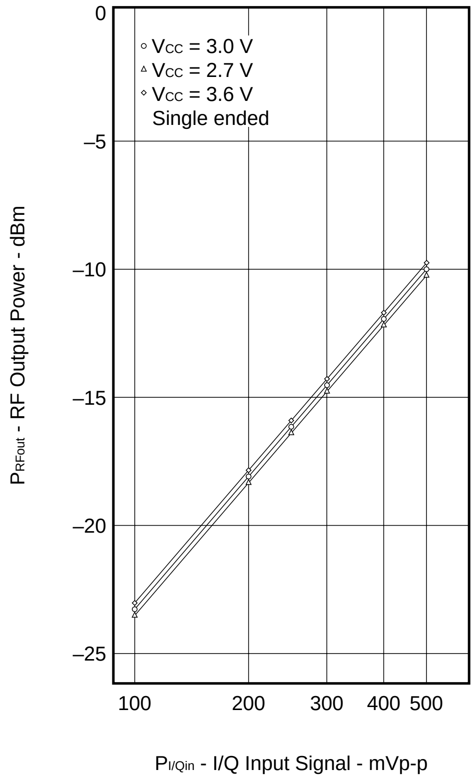
CIRCUIT CURRENT vs POWER SAVE VOLTAGE



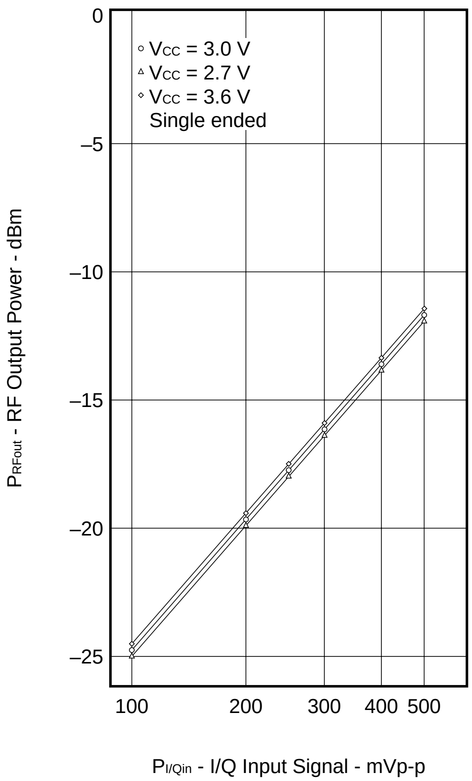
RF OUTPUT POWER vs I/Q INPUT SIGNAL
(at T_A = –40 ˚C)



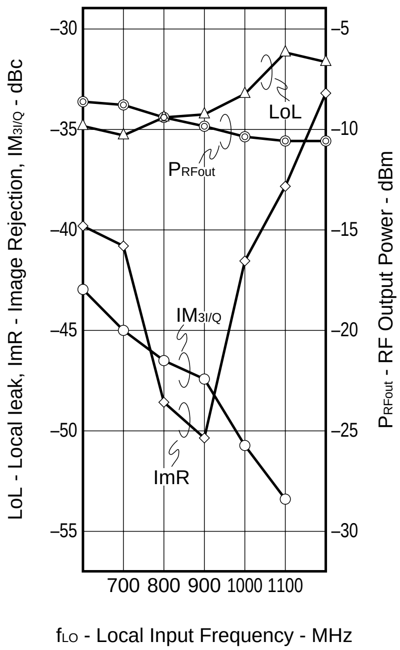
RF OUTPUT POWER vs I/Q INPUT SIGNAL
(at T_A = +25 ˚C)



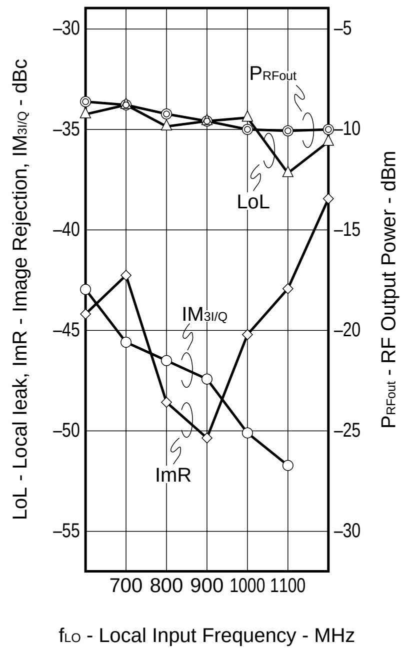
RF OUTPUT POWER vs I/Q INPUT SIGNAL
(at T_A = +85 ˚C)



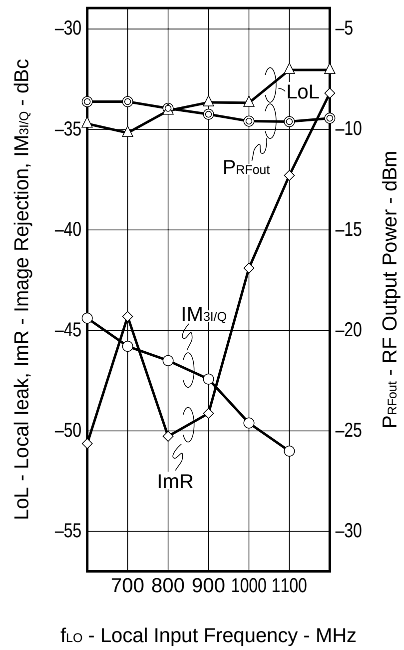
Lo INPUT FREQUENCY vs
P_{RFout}, LoL, ImR, $IM_{3I/Q}$
(at V_{CC} = 2.7 V, T_A = –40 ˚C)



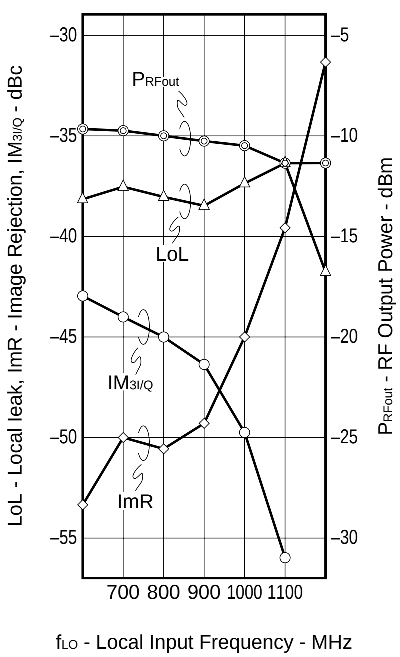
Lo INPUT FREQUENCY vs
P_{RFout}, LoL, ImR, $IM_{3I/Q}$
(at V_{CC} = 3.0 V, T_A = –40 ˚C)



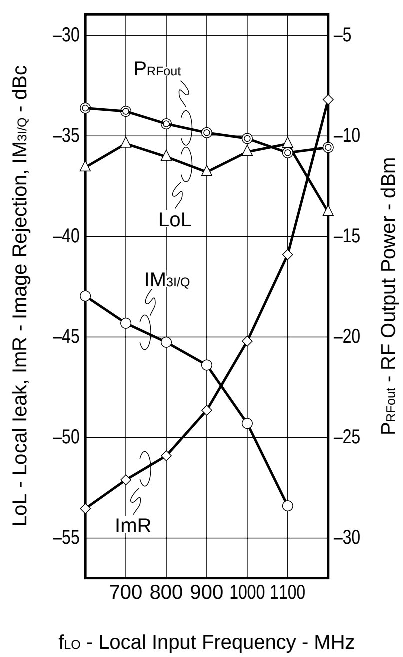
Lo INPUT FREQUENCY vs
P_{RFout}, LoL, ImR, $IM_{3I/Q}$
(at V_{CC} = 3.6 V, T_A = –40 ˚C)



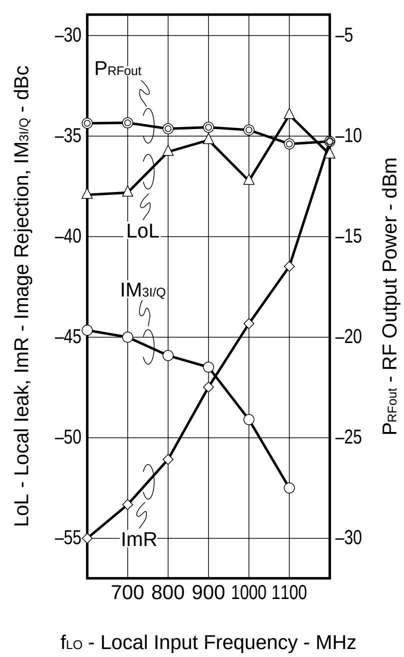
Lo INPUT FREQUENCY vs
P_{RFout}, LoL, ImR, $IM_{3I/Q}$
(at V_{CC} = 2.7 V, T_A = +25 ˚C)



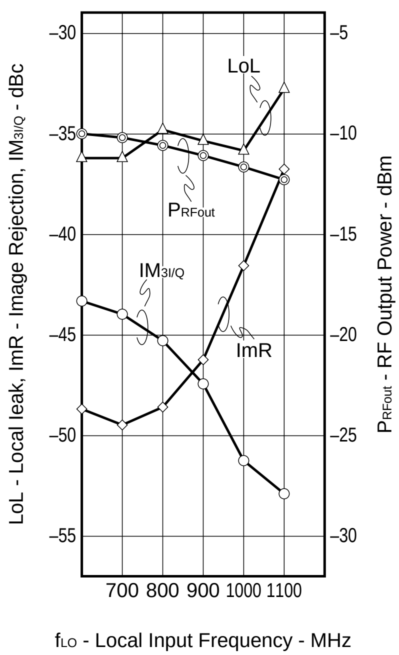
Lo INPUT FREQUENCY vs
P_{RFout}, LoL, ImR, $IM_{3I/Q}$
(at V_{CC} = 3.0 V, T_A = +25 ˚C)



Lo INPUT FREQUENCY vs
P_{RFout}, LoL, ImR, $IM_{3I/Q}$
(at V_{CC} = 3.6 V, T_A = +25 ˚C)



Lo INPUT FREQUENCY vs
P_{RFout}, LoL, ImR, $IM_{3I/Q}$
(at V_{CC} = 2.7 V, T_A = +85 °C)



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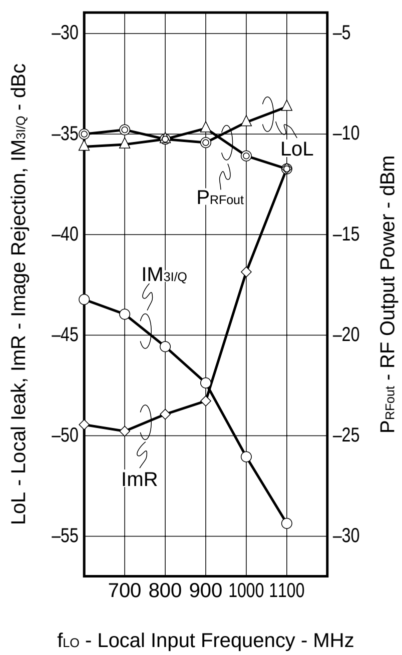
P_{RFout}, LoL, ImR, $IM_{3I/Q}$
(at V_{CC} = 3.0 V, T_A = +85 °C)



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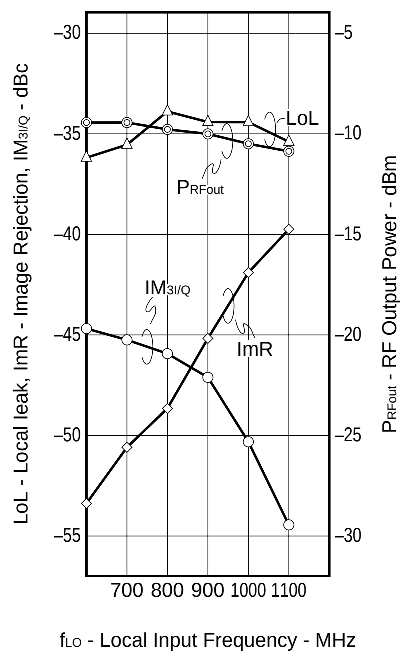
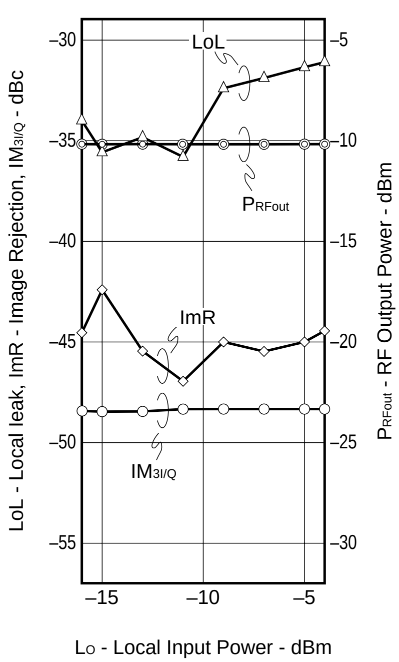
P_{RFout}, LoL, ImR, $IM_{3I/Q}$
(at V_{CC} = 3.6 V, T_A = +85 °C)



Lo INPUT POWER vs
P_{RFout}, LoL, ImR, $IM_{3I/Q}$
(at V_{CC} = 2.7 V, T_A = –40 °C)



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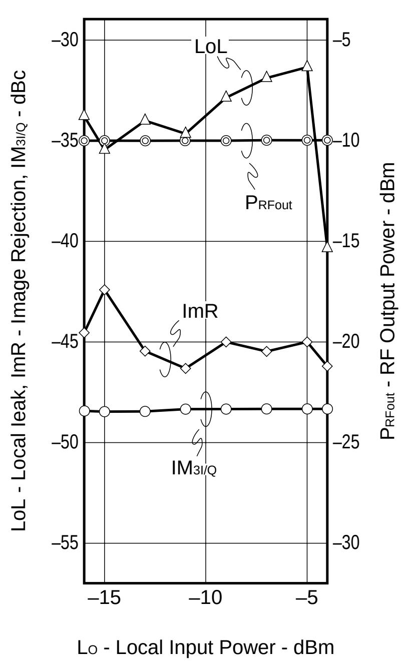
P_{RFout}, LoL, ImR, $IM_{3I/Q}$
(at V_{CC} = 3.0 V, T_A = –40 °C)



Lo INPUT POWER vs
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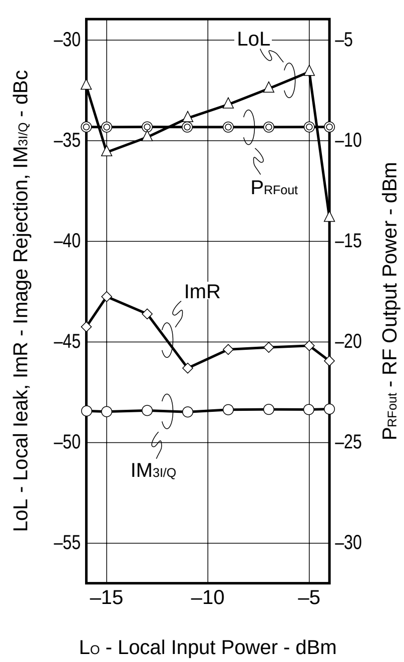
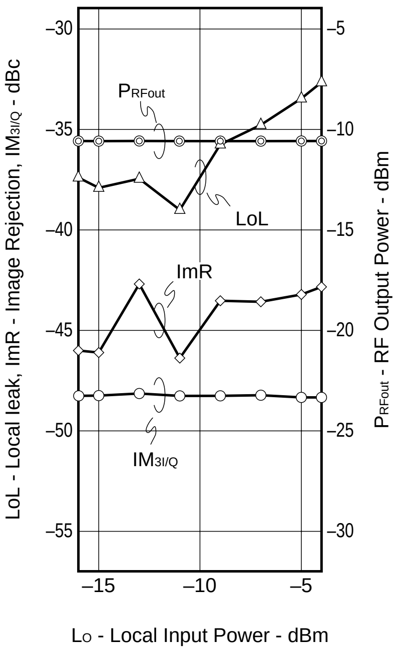
(at V_{CC} = 3.6 V, T_A = –40 °C)



Lo INPUT POWER vs
PRFout, LoL, ImR, IM3I/Q
(at Vcc = 2.7 V, TA = +25 ˚C)



Lo INPUT POWER vs
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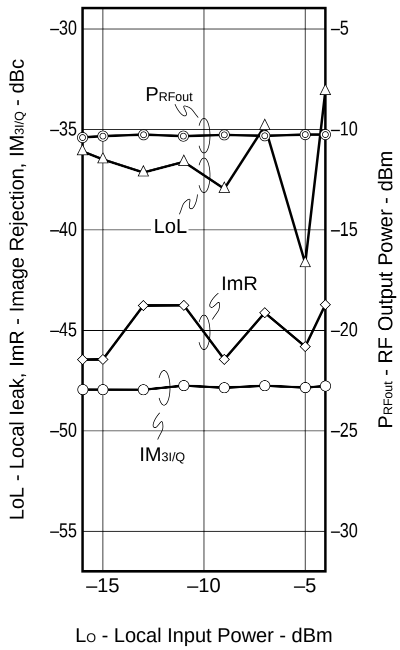
(at Vcc = 3.0 V, TA = +25 ˚C)



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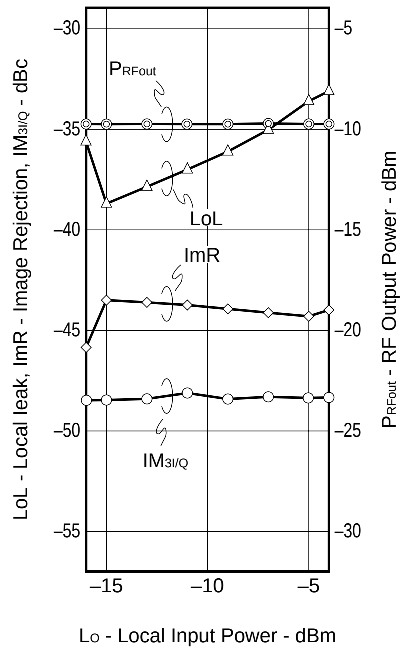
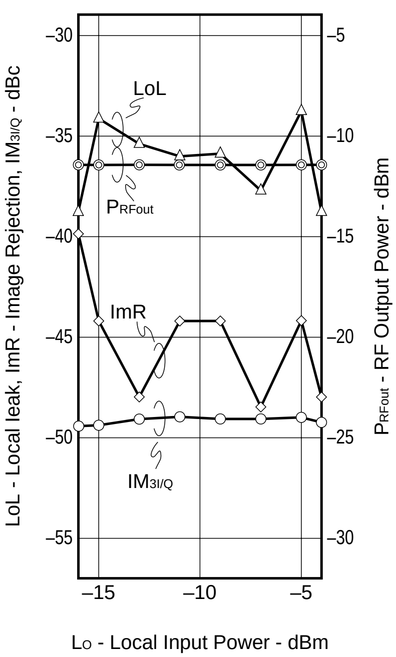
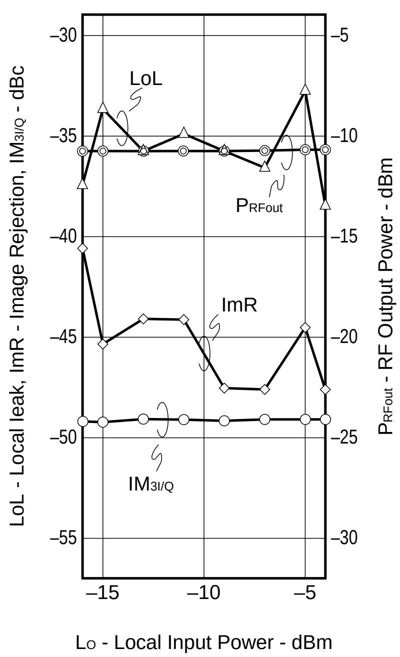


Lo INPUT POWER vs
PRFout, LoL, ImR, IM3I/Q
(at Vcc = 2.7 V, TA = +85 ˚C)



Lo INPUT POWER vs
PRFout, LoL, ImR, IM3I/Q
(at Vcc = 3.0 V, TA = +85 ˚C)



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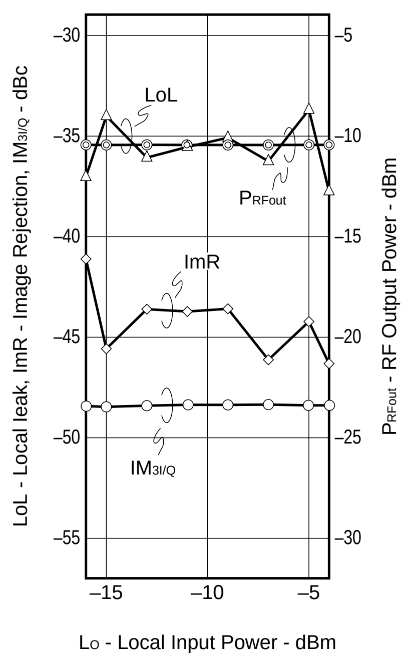
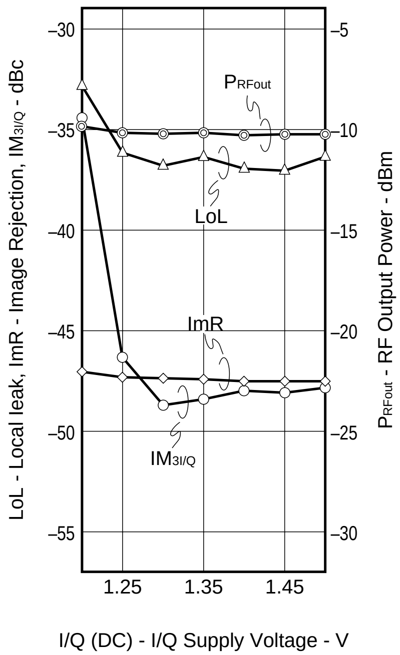
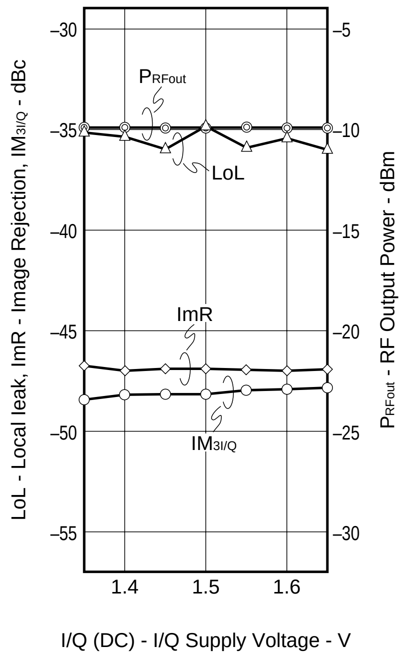
PRFout, LoL, ImR, IM3I/Q
(at Vcc = 3.6 V, TA = +85 ˚C)



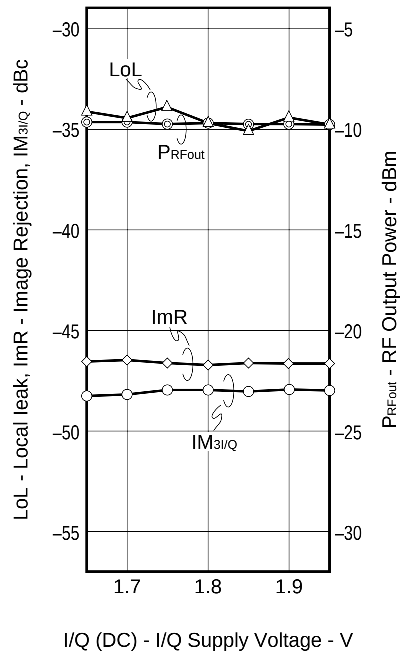
I/Q BIASE VOLTAGE vs
P_{RFout}, LoL, ImR, $IM_{3I/Q}$
(at V_{CC} = 2.7 V, T_A = –40 ˚C)



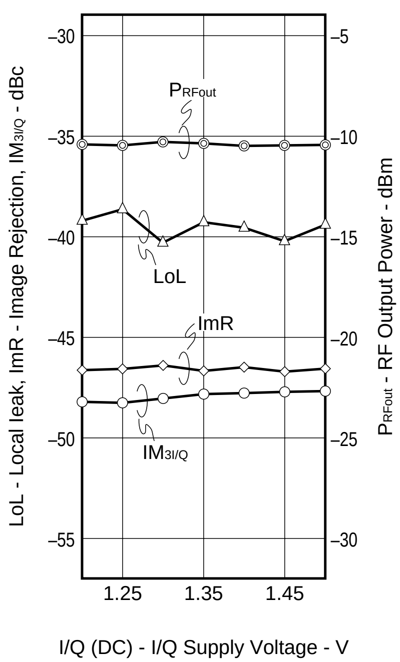
I/Q BIASE VOLTAGE vs
P_{RFout}, LoL, ImR, $IM_{3I/Q}$
(at V_{CC} = 3.0 V, T_A = –40 ˚C)



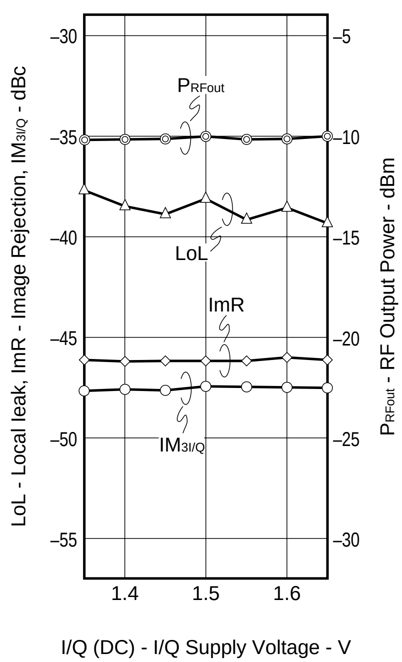
I/Q BIASE VOLTAGE vs
P_{RFout}, LoL, ImR, $IM_{3I/Q}$
(at V_{CC} = 3.6 V, T_A = –40 ˚C)



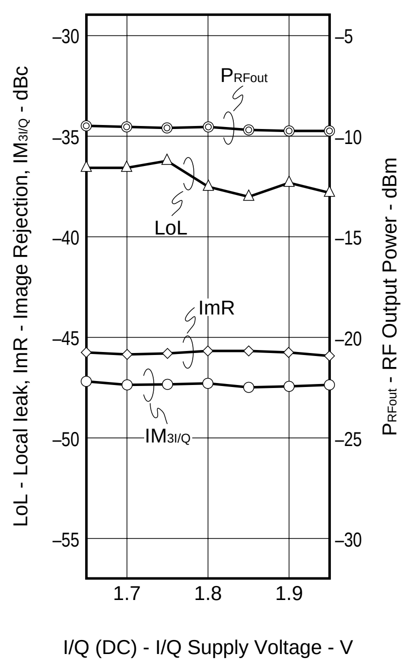
I/Q BIASE VOLTAGE vs
P_{RFout}, LoL, ImR, $IM_{3I/Q}$
(at V_{CC} = 2.7 V, T_A = +25 ˚C)



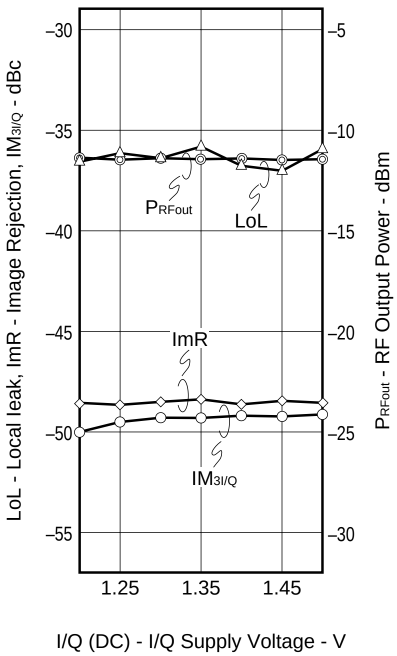
I/Q BIASE VOLTAGE vs
P_{RFout}, LoL, ImR, $IM_{3I/Q}$
(at V_{CC} = 3.0 V, T_A = +25 ˚C)



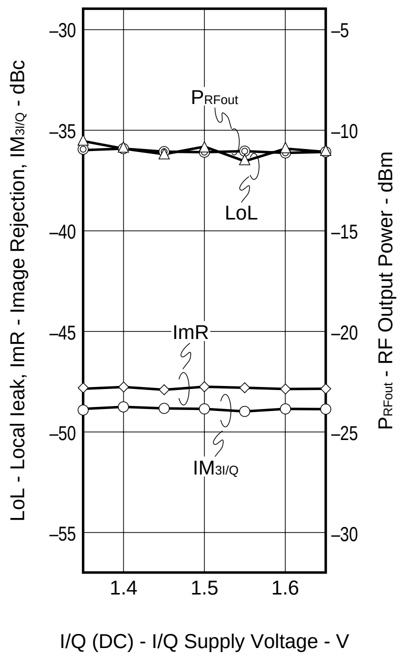
I/Q BIASE VOLTAGE vs
P_{RFout}, LoL, ImR, $IM_{3I/Q}$
(at V_{CC} = 3.6 V, T_A = +25 ˚C)



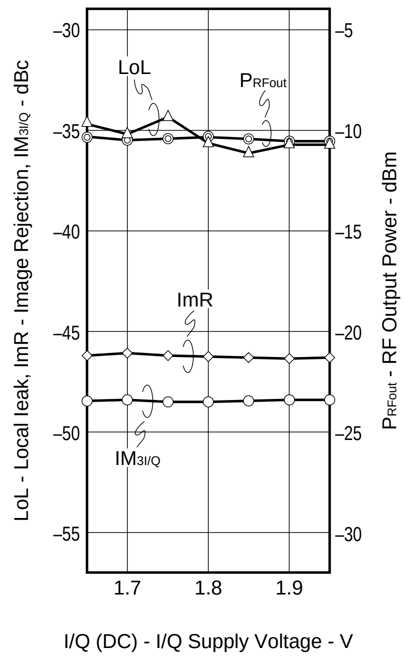
I/Q BIASE VOLTAGE vs
P_{RFout}, LoL, ImR, $IM_{3I/Q}$
(at V_{CC} = 2.7 V, T_A = +85 ˚C)



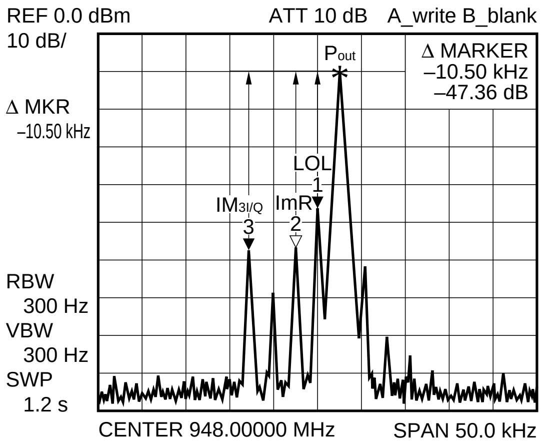
I/Q BIASE VOLTAGE vs
P_{RFout}, LoL, ImR, $IM_{3I/Q}$
(at V_{CC} = 3.0 V, T_A = +85 ˚C)



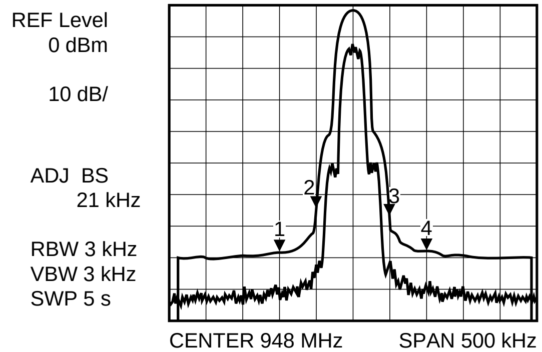
I/Q BIASE VOLTAGE vs
P_{RFout}, LoL, ImR, $IM_{3I/Q}$
(at V_{CC} = 3.6 V, T_A = +85 ˚C)



TYPICAL SINE WAVE MODULATION OUTPUT SPECTRUM
<PDC> 42 kbps, RNYQ α = 0.5, MOD Pattern [0000]

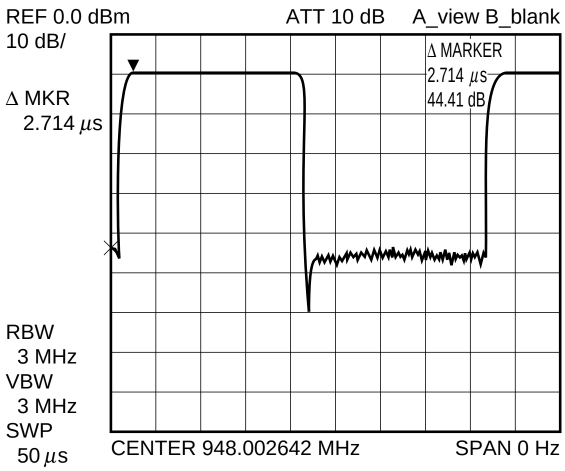


TYPICAL π/4DQPSK MODULATION OUTPUT SPECTRUM
<PDC> 42 kbps, RNYQ α = 0.5, MOD Pattern [PN9]

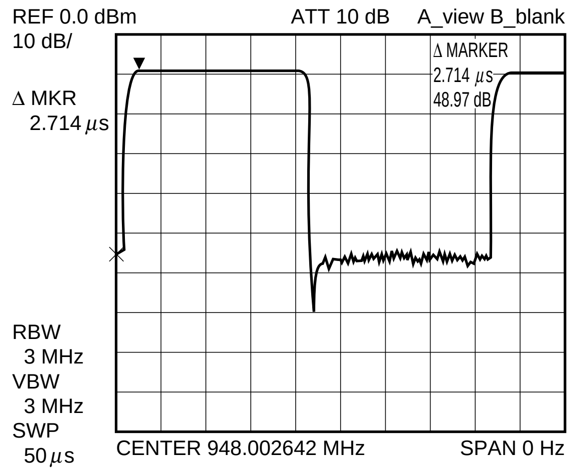


Padj (dB)	Marker			
		No.1 : 947.90 MHz	–78.0 dB	Δf = –100 kHz
		No.2 : 947.95 MHz	–67.0 dB	Δf = –50 kHz
		No.3 : 948.05 MHz	–70.3 dB	Δf = +50 kHz
		No.4 : 948.10 MHz	–77.8 dB	Δf = +100 kHz

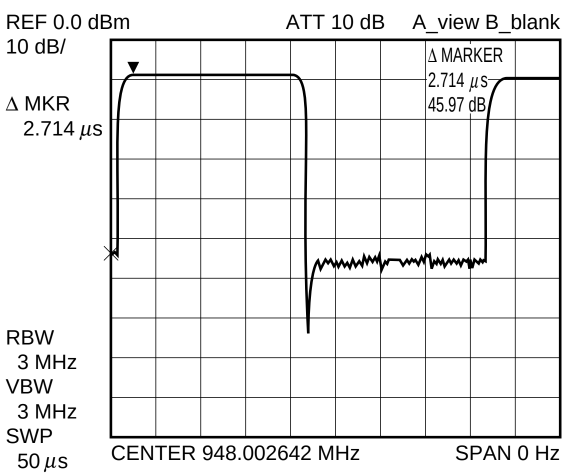
POWER SAVE RESPONSE
(at $V_{CC} = V_{PS} = 2.7$ V)



POWER SAVE RESPONSE
(at $V_{CC} = V_{PS} = 3.0$ V)

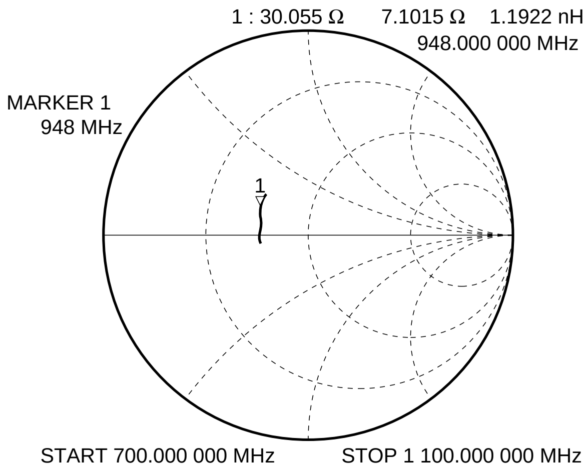


POWER SAVE RESPONSE
(at $V_{CC} = V_{PS} = 3.6$ V)

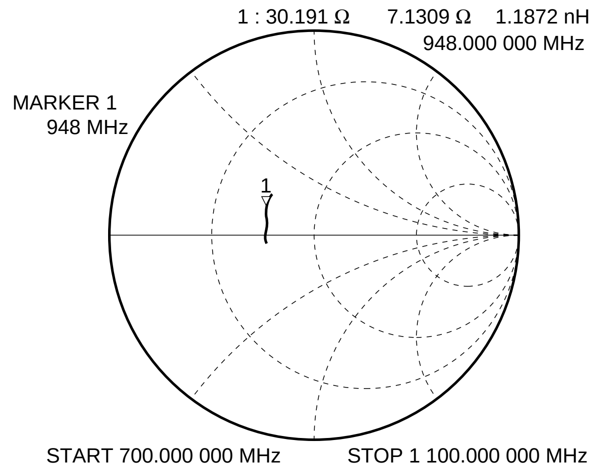


LO INPUT (LOin) IMPEDANCE

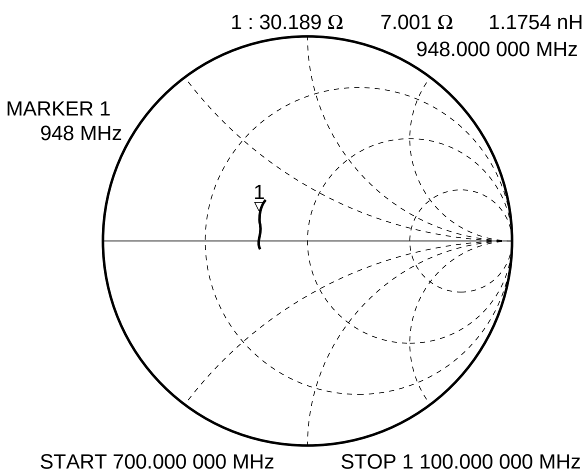
$V_{CC} = V_{PS} = 2.7$ V



$V_{CC} = V_{PS} = 3.0$ V

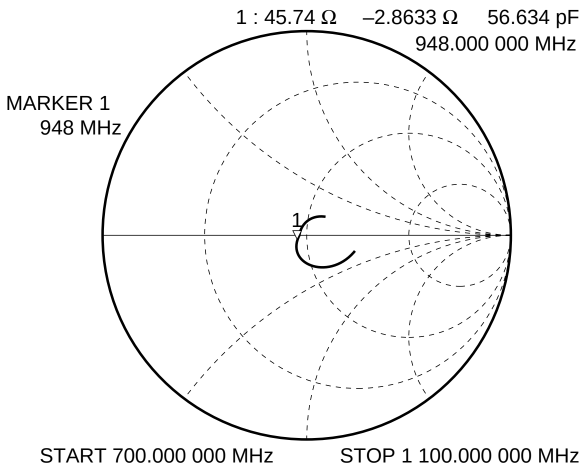


$V_{CC} = V_{PS} = 3.6$ V

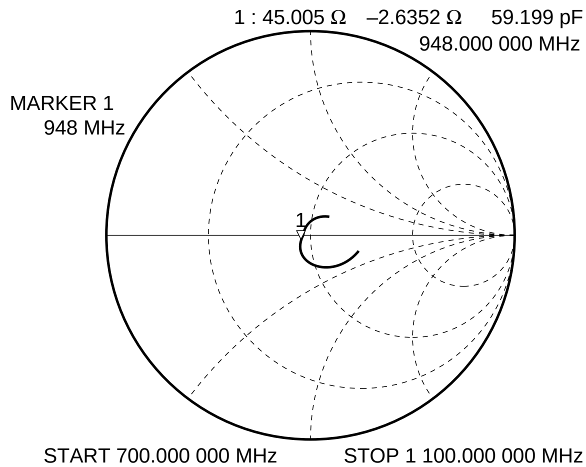


RF OUTPUT (RF_{out}) IMPEDANCE

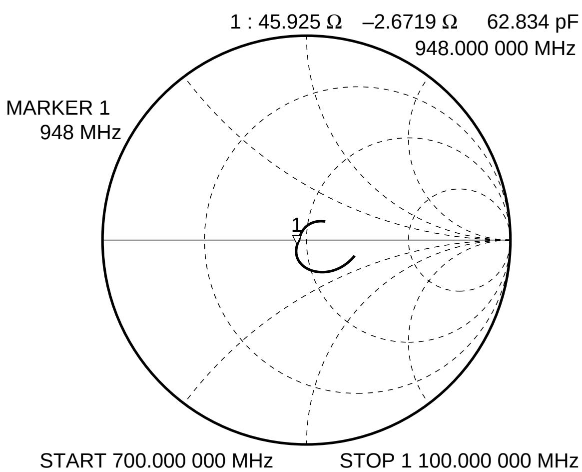
$V_{CC} = V_{PS} = 2.7$ V



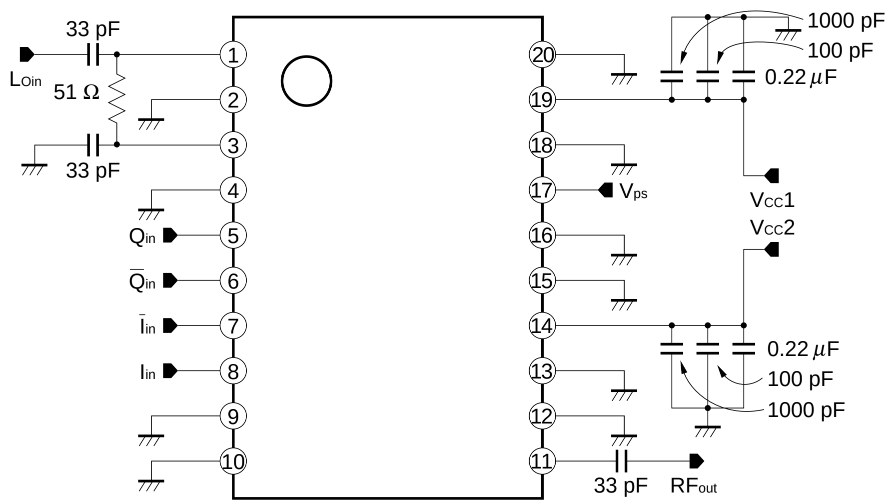
$V_{CC} = V_{PS} = 3.0$ V



$V_{CC} = V_{PS} = 3.6$ V

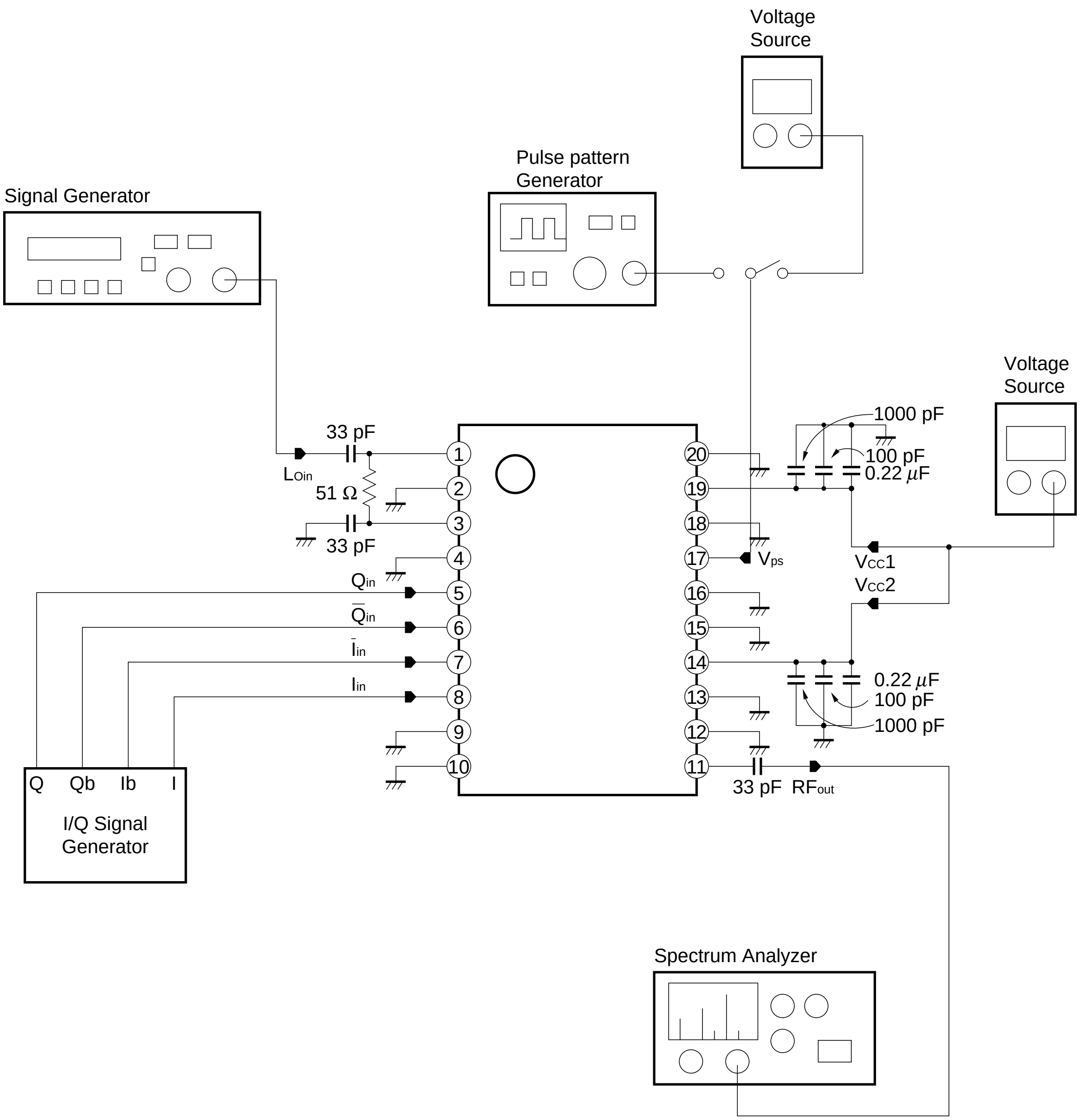


TEST CIRCUIT



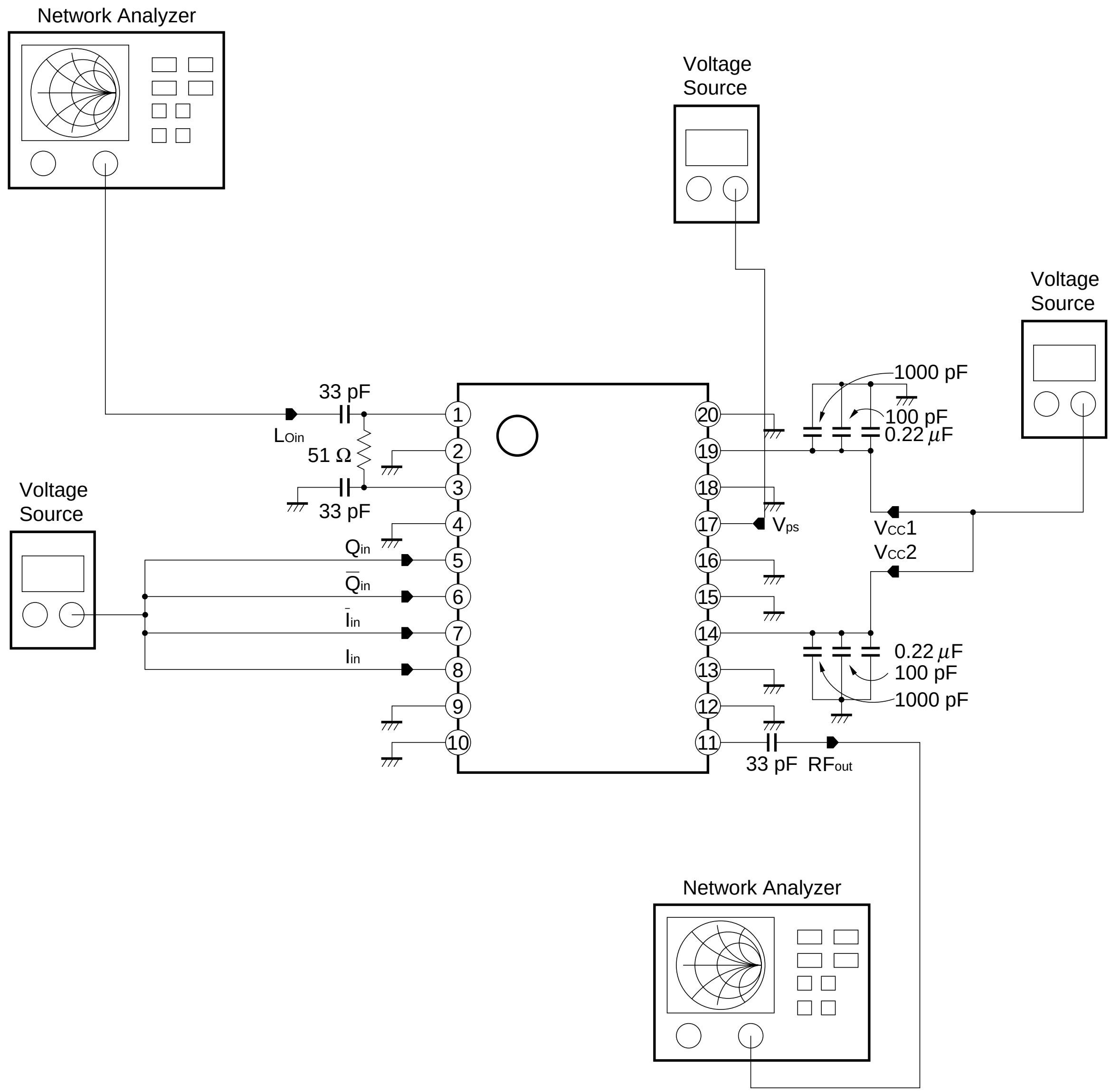
MEASUREMENT BLOCK DIAGRAM 1

(RF Output Power, Local Carrier Leak, Image Rejection, I/Q 3rd Order Intermodulation Distortion and Power Save Rise and Fall Time)

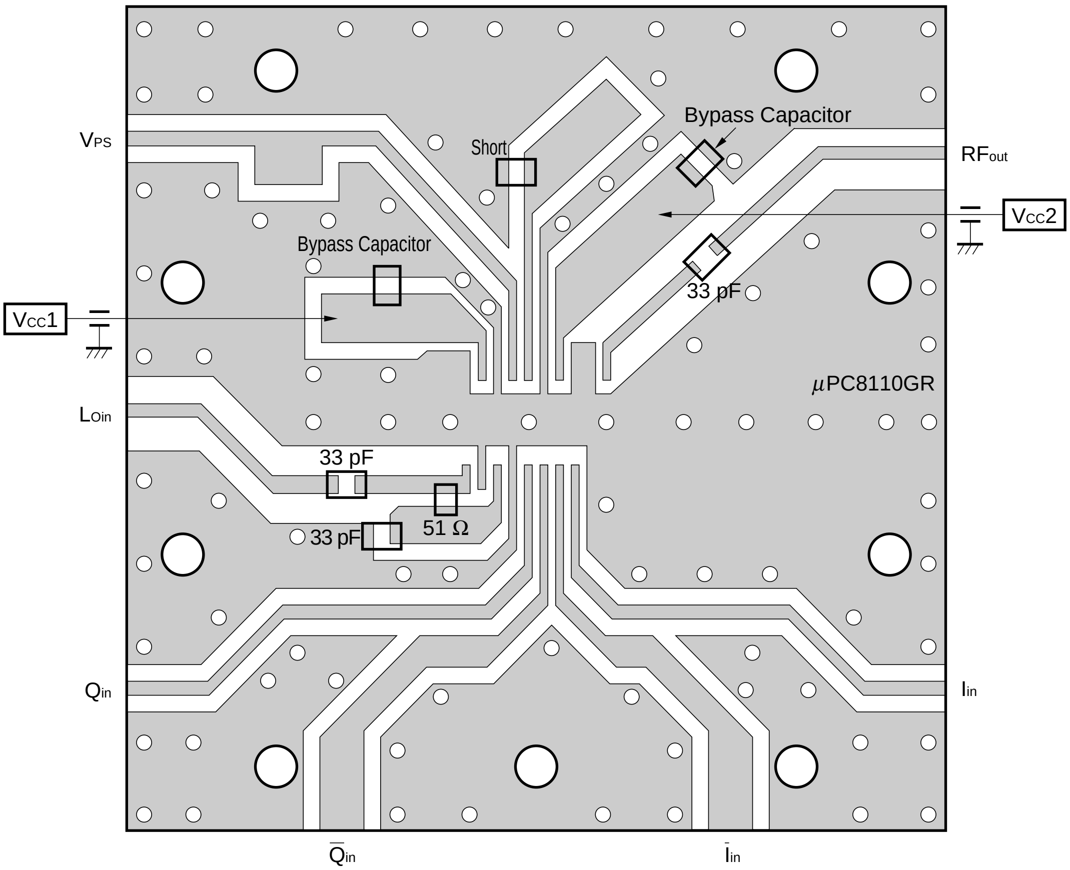


MEASUREMENT BLOCK DIAGRAM 2

(Local Input VSWR and RF Output VSWR)



TEST BOARD



Notes 1. Double-sided patterning with 35 μm thick copper on polyhimid board sizing 50 × 50 × 0.4 mm.

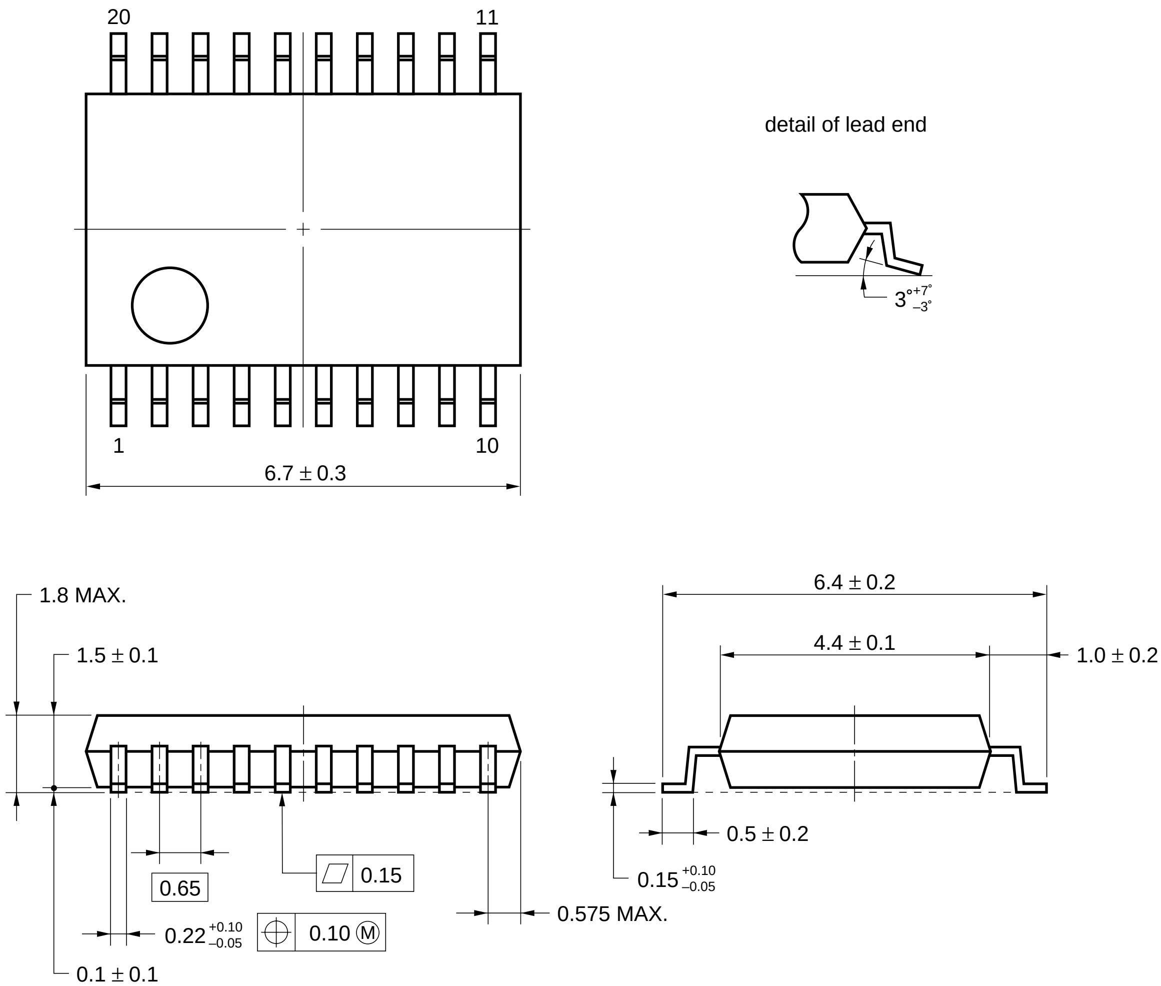
2. GND pattern on backside.

3. Solder coating over patterns.

4. ○, ◯ indicate through-holes.

PACKAGE DIMENSIONS

★ **20 PIN PLASTIC SSOP (225 mil) (UNIT: mm)**



NOTE Each lead centerline is located within 0.10 mm of its true position (T.P.) at maximum material condition.

NOTE ON CORRECT USE

(1) Observe precautions for handling because of electrostatic sensitive devices.
(2) Form a ground pattern as wide as possible to keep the minimum ground impedance (to prevent undesired oscillation).
(3) Keep the track length of the ground pins as short as possible.
(4) Connect a bypass capacitor (e.x. 1 000 pF) to the V_{CC} pin.
(5) $\overline{I}$, $\overline{Q}$ DC offset voltage should be same as the I, Q DC offset voltage (to prevent changing the local leak level with power save control.)

RECOMMENDED SOLDERING CONDITIONS

This product should be soldered in the following recommended conditions. Other soldering method and conditions than the recommended conditions are to be consulted with our sales representatives.

μPC8110GR

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak package's surface temperature: 235 °C or below, Reflow time: 30 seconds or below (210 °C or higher), Number of reflow process: 3, Exposure limit[Note]: None	IR35-00-3
VPS	Peak package's surface temperature: 215 °C or below, Reflow time: 40 seconds or below (200 °C or higher), Number of reflow process: 3, Exposure limit[Note]: None	VP15-00-3
Wave soldering	Solder temperature: 260 °C or below, Flow time: 10 seconds or below, Number of flow process: 1, Exposure limit[Note]: None	WS60-00-1
Partial heating method	Terminal temperature: 300 °C or below, Flow time: 3 seconds/pin or below, Exposure limit[Note]: None	

Note Exposure limit before soldering after dry-pack package is opened.
Storage conditions: 25 °C and relative humidity at 65 % or less.

Caution Apply only a single process at once, except for "Partial heating method".

For details of recommended soldering conditions for surface mounting, refer to information document SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL (C10535E).

[MEMO]

[MEMO]

[MEMO]