NEC

# BIPOLAR ANALOG INTEGRATED CIRCUIT

# μPC2712T

## 2.6 GHz WIDE BAND AMPLIFIER
## SILICON BIPOLAR MONOLITHIC INTEGRATED CIRCUIT

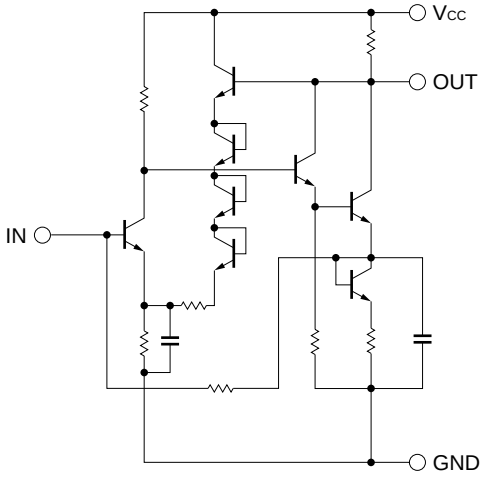
### FEATURES

- High power gain : 20 dB TYP. @ f = 1 GHz
- Excellent frequency response : 2.6 GHz TYP. @ 3 dB down below the gain at 0.1 GHz
- Noise figure : 4.5 dB @ f = 1 GHz
- Single supply voltage : 5 V
- Input and output matching : 50 Ω
- Mini package : 6-pin mini mold

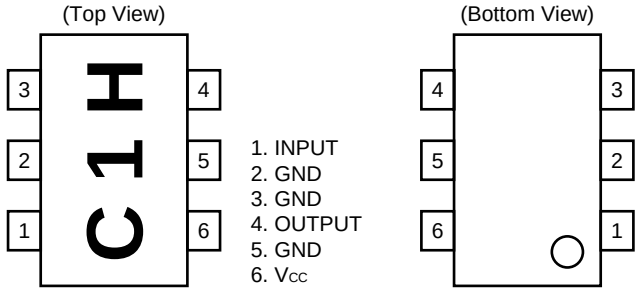
### ORDERING INFORMATION

| PART NUMBER | PACKAGE | SUPPLYING FORM |
|---|---|---|
| μPC2712T-E3 | 6-pin mini mold | Embossed tape 8 mm wide. QTY 3 KP/Reel.<br>Pin 1, 2, 3 face to perforation side of the tape. |

### EQUIVALENT CIRCUIT




### PIN CONNECTIONS




**Caution: Electro-static sensitive devices**

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## ABSOLUTE MAXIMUM RATINGS (Unless otherwise specified, $T_A$ = +25 °C)

| | | | |
|---|---|---|---|
| Supply Voltage | $V_{CC}$ | 6 | V |
| Total Circuit Current | $I_{CC}$ | 30 | mA |
| Power Dissipation | $P_D$ | 280* | mW |
| Operating Ambient Temperature | $T_A$ | –40 to +85 | °C |
| Storage Temperature | $T_{stg}$ | –55 to +150 | °C |
| Input Power | $P_{in}$ | +10 | dBm |

* Mounted on 50 × 50 × 1.6 mm double sided copper clad epoxy glass PWB ($T_A$ = +85 °C)

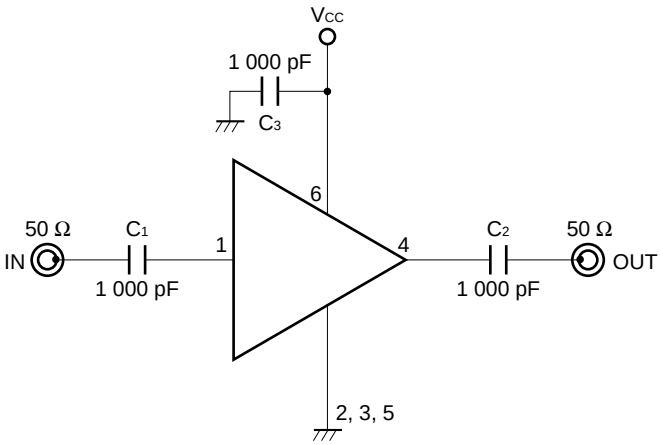
## RECOMMENDED OPERATING CONDITIONS

| PARAMETER | SYMBOL | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | 4.5 | 5.0 | 5.5 | V |

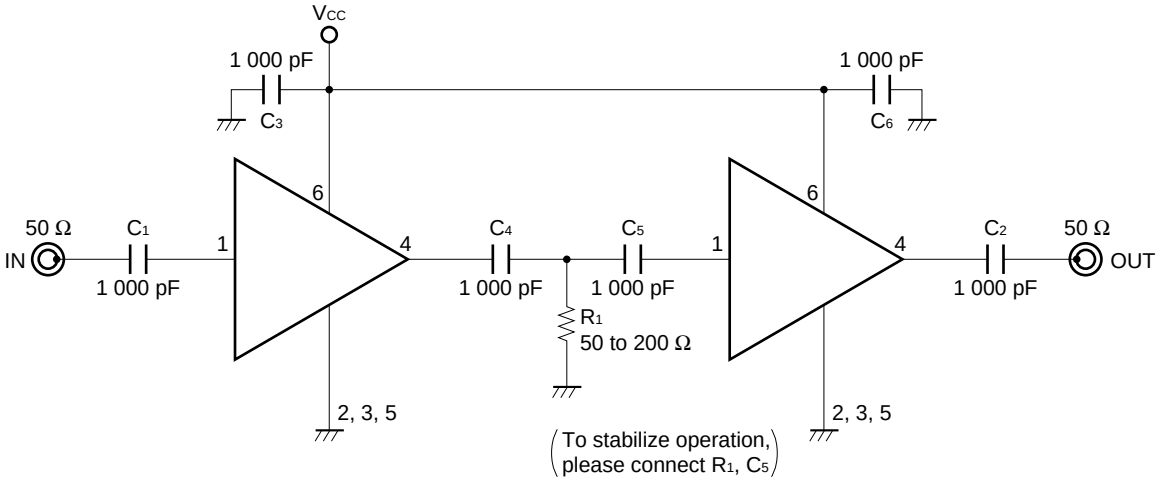
## ELECTRICAL CHARACTERISTICS ($T_A$ = +25 °C, $V_{CC}$ = 5.0 V, $Z_S$ = $Z_L$ = 50 Ω)

| PARAMETERS | SYMBOL | MIN. | TYP. | MAX. | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|
| Circuit Current | $I_{CC}$ | 9 | 12 | 15 | mA | No Signals |
| Power Gain | $G_P$ | 18 | 20 | 23.5 | dB | f = 1 GHz |
| Maximum Output Level | $P_{O(sat)}$ | 0 | +3 | — | dBm | f = 1 GHz, $P_{in}$ = –2 dBm |
| Noise Figure | NF | — | 4.5 | 6 | dB | f = 1 GHz |
| Upper Limit Operating Frequency | $f_u$ | 2.2 | 2.6 | — | GHz | 3 dB down below flat gain at f = 0.1 GHz |
| Isolation | ISL | 28 | 33 | — | dB | f = 1 GHz |
| Input Return Loss | $RL_{in}$ | 9 | 12 | — | dB | f = 1 GHz |
| Output Return Loss | $RL_{out}$ | 10 | 13 | — | dB | f = 1 GHz |
| Gain Flatness | $\Delta G_P$ | — | ±0.8 | — | dB | f = 0.1 to 2.0 GHz |

## TEST CIRCUIT




## EXAMPLE OF APPLICATION CIRCUIT




The application circuits and their parameters are for reference only and are not intended for use in actual design-ins.

**Capacitors for $V_{CC}$, input and output pins**

1 000 pF capacitors are recommendable as bypass capacitor for $V_{CC}$ pin and coupling capacitors for input/output pins.

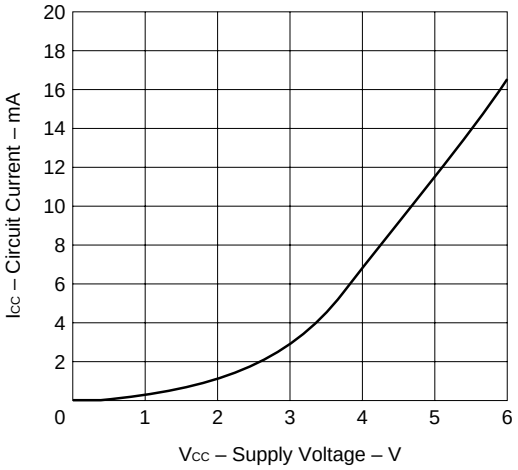
Bypass capacitor for $V_{CC}$ pin is intended to minimize $V_{CC}$ pin's ground impedance. Therefore, stable bias can be supplied against $V_{CC}$ fluctuation.

Coupling capacitors for input/output pins are intended to minimize RF serial impedance and cut DC.

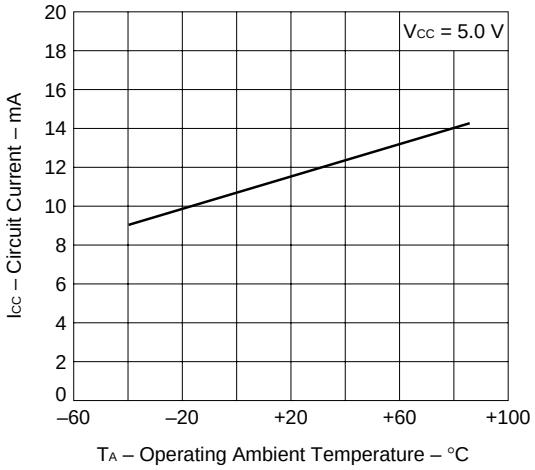
To get flat gain from 100 MHz up, 1 000 pF capacitors are assembled on the test circuit. [Actually, 1 000 pF capacitors give flat gain at least 10 MHz. In the case of under 10 MHz operation, increase the value of coupling capacitor such as 2 200 pF. Because the coupling capacitors are determined by the equation of $C = 1/(2 \pi fZs)$.]

## TYPICAL CHARACTERISTICS ($T_A$ = +25 °C)

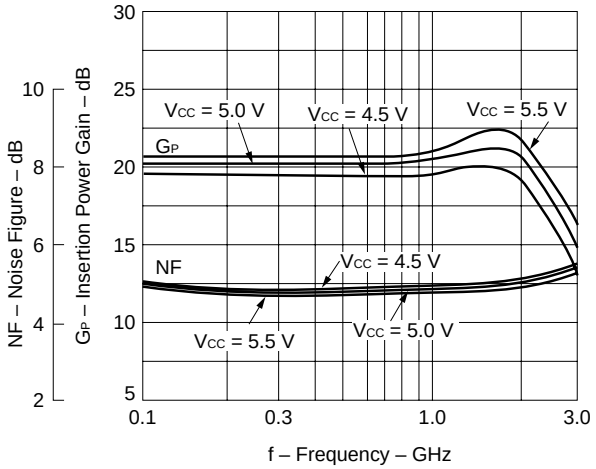
**CIRCUIT CURRENT vs. SUPPLY VOLTAGE**



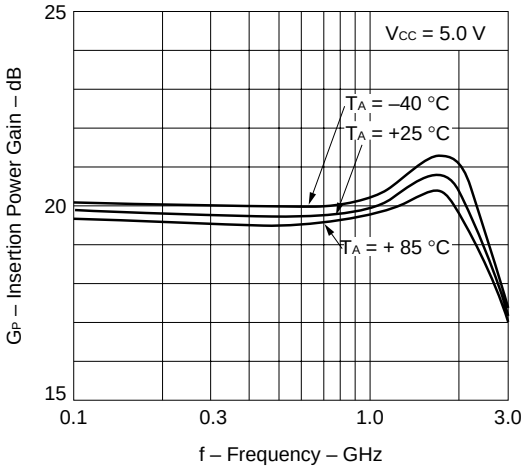

**CIRCUIT CURRENT vs. OPERATING AMBIENT TEMPERATURE**



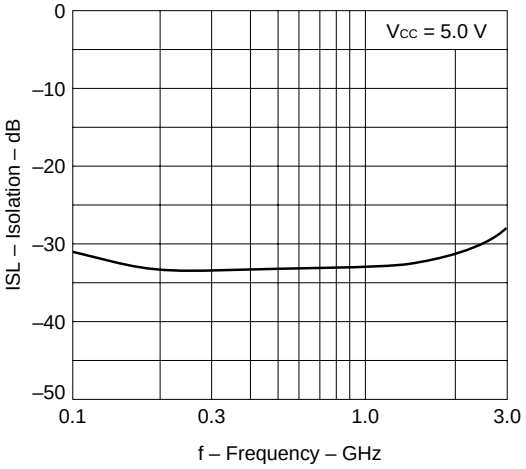

**NOISE FIGURE AND INSERTION POWER GAIN vs. FREQUENCY**



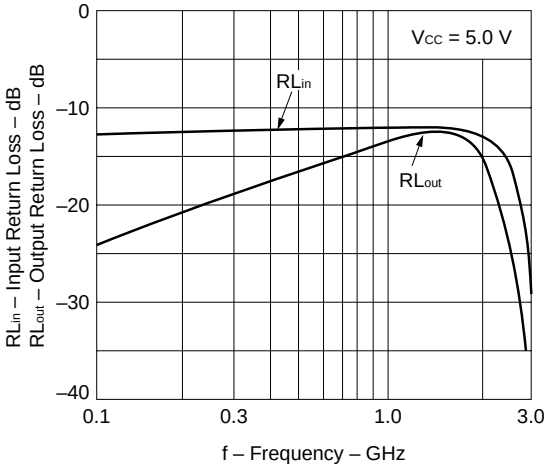

**INSERTION POWER GAIN vs. FREQUENCY**



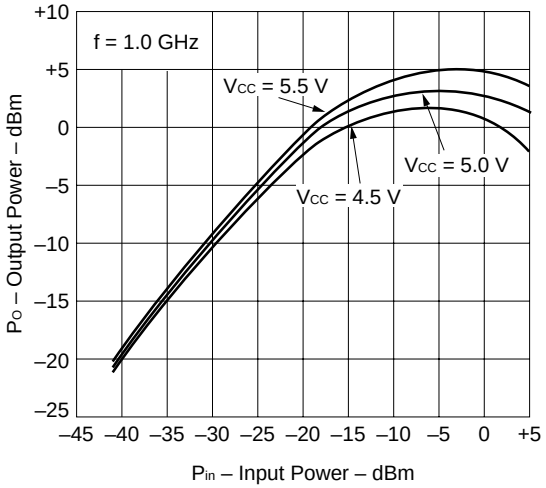

**ISOLATION vs. FREQUENCY**



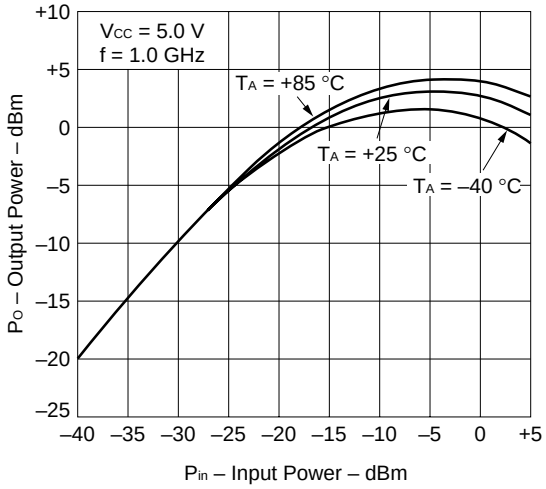

**INPUT RETURN LOSS, OUTPUT RETURN LOSS vs. FREQUENCY**



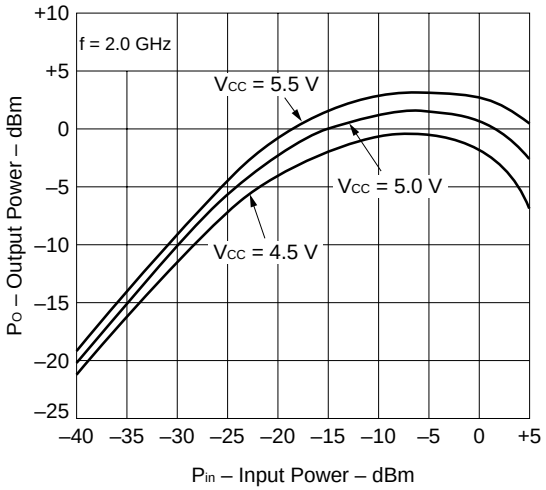
**OUTPUT POWER vs. INPUT POWER**



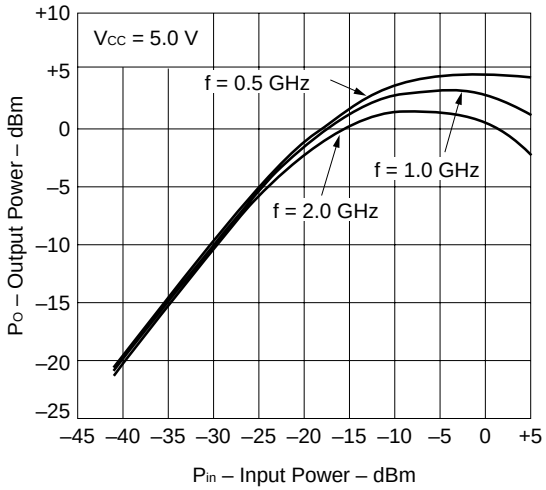

**OUTPUT POWER vs. INPUT POWER**



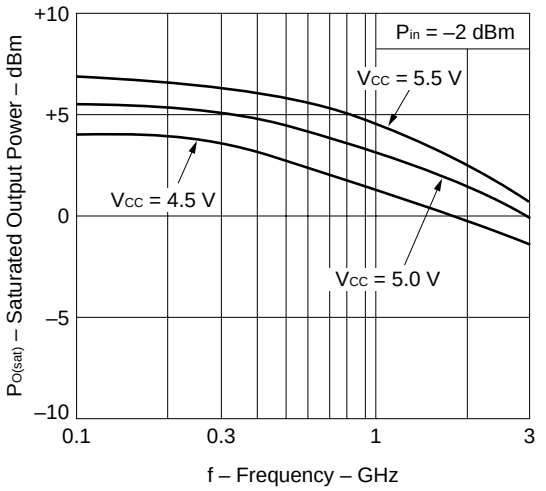

**OUTPUT POWER vs. INPUT POWER**



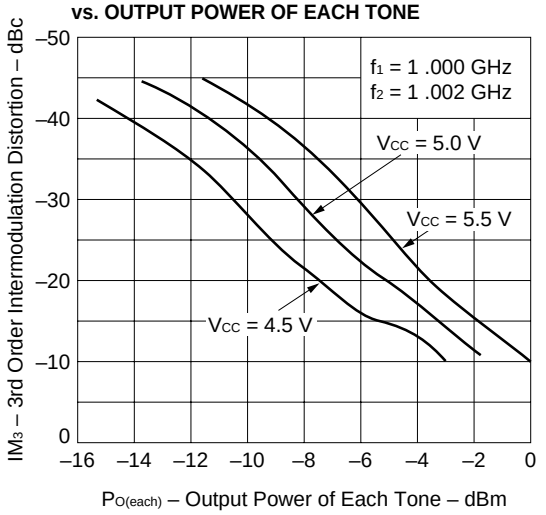

**OUTPUT POWER vs. INPUT POWER**




**SATURATED OUTPUT POWER vs. FREQUENCY**

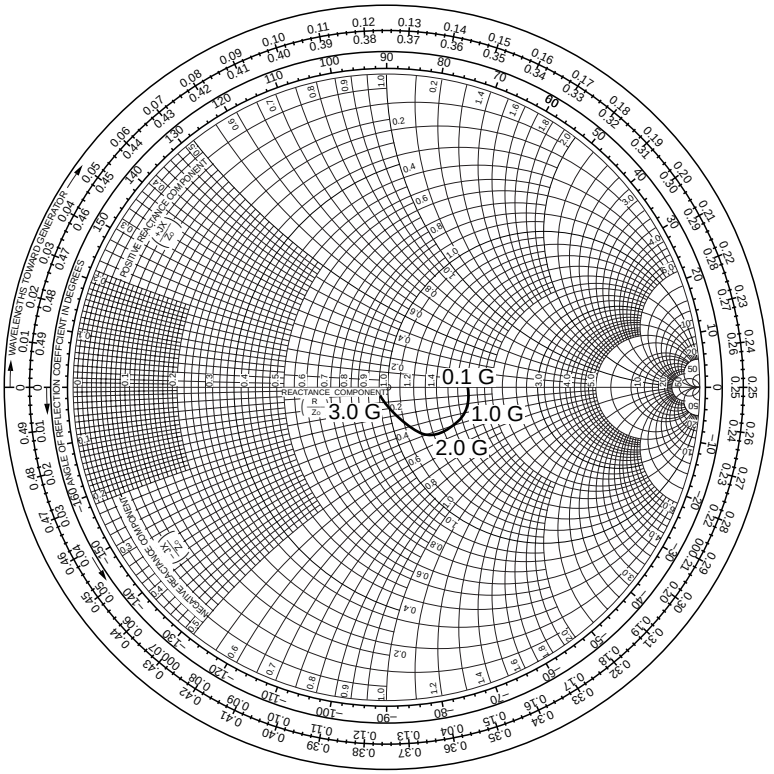



**THIRD ORDER INTERMODULATION DISTORTION vs. OUTPUT POWER OF EACH TONE**



## S-PARAMETER ($V_{CC}$ = 5.0 V)

### $S_{11}$-FREQUENCY




### $S_{22}$-FREQUENCY

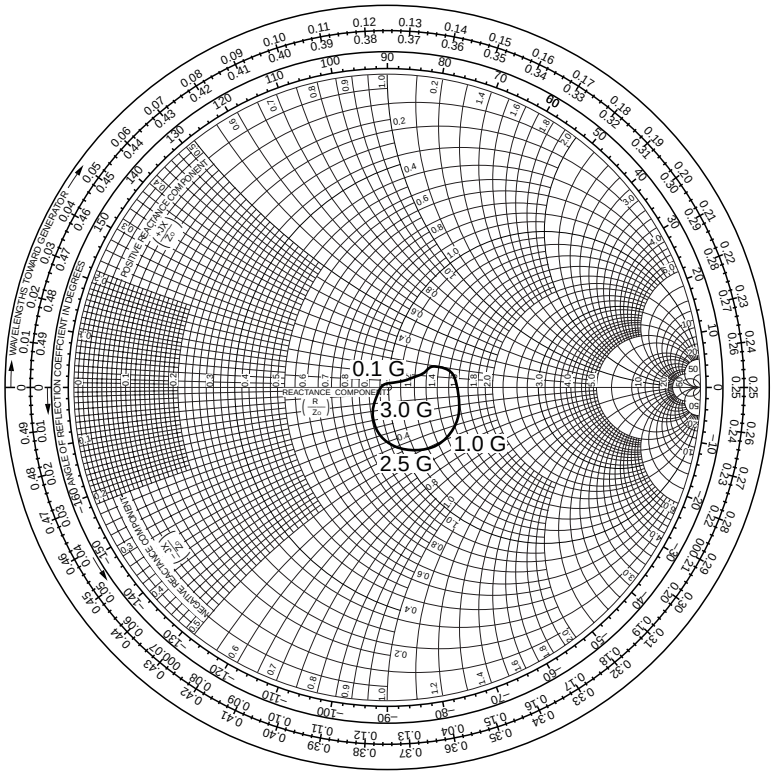
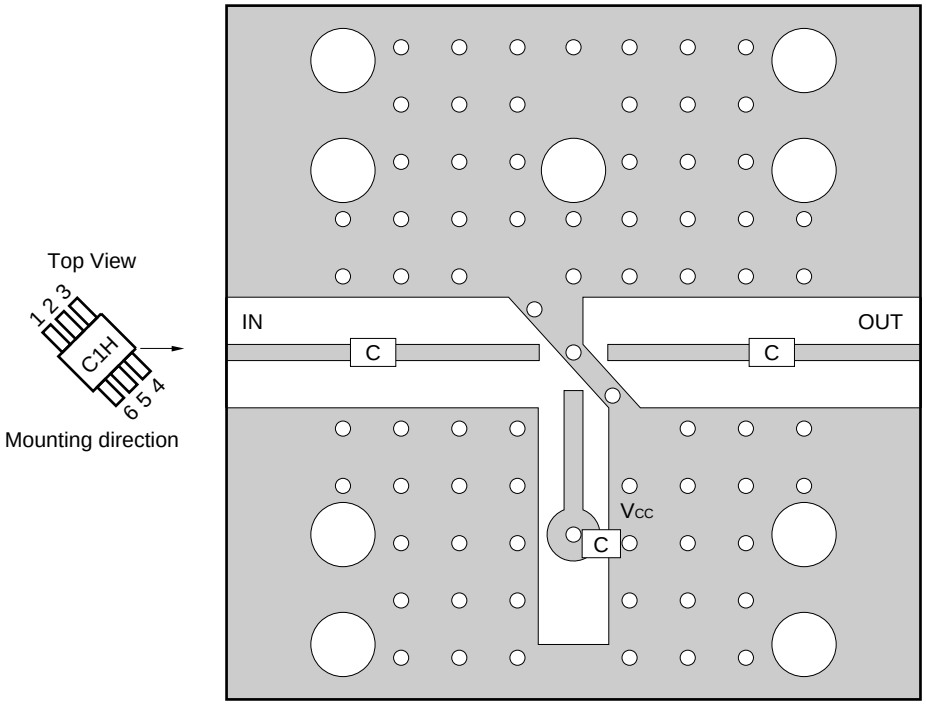


**ILLUSTRATION OF APPLICATION CIRCUIT ASSEMBLED ON EVALUATION BOARD**



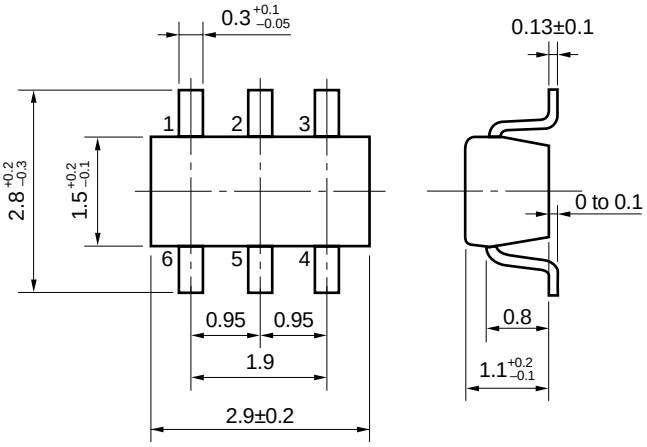

**COMPONENT LIST FOR APPLICATION EXAMPLE**

| | VALUE |
|---|---|
| C | 1 000 pF |

**Note for evaluation board**

1. $30 \times 30 \times 0.4$ mm double copper clad polyimide board
2. Back side: GND pattern
3. Solder plated on pattern
4. ○◯: Through holes

**6 PIN MINI MOLD PACKAGE DIMENSIONS (Unit: mm)**



## NOTE ON CORRECT USE

(1) Observe precautions for handling because of electro-static sensitive devices.
(2) Form a ground pattern as wide as possible to prevent an increase in ground impedance (to prevent undesired oscillation).
(3) Keep the track length of the ground pins as short as possible.
(4) Connect a bypass capacitor (e.g. 1000 pF) to the $V_{CC}$ pin.

## RECOMMENDED SOLDERING CONDITIONS

This product should be soldered in the following recommended conditions. Other soldering methods and conditions than the recommended conditions are to be consulted with our sales representatives.

μPC2712T

| Soldering method | Soldering conditions | Recommended condition symbols |
|---|---|---|
| Infrared ray reflow | Package peak temperature: 235 °C,<br>Hour: within 30 s. (more than 210 °C),<br>Time: 3 time, Limited days; no.*1 | IR35-00-3 |
| VPS | Package peak temperature: 215 °C,<br>Hour: within 40 s. (more than 200 °C),<br>Time: 3 time, Limited days: no.*1 | VP15-00-3 |
| Wave soldering | Soldering tub temperature: less than 260 °C,<br>Hour: within 10 s.<br>Time: 1 time, Limited days: no. | WS60-00-1 |
| Pin part heating | Pin area temperature: less than 300 °C,<br>Hour: within 3 s.<br>Limited days: no.*1 | |

***1** It is the storage days after opening a dry pack, the storage conditions are 25 °C, less than 65 % RH.

**Caution The combined use of soldering method is to be avoided (However, except the pin area heating method).**

For details of recommended soldering conditions for surface mounting, refer to information document SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL (C10535E).

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