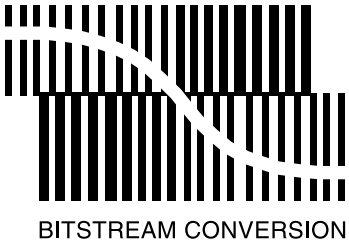
DATA SHEET



UDA1343TT
Economy audio CODEC with features

Preliminary specification
File under Integrated Circuits, IC01

2000 Jan 12

Philips
Semiconductors

PHILIPS

Economy audio CODEC with features UDA1343TT

FEATURES

General

- Low power consumption
- 2.4 V to 3.6 V power supply range, with 3 V typical
- 5 V tolerant TTL compatible digital inputs
- 256, 384 and 512f_s system clock
- Supports sampling frequencies from 8 to 110 kHz
- Non-inverting ADC plus integrated high-pass filter to cancel DC offset
- The ADC supports 2 V (RMS) input signals
- Stereo PGA with 0 to 24 dB gain in 3 dB steps
- Overload detector for easy record level control
- Separate power control for ADC + PGA and DAC
- Integrated digital interpolation filter plus non-inverting DAC
- Functions controllable by L3 microcontroller interface
- Small package size (TSSOP28)
- ADC and DAC output polarity can be set.

Multiple format input interface

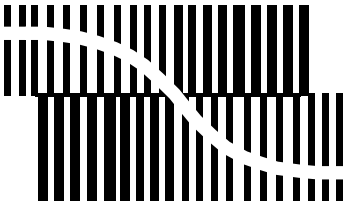
- I^2S-bus, MSB-justified up to 24 bits and LSB-justified 16, 18, 20 and 24 bits format compatible
- Four combined data formats with MSB data output and LSB 16, 18, 20 and 24 bits data input
- 1f_s input and output format data rate.

DAC digital sound processing

- Digital dB-linear volume control (low microcontroller load) via L3 microcontroller in 0.25 dB steps
- Digital de-emphasis for 32, 44.1, 48 and 96 kHz
- Cosine roll-soft mute.

Advanced audio configuration

- Stereo single-ended input configuration
- Stereo line output (under microcontroller volume control), no post filter required



BITSTREAM CONVERSION

- High linearity, dynamic range and low distortion
- Digital silence detector
- Digital mixer for mixing ADC signal and playback signal
- ADC volume control in 0.25 dB steps and cosine roll-off mute.

APPLICATIONS

- Portable equipment which includes audio functions
- Digital video camera.

GENERAL DESCRIPTION

The UDA1343TT is a single-chip stereo Analog-to-Digital Converter (ADC) and Digital-to-Analog Converter (DAC) with basic signal processing features employing bitstream conversion techniques. The low power consumption, the small package size and low voltage requirements make the device eminently suitable for use in low-voltage low-power portable digital audio equipment which incorporates recording and playback functions.

The UDA1343TT is equipped with a digital mixer for mixing the ADC signal directly to the playback signal (for example for Karaoke applications). In the mixing mode the ADC output signal can be output before or after the mixer.

The mixer can also be used as a selector to select between the ADC or the digital data being played back at the DAC.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UDA1343TT	TSSOP28	plastic shrink small outline package; 28 leads; body width 4.4 mm	SOT361-1

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
$V_{DDA(ADC)}$	ADC analog supply voltage		2.4	3.0	3.6	V
$V_{DDA(DAC)}$	DAC analog supply voltage		2.4	3.0	3.6	V
V_{DDD}	digital supply voltage		2.4	3.0	3.6	V
$I_{DDA(ADC)}$	ADC analog supply current	operating mode	–	10	–	mA
		ADC power-down	–	100	–	µA
$I_{DDA(DAC)}$	DAC analog supply current	operating mode	–	4	–	mA
		DAC power-down	–	50	–	µA
$I_{DDO(DAC)}$	DAC operational amplifier supply current	operating mode	–	2.5	–	mA
		DAC power-down	–	200	–	µA
I_{DDD}	digital supply current	operating mode	–	5	–	mA
		ADC plus DAC power-down	–	300	–	µA
T_{amb}	ambient temperature		–40	–	+85	°C
Analog-to-digital converter						
$V_{i(rms)}$	input voltage (RMS value)	notes 1, 2 and 3	–	1.0	–	V
(THD + N)/S	total harmonic distortion-plus-noise to signal ratio	at 0 dB				
		f_s = 44.1 kHz	–	–85	–	dB
		f_s = 96 kHz	–	–81	–	dB
		at –60 dB; A-weighted				
		f_s = 44.1 kHz	–	–37	–	dB
		f_s = 96 kHz	–	–35	–	dB
S/N	signal-to-noise ratio	V_i = 0 V; A-weighted				
		f_s = 44.1 kHz	–	97	–	dB
		f_s = 96 kHz	–	95	–	dB
α_{cs}	channel separation		–	100	–	dB
Digital-to-analog converter						
$V_{o(rms)}$	output voltage (RMS value)		–	900	–	mV
(THD + N)/S	total harmonic distortion-plus-noise to signal ratio	at 0 dB				
		f_s = 44.1 kHz	–	–85	–	dB
		f_s = 96 kHz	–	–80	–	dB
		at –60 dB; A-weighted				
		f_s = 44.1 kHz	–	–37	–	dB
		f_s = 96 kHz	–	–35	–	dB
α_{cs}	channel separation		–	100	–	dB
S/N	signal-to-noise ratio	code = 0; A-weighted				
		f_s = 44.1 kHz	–	100	–	dB
		f_s = 96 kHz	–	98	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Power performance						
P_{ADDA}	power consumption in record and playback mode		–	64	–	mW
P_{DA}	power consumption in playback mode		–	36	–	mW
P_{AD}	power consumption in record mode		–	46	–	mW
P_{PD}	power consumption in power-down mode		–	2.0	–	mW

Notes

1. The input voltage can be up to 2 V (RMS) when the current through the ADC input pin is limited to approximately 1 mA by using a series resistor.
2. The input voltage to the ADC scales proportionally with the power supply.
3. The performance figures and input voltage of the ADC are given with the PGA gain set to 0 dB.

BLOCK DIAGRAM

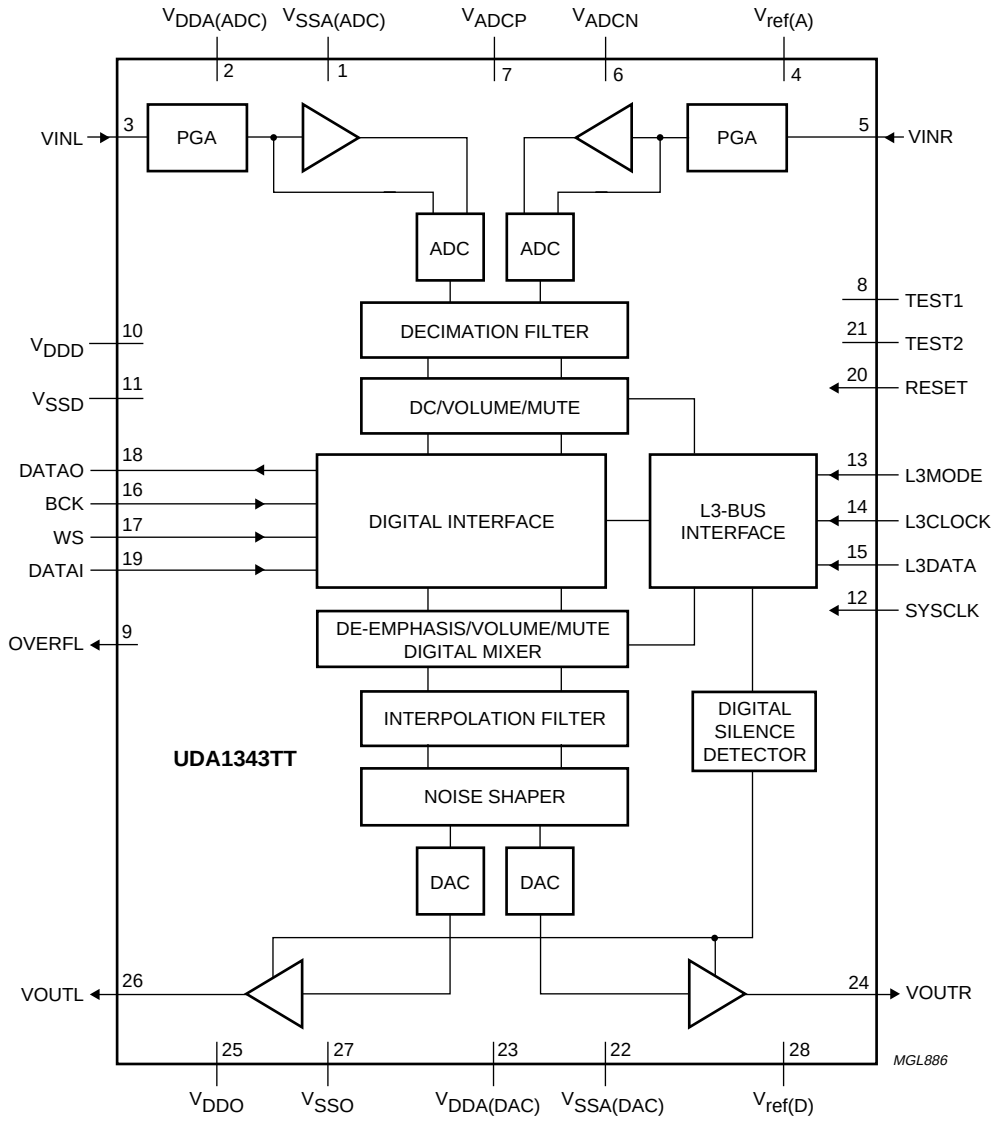


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	TYPE	DESCRIPTION
$V_{SSA(ADC)}$	1	analog ground pad	ADC analog ground
$V_{DDA(ADC)}$	2	analog supply pad	ADC analog supply voltage
VINL	3	analog input pad	ADC input left
$V_{ref(A)}$	4	analog pad	ADC reference voltage
VINR	5	analog input pad	ADC input right
V_{ADCN}	6	analog pad	ADC negative reference voltage
V_{ADCP}	7	analog pad	ADC positive reference voltage
TEST1	8	5 V tolerant digital input pad with internal pull-down pad	test pin 1
OVERFL	9	5 V tolerant slew-rate controlled digital output pad	ADC overload output
V_{DDD}	10	digital supply pad	digital supply voltage
V_{SSD}	11	digital ground pad	digital ground
SYSCLK	12	5 V tolerant digital Schmitt triggered input pad	system clock input 256, 384 or 512f_s
L3MODE	13	digital input pad	L3MODE input
L3CLOCK	14	5 V tolerant digital Schmitt triggered input pad	L3CLOCK input
L3DATA	15	5 V tolerant digital Schmitt triggered input with pull down, slew rate controlled output pad	L3DATA input
BCK	16	5 V tolerant digital Schmitt triggered input pad	bit clock input
WS	17	5 V tolerant digital Schmitt triggered input pad	word select input
DATAO	18	5 V tolerant slew-rate controlled digital output pad	data output
DATAI	19	5 V tolerant digital Schmitt triggered input pad	data input
RESET	20	5 V tolerant digital Schmitt triggered input pad with internal pull down	reset input
TEST2	21	5 V tolerant digital input pad with internal pull-down pad	test pin 2
$V_{SSA(DAC)}$	22	analog ground pad	DAC analog ground
$V_{DDA(DAC)}$	23	analog supply pad	DAC analog supply voltage
VOUTR	24	analog output pad	DAC output right
V_{DDO}	25	analog supply pad	operational amplifier supply voltage
VOUTL	26	analog output pad	DAC output left
V_{SSO}	27	analog ground pad	operational amplifier ground
$V_{ref(D)}$	28	analog pad	DAC reference voltage

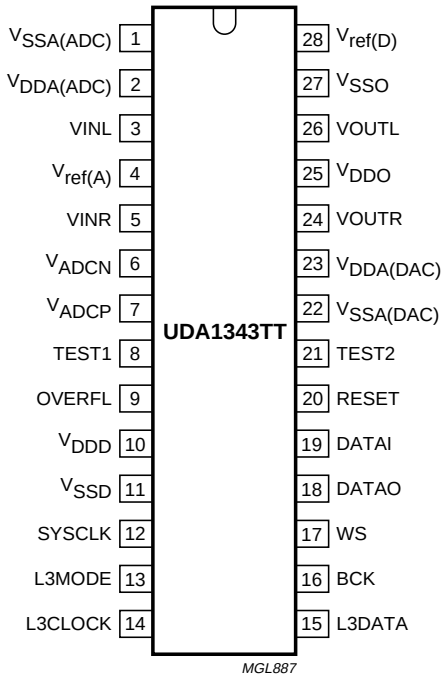


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The UDA1343TT accommodates slave mode only, this means that in all applications the system devices must provide the system clock and the serial audio clock signals.

The system clock must be locked in frequency to the digital interface input signals.

The BCK clock can be up to $128f_s$, or in other words the BCK frequency f_{BCK} is 128 times the Word Select (WS) frequency f_{WS} or less: $f_{BCK} = < 128 \times f_{WS}$.

Important: the WS edge MUST fall on the negative edge of the BCK at all times for correct operation of the digital I/O data interface.

Note: the sampling frequency range is from 8 to 110 kHz, however for the $512f_s$ clock mode the sampling range is from 8 to 55 kHz.

Reset

Pin 20 is a reset pin (active HIGH), which resets the internal digital core of the IC and also resets all feature values of the L3 interface to their default settings as given in Tables 8 and 9.

Since the RESET pin is a pull-down pad with Schmitt-trigger, a Power-On Reset (POR) function can be made by connecting this pin to the digital power supply via a capacitor.

Note: care must be taken that during the HIGH period of the reset signal it is best to have at least 8 SYSCLK clock cycles to properly reset the device.

Analog-to-Digital Converter (ADC)

The stereo ADC of the UDA1343TT consists of two 5th-order Sigma-Delta modulators. They have a modified Ritchie-coder architecture in a differential switched capacitor implementation. The oversampling ratio is 64.

Analog front-end

The analog front-end is equipped with a Programmable Gain Amplifier (PGA) which can be controlled via the L3 interface. The control range is from 0 dB to 24 dB gain in 3 dB steps independant for left and right.

In applications in which a 2 V (RMS) input signal is used, a 12 kΩ resistor must be connected in series with the input of the ADC. This makes a voltage divider with the internal ADC resistor and makes sure only 1 V (RMS) maximum is input to the IC. Using this application for a 2 V (RMS) input signal, the switch must be set to 0 dB. When a 1 V (RMS) input signal is input to the ADC in the same application, the gain switch of the PGA must be set to 6 dB via the L3 interface.

An overview of the maximum input voltages allowed against the presence of an external resistor and the setting of the gain switch is given in Table 1.

Table 1 Application modes using input gain stage

RESISTOR (12 kΩ)	PGA GAIN	MAXIMUM INPUT VOLTAGE
Present	0 dB	2 V (RMS)
Present	6 dB	1 V (RMS)
Absent	0 dB	1 V (RMS)
Absent	6 dB	0.5 V (RMS)

Decimation filter (ADC)

The decimation from $64f_s$ to $1f_s$ is performed in two stages.

The first stage realizes a 4th-order $\frac{\sin x}{x}$ characteristic.

This filter decreases the sample rate by 16. The second stage consists of 2 half-band filters and a recursive filter, each decimating by a factor of 2.

Table 2 Digital decimation filter characteristics

ITEM	CONDITIONS	VALUE (dB)
Pass-band ripple	$0 - 0.45f_s$	±0.05
Stop band	$>0.55f_s$	–50
Dynamic range	$0 - 0.45f_s$	114
Overall gain with 0 dB input to the ADC	DC	–1.16

In the ADC path there is a volume control with a range of 0 dB to –66 dB and –∞ dB in 0.25 dB steps, and a cosine roll-off soft mute.

Note: it should be noted that the digital output level is inversely proportional to the ADC analog power supply. This means that with a constant analog input level and increasing analog power supply, the digital output level will decrease proportionally.

Overload detection (ADC)

In practice the output is used to indicate whenever the output data, in either the left or right channel, is larger than –1 dB (the actual figure is –1.16 dB) of the maximum possible digital swing. When this condition is detected the OVERFL output (pin 9) is forced HIGH for at least $512f_s$ cycles (11.6 ms at f_s = 44.1 kHz). This time-out is reset for each infringement.

Interpolation filter (DAC)

The digital filter interpolates from 1 to $128f_s$ by means of a cascade of a recursive filter and an FIR filter.

Table 3 Digital interpolation filter characteristics

ITEM	CONDITIONS	VALUE (dB)
Pass-band ripple	$0 - 0.45f_s$	±0.03
Stop band	$>0.55f_s$	–65
Dynamic range	$0 - 0.45f_s$	116.5
Gain	DC	–3.5

Digital silence detector

The UDA1343 is equipped with a digital silence detector on the digital data input. This detects whether a certain amount of consecutive samples are 0. The status of the digital silence detector can be read from the microcontroller interface.

The number of samples can be set via the L3 interface to 3200, 4800, 9600 or 19600 samples.

Mute

Muting the DAC will result in a cosine roll-off soft mute, using $32 \times 4 = 128$ samples (at 44.1 kHz this is 3 ms). The cosine roll-off curve is illustrated in Fig.3.

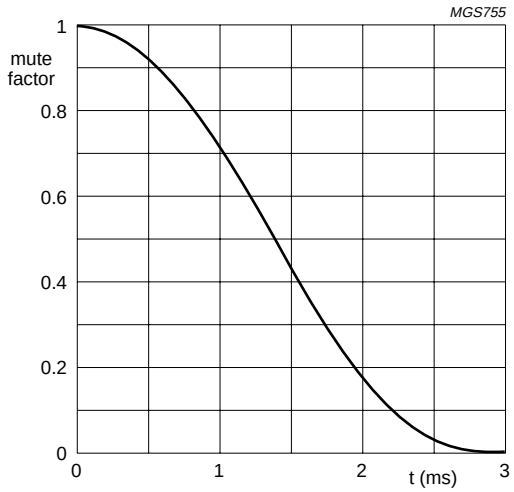


Fig.3 Mute as a function of raised cosine roll-off.

Double speed

SInce the device supports a sampling range of 8 to 110 kHz, the device can support double speed (e.g. for 44.1 kHz and 48 kHz) by just doubling the system speed. In double speed all features are available.

Digital mixer

The UDA1343TT has a digital mixer which can mix the ADC signal to the playback signal. A functional block diagram of the mixer mode is given in Fig.4.

When the device is in mixer mode, care is taken to avoid clipping. This is done by reducing both signals by –6 dB before mixing. After mixing there is master volume and mute, after which the signal is reamplified digitally by 6 dB.

The codec can be set to mixer mode via the L3 interface by setting the MIX bit HIGH.

In the mixer mode there are 3 volume and mute controls available; one for the ADC channel, one for the playback channel and one for the master (equal sum) signal. All three volume ranges can be controlled in 0.25 dB steps.

In the mixer mode, the ADC volume control is used for mixing purposes. The decimator output signal can be output from the chip before the ADC volume control or after the ADC volume control. This can be set via the L3 interface using the ADC output select bit.

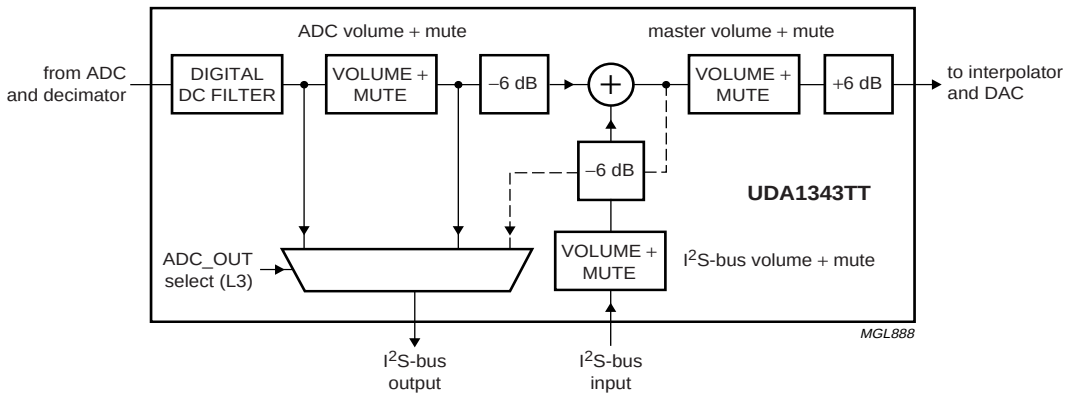


Fig.4 Mixing feature in the UDA1343TT.

Digital output signal

The output to the digital output of the UDA1343TT can be selected from 3 positions, using the two bits ADC_OUT select in the L3 microcontroller interface. The 3 positions are as follows:

- Directly from the ADC and decimator (default)
- After volume control and mute in the ADC data path
- After the digital mixer and before master volume control and mute. It should be noted that this output is before the +6 dB gain. This is done in order to prevent clipping at the mixer output at all times.

Noise shaper (DAC)

The 3rd-order noise shaper operates at $128f_s$. It shifts in-band quantization noise to frequencies well above the audio band. This noise shaping technique enables high signal-to-noise ratios to be achieved. The noise shaper output is converted into an analog signal using a Filter Stream Digital-to-Analog Converter (FSDAC).

The Filter Stream DAC (FSDAC)

The FSDAC is a semi-digital reconstruction filter that converts the 1-bit data stream of the noise shaper to an analog output voltage. The filter coefficients are implemented as current sources and are summed at virtual ground of the output operational amplifier.

In this way very high signal-to-noise performance and low clock jitter sensitivity is achieved. A post-filter is not needed due to the inherent filter function of the DAC. On-board amplifiers convert the FSDAC output current to an output voltage signal capable of driving a line output.

The output voltage of the FSDAC scales proportionally with the power supply voltage.

Multiple format input/output audio interface

The digital audio interface supports multiple standards:

- I^2S-bus with data word length of up to 24 bits
- MSB-justified serial format with data word length of up to 24 bits
- LSB-justified data formats with word lengths of 16, 18, 20 and 24 bits.
- Four combined data formats with MSB data output and 16, 18, 20 and 24 LSB data input.

The digital audio interface formats are illustrated in Fig.5.

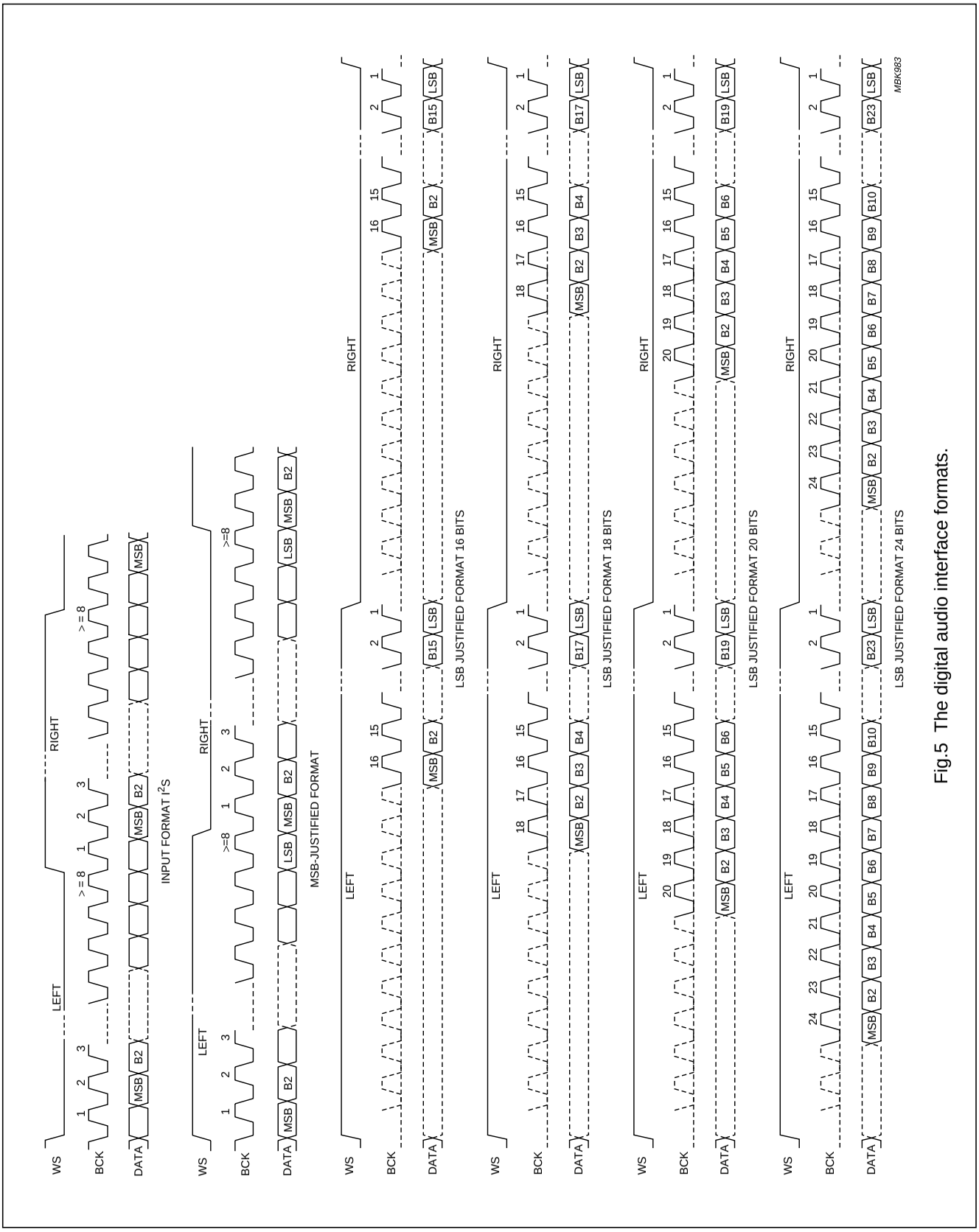


Fig.5 The digital audio interface formats.

L3 INTERFACE

Introduction

The UDA1343TT has a microcontroller input mode. In the microcontroller mode, all the digital sound processing features and the system controlling features can be controlled by the microcontroller. The controllable features are:

- System clock frequency
- Data input format
- Power control
- DC filtering
- De-emphasis
- Volume: master volume, I^2S-bus mixer volume and ADC volume
- Mute: master mute, I^2S-bus mute and ADC mute
- Mixer settings
- PGA gain settings
- Digital silence control settings
- Polarity settings of the ADC and the DAC.

The exchange of data and control information between the microcontroller and the UDA1343TT is accomplished through a serial hardware interface comprising the following pins:

- L3DATA: microcontroller interface data line
- L3MODE: microcontroller interface mode line
- L3CLOCK: microcontroller interface clock line.

Information transfer via the microcontroller bus is organized LSB first, and in accordance with the so called ‘L3’ format, in which two different modes of operation can be distinguished; address mode and data transfer mode (see Fig 6).

Important: when the device is powered-up, at least one L3CLOCK pulse must be sent to the L3 interface to wake-up the interface prior to sending to the device. This is only needed once after the device is powered-up.

Device addressing

The device addressing mode is used to select a device for subsequent data transfer. The address mode is characterized by L3MODE being LOW and a burst of 8 pulses on L3CLOCK, accompanied by 8 bits.
The fundamental timing is illustrated in Fig.6.

Basically, 2 types of transfer can be defined; data transfer to the device and data transfer from the device; see Table 4.

Table 4 Selection of data transfer

DOM BIT 1	DOM BIT 0	TRANSFER
0	0	not used
0	1	not used
1	0	DATA and STATUS write or pre-read
1	1	DATA and STATUS read

As can be seen in Table 4, the DATA and STATUS read and write actions are combined.

The device address consists of one byte, which is split up into two parts:

- Bits 7 to 2 represent a 6-bit device address
- Bits 1 and 0 represent the type of data transfer according to Table 4.

As can be seen in Table 4, there are two types of data transfers, being DATA and STATUS which can be read and written.

Register addressing

After sending the device address, including the flags (the DOM bits) whether the information is read or written, one byte is sent with the destination register address using 7 bits, and 1 bit which signals whether information will be read or written. The fundamental timing for the data mode is illustrated in Fig.7.

Basically there are 3 cases for register addressing:

1. Register addressing for L3 write: the first bit is at logic 0 indicating a write action to the destination register, and is followed by 7 register address bits.
2. Prepare read addressing: the first bit of the byte is at logic 1, signalling data will be read from the register indicated.
3. The read action itself: in this case the device returns a register address prior to sending data from that register. When the first bit of the byte is at logic 0, the register address is valid, if the first bit is at logic 1 the register address is invalid.

Data write mode

For writing data to a device four bytes must be sent. The data write mode is illustrated in Fig.8.

1. One byte with the device address including ‘01’ for signalling write to the device.
2. One byte starting with a logic 0 for signalling write followed by 7 bits indicating the destination address.
3. Two data bytes.

Notes:

1. Each time a new destination address needs to be written, the device address must sent again.
2. When addressing the device for the first time after power-up of the device, at least one L3 clock cycle must be sent to enable the L3 interface.

Data read mode

For reading from the device, a prepare-read must first be done. After the prepare-read, the device address is sent again. The device then returns with the register address, indicating whether the address was valid or not, and the data of the register. This procedure is explained below, and an example transmission is illustrated in Fig.9.

1. One byte with the device address including ‘01’ for signalling write to the address.
2. One byte is sent with the register address which needs to be read. This byte starts with a logic 1, which indicated that there will be a read action from the register.
3. One byte with the device address including ‘11’ is sent to the device. The ‘11’ indicates that the device must write data to the microcontroller.
4. The device now writes the requested register address to the bus, indicating whether the requested register was valid or not (logic 0 means valid, logic 1 means invalid).
5. The device writes the data from the requested register to the bus (two bytes).

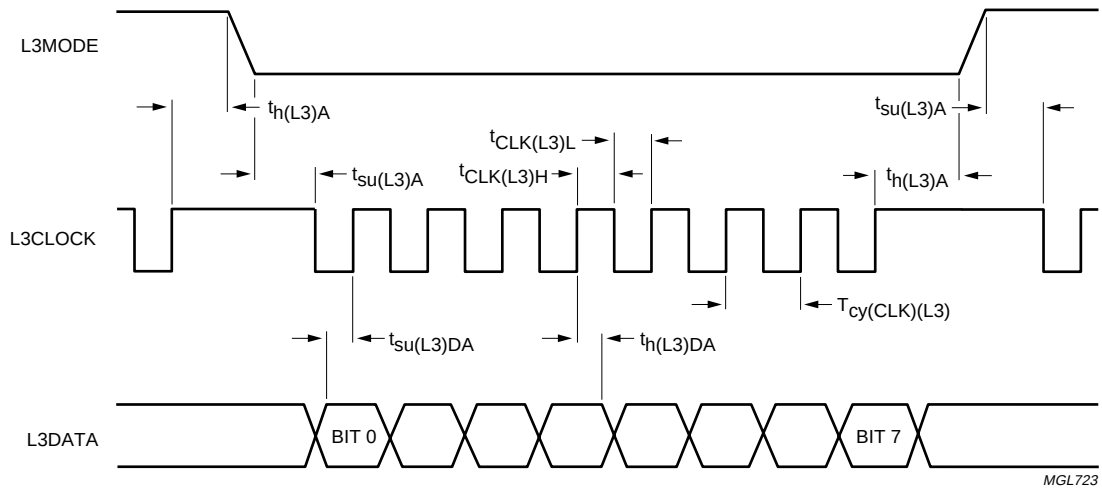


Fig.6 Timing address mode.

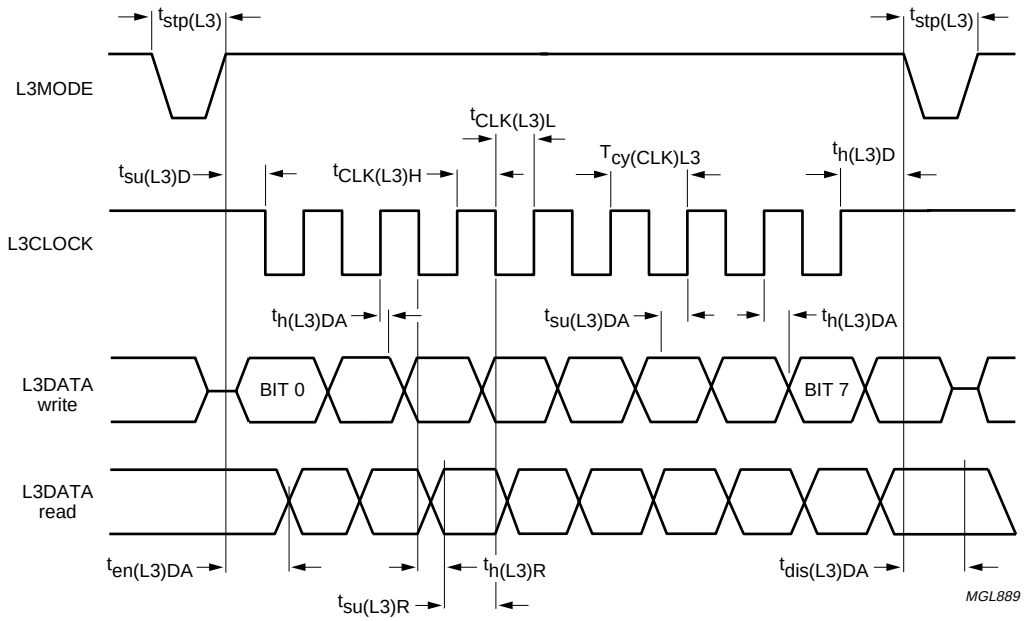


Fig.7 Data write and read mode timing.

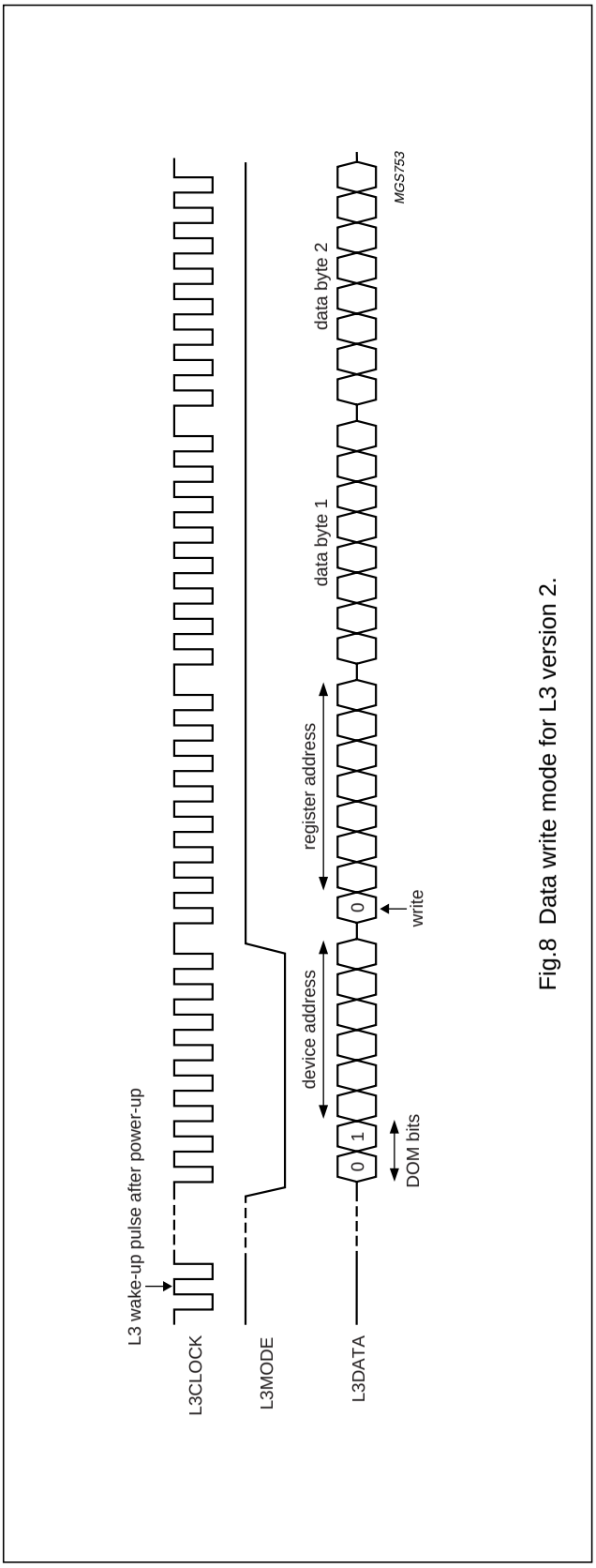


Fig.8 Data write mode for L3 version 2.

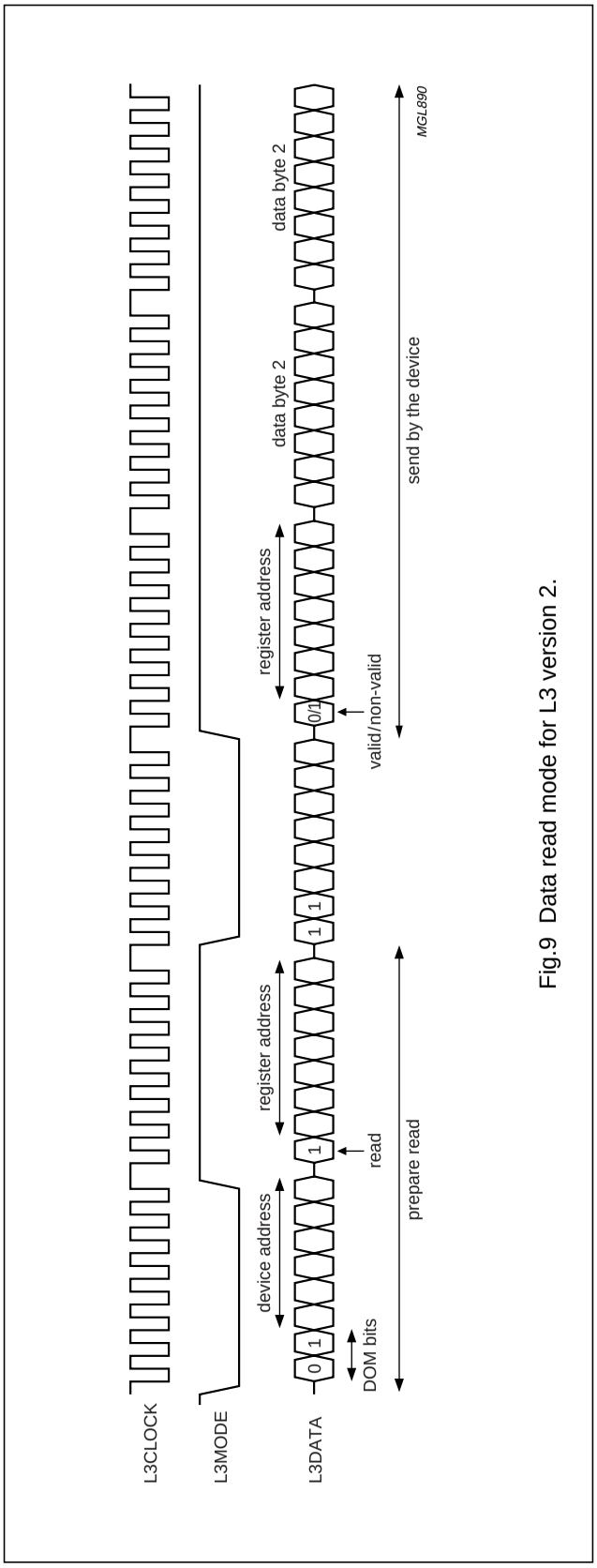


Fig.9 Data read mode for L3 version 2.

L3 protocol

WARNING
Write followed by read When issuing a read command following a write command, at least 8 μs delay must be inserted to allow the write to take effect. No further restrictions apply to the order of L3 read and write commands.

Table 5 L3 data WRITE

MODE	DATA	FIRST IN TIME					LATEST IN TIME		
		BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
Addressing mode	device address	0	1	1	1	1	0	0	0
Data transfer 1	register address	0 (write)	A6	A5	A4	A3	A2	A1	A0
Data transfer 2	MS data byte	D15	D14	D13	D12	D11	D10	D9	D8
Data transfer 3	LS data byte	D7	D6	D5	D4	D3	D2	D1	D0

Table 6 L3 prepare READ DATA

MODE	DATA	FIRST IN TIME					LATEST IN TIME		
		BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
Addressing mode	device address	0	1	1	1	1	0	0	0
Data transfer 1	register address	1 (read)	A6	A5	A4	A3	A2	A1	A0

Table 7 L3 READ DATA

MODE	DATA	FIRST IN TIME					LATEST IN TIME		
		BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
Addressing mode	device address	1	1	1	1	1	0	0	0
Data transfer 1	register address	0 = valid 1 = invalid	A6	A5	A4	A3	A2	A1	A0
Data transfer 2	MS data byte	D15	S14	D13	D12	D11	D10	D9	D8
Data transfer 3	LS data byte	D7	D6	D5	D4	D3	D2	D1	D0

L3 settings

L3 REGISTER MAPPING

Table 8 L3 register mapping including default register settings; bits D15 to D8

REG NUM	FUNCTION	D15	D14	D13	D12	D11	D10	D9	D8
Writable and readable registers									
00H	system setting			POLinv DAC	POLinv ADC	PON DAC		SC1	SC0
		0	0	0	0	1	0	1	1
11H	MASTER volume control	0	0	0	0	0	0	0	0
12H	silence detector							ADC_out Select1	ADC_out Select0
	ADC output select	0	0	0	0	0	0	0	0
13H	ADC volume	VC-AD7	VC-AD6	VC-AD5	VC-AD4	VC-ADC3	VC-ADC2	VC-ADC1	VC-ADC0
	I^2S-bus mixer volume	0	0	0	0	0	0	0	0
14H	mute						MTM	MT-ADC	MT-IIS
	de-emphasis	0	0	0	0	0	0	0	0
20H	ADC settings	PON-R ADC	PON-L ADC	PON BIAS				DCfilt1	DCfilt0
		1	1	1	0	0	0	0	0
7FH	software reset	writing this sets all controllable settings to their default values							
Readable registers									
18H	interpolator								

Table 9 L3 register mapping including default register settings; bits D7 to D0

REG NUM	FUNCTION	D7	D6	D5	D4	D3	D2	D1	D0
Writable and readable registers									
00H	system setting			SFOR3	SFOR2	SFOR1	SFOR0		MIX
		0	1	0	0	0	0		0
11H	MASTER volume control	VC7	VC6	VC5	VC4	VC3	VC2	VC1	VC0
		0	0	0	0	0	0	0	0
12H	silence detector						SDET1	SDET0	SDET_on
	ADC output select	0	0	0	0	0	0	0	1
13H	ADC volume	VC-IIS7	VC-IIS16	VC-IIS5	VC-IIS4	VC-IIS3	VC-IIS2	VC-IIS1	VC-IIS0
	I^2S-bus mixer volume	0	0	0	0	0	0	0	0
14H	mute						DE2	DE1	DE0
	de-emphasis	0	0	0	0	0	0	0	0
20H	ADC settings	PGAL3	PGAL2	PGAL1	PGAL0	PGAR3	PGAR2	PGAR1	PGAR0
		0	0	0	0	0	0	0	0
7FH	software reset								
Readable registers									
18H	interpolator			SDET-IIS-R	SDET-IIS-L		MTM state	MT-ADC state	MT-IIS state

Polarity control of the DAC

A 1-bit value to program the DAC output polarity.

Table 10 Polarity control of the DAC

POLINV DAC	FUNCTION
0	DAC output is not inverting
1	DAC output is inverting

Polarity control of the ADC

A 1-bit value to program the ADC output polarity.

Table 11 Polarity control of the ADC

POLINV ADC	FUNCTION
0	ADC output is not inverting
1	ADC output is inverting

Power control of the DAC

A 1-bit value to program the power setting of the DAC.

Table 12 Power control of the DAC

PON DAC	FUNCTION
0	DAC powered down
1	DAC powered up

System clock settings

A 2-bit value (SC1 and SC0) to select the required external clock frequency (see Table 13).

Table 13 System clock frequency settings

SC1	SC0	FUNCTION
0	0	$512f_s$
0	1	$384f_s$
1	0	$256f_s$
1	1	

Data input format

A 3-bit value (SFOR3 to SFOR0) to select the required data format (see Table 14).

Table 14 : Data input format settings

SFOR3	SFOR2	SFOR1	SFOR0	FUNCTION
0	0	0	0	I^2S-bus
0	0	0	1	LSB-justified; 16 bits
0	0	1	0	LSB-justified; 18 bits
0	0	1	1	LSB-justified; 20 bits
0	1	0	0	MSB-justified
0	1	0	1	MSB-justified output/LSB-justified 16 bits input
0	1	1	0	MSB-justified output/LSB-justified 18 bits input
0	1	1	1	MSB-justified output/LSB-justified 20 bits input
1	0	0	0	MSB justified output/ LSB-justified 24 bits input
1	0	0	1	LSB justified, 24 bits
1	:	:	:	other codes are reserved for future use

Mixer setting

A 1-bit value to enable or disable the digital mixer (for mixing the ADC signal to the playback signal).

Table 15 Mixer setting

MIX	FUNCTION
0	mixer disabled
1	mixer enabled

ADC OUTPUT SELECTOR

A 1-bit value to set the ADC I^2S-bus output signal, being either before or after the mixer volume control and mute.

Table 16 ADC output select

ADC_OUT_SELECT1	ADC_OUT_SELECT0	FUNCTION
0	0	digital output before the ADC volume and mute
0	1	digital output after ADC volume control and mute
1	0	digital output after the mixer
1	1	not used

MASTER VOLUME CONTROL

An 8-bit value to program the left and right channel master volume attenuation (VC5 to VC0). The range is 0 dB to –∞ dB in steps of 0.25 dB (see Table 17).

Table 17 Master volume control: volume settings interpolator core

VC7	VC6	VC5	VC4	VC3	VC2	VC1	VC0	VOLUME (dB)
0	0	0	0	0	0	0	0	0
0	0	0	0	0	1	0	0	0
0	0	0	0	0	1	0	1	–0.25
0	0	0	0	0	1	1	0	–0.5
0	0	0	0	0	1	1	1	–0.75
0	0	0	0	1	0	0	0	–1
								:
1	1	0	0	1	1	0	0	–50
1	1	0	1	0	0	0	0	–52
1	1	0	1	0	1	0	0	–54
1	1	0	1	1	0	0	0	–57
1	1	0	1	1	1	0	0	–60
1	1	1	0	0	0	0	0	–66
1	1	1	0	0	1	0	0	-∞
1	1	1	1	1	1	1	1	-∞

SILENCE DETECTOR SAMPLES SETTING

A 2-bit value to set the number of samples for the digital silence detector circuit.

Table 18 Silence detector settings

SDET1	SDET0	FUNCTION
0	0	3200 samples
0	1	4800 samples
1	0	9600 samples
1	1	19600 samples

SILENCE DETECTOR ENABLE SETTING

A 1-bit value to enable or disable the digital silence detection signal.

Table 19 Silence detector control setting

SDET_ON	FUNCTION
0	silence detector disabled
1	silence detector enabled

ADC AND IIS MIXER VOLUME CONTROL

An 8-bit value to program the volume ADC attenuation. The range is 0 dB to –∞ dB in steps of 0.25 dB (see Table 20).

Table 20 Mixer volume settings.

VC-AD7 VC-IIS7	VC-AD6 VC-IIS6	VC-AD5 VC-IIS5	VC-AD4 VC-IIS4	VC-AD3 VC-IIS3	VC-AD2 VC-IIS2	VC-AD1 VC-IIS1	VC-AD0 VC-IIS0	VOLUME (dB)
0	0	0	0	0	0	0	0	0
0	0	0	0	0	1	0	0	0
0	0	0	0	0	1	0	1	–0.25
0	0	0	0	0	1	1	0	–0.5
0	0	0	0	0	1	1	1	–0.75
0	0	0	0	0	1	0	0	–1
								:
1	0	1	1	0	1	0	0	–44
1	0	1	1	1	0	0	0	–46
1	0	1	1	1	1	0	0	–48
1	1	0	0	0	0	0	0	–51
1	1	0	0	0	1	0	0	–54
1	1	0	0	1	0	0	0	–60
1	1	0	0	1	1	0	0	–∞
1	1	1	1	1	1	1	1	–∞

MASTER MUTE CONTROL

A 1-bit value to enable the digital master mute. This mute control signal mutes the master playback signal after mixing.

Table 21 Master mute

MTM	FUNCTION
0	no muting
1	muting

MIXER MUTE CONTROL

Two 1-bit values to enable the digital mutes of the mixer. These signals can be used to independently mute the I^2S-bus playback signal or the signal coming from the ADC. These mute functions can only be used in the mixer mode when the MIX bit is set HIGH.

The MT-ADC and MT-IIS bits can also be used to select either the I^2S-bus or the ADC signal for playback.

DC FILTER

Table 22 Mixer mute

MT-ADC/MT-IIS	FUNCTION
0	no muting
1	muting

DIGITAL DE-EMPHASIS

A 2-bit value to enable the digital de-emphasis filter.

Table 23 De-emphasis settings

DE2	DE1	DE0	FUNCTION
0	0	0	no de-emphasis
0	0	1	de-emphasis; 32 kHz
0	1	0	de-emphasis; 44.1 kHz
0	1	1	de-emphasis; 48 kHz
1	0	0	de-emphasis; 96 kHz
1	0	1	not used
1	1	0	
1	1	1	

A 1-bit value to enable the digital DC filter (see Table 24).

Table 24 DC filtering; note 1

DC1	DC0	FUNCTION
0	0	no DC filtering
0	1	DC filtering with –3 dB at 3 Hz
1	0	DC filtering with –3 dB at 100 Hz
1	1	DC filtering with –3 dB at 200 Hz

Note

1. The corner frequencies of the DC filter are given assuming 44.1 kHz sampling frequency.

ADC POWER CONTROL

Three 1-bit value to disable the ADC to reduce power consumption.

Table 25 Power control settings

PON BIAS	PON-R ADC	PON-L ADC	FUNCTION
0	x	x	both ADC channels off and also bias block turned off
1	0	1	ADC left channel powered on, bias block turned on
1	1	0	ADC right channel powered on, bias block turned on
1	1	1	both left and right ADC channels enabled, bias block turned on

PGA GAIN SETTINGS

Two 4-bit values to program the PGA gain settings. The PGA settings can be set individually for the left and the right channels.

Table 26 PGA gain control settings

PGAL3, PGAR3	PGAL2, PGAR2	PGAL1, PGAR1	PGAL0, PGAR0	FUNCTION
0	0	0	0	0 dB gain
0	0	0	1	3 dB gain
0	0	1	0	6 dB gain
0	0	1	1	9 dB gain
0	1	0	0	12 dB gain
0	1	0	1	15 dB gain
0	1	1	0	18 dB gain
0	1	1	1	21 dB gain
1	0	0	0	24 dB gain
1	:	:	:	not used

L3 readable registers

The L3 interface also contains some read-only registers in which system status can be read. The read-only registers are given in Table 27. It should be noted that all bits mentioned in the table are active HIGH.

Table 27 Description of the bits from the READ ONLY registers

NAME	FUNCTION
SDET-IIS-L	signals whether the output data of the I^2S-bus left channel is digitally zero
SDET-IIS-R	signals whether the output data of the I^2S-bus right channel is digitally zero
MTM_state	signals whether there is master mute
MT-ADC_state	signals whether there is mute in the ADC channel
MT-IIS_state	signals whether there is mute in the I^2S-bus input channel

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134). All voltages referenced to ground; $V_{DDD} = V_{DDA} = V_{DDO} = 3$ V; $T_{amb} = 25$ °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DDD}	digital supply voltage	note 1	–	5.0	V
$T_{xtal(max)}$	maximum crystal temperature		–	150	°C
T_{stg}	storage temperature		–65	+125	°C
T_{amb}	ambient temperature		–40	+85	°C
V_{es}	electrostatic handling voltage	human body model; note 2			
		machine model; note 2			

Note

1. All V_{DD} and V_{SS} connections must be made to the same power supply.
2. According to JEDEC II specification.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	110	K/W

DC CHARACTERISTICS

$V_{DDD} = V_{DDA} = V_{DDO} = 3.0$ V; $T_{amb} = 25$ °C; $R_L = 5$ kΩ; note 1; all voltages referenced to ground; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
$V_{DDA(ADC)}$	ADC analog supply voltage		2.4	3.0	3.6	V
$V_{DDA(DAC)}$	DAC analog supply voltage		2.4	3.0	3.6	V
V_{DDD}	digital supply voltage		2.4	3.0	3.6	V
$I_{DDA(ADC)}$	ADC analog supply current	operating mode	–	10	–	mA
		ADC power-down	–	100	–	μA
$I_{DDA(DAC)}$	DAC analog supply current	operating mode	–	4	-	mA
		DAC power-down	–	50	–	μA
$I_{DDO(DAC)}$	DAC operational amplifier supply current	operating mode	–	2.5	–	mA
		DAC power-down	–	200	–	
I_{DDD}	digital supply current	operating mode	–	5	–	mA
		ADC and DAC power-down	–	300	–	μA
Digital input pins (5 V tolerant TTL compatible)						
V_{IH}	HIGH-level input voltage		2.0	–	5.0	V
V_{IL}	LOW-level input voltage		–0.5	–	0.8	V
$V_{IH(th)}$	HIGH-level threshold input voltage		1.3	–	1.9	V
$V_{IL(th)}$	LOW-level threshold input voltage		0.9	–	1.35	V
V_{hys}	Schmitt trigger hysteresis		0.4	–	0.7	V
$\lvert I_{LI} \rvert$	input leakage current		–	–	10	μA
C_i	input capacitance		–	–	10	pF
V_{IL}	LOW-level input voltage		–0.5	–	$0.2V_{DDD}$	V
Digital output pins						
V_{OH}	HIGH-level output voltage	$I_{OH} = -2$ mA	$0.85V_{DDD}$	–	–	V
V_{OL}	LOW-level output voltage	$I_{OL} = 2$ mA	–	–	0.4	V
Analog-to-digital converter						
$V_{ref(A)}$	reference voltage	referenced to $V_{SSA(ADC)}$	$0.45V_{DDA}$	$0.5V_{DDA}$	$0.55V_{DDA}$	V
$R_{o(refA)}$	$V_{ref(A)}$ reference output resistance		–	24	–	kΩ
R_i	input resistance	$f_i = 1$ kHz	–	9.8	–	kΩ
C_i	input capacitance		–	20	–	pF
Digital-to-analog converter						
$V_{ref(D)}$	reference voltage	referenced to $V_{SSA(DAC)}$	$0.45V_{DDA}$	$0.5V_{DDA}$	$0.55V_{DDA}$	V
$R_{o(refD)}$	$V_{ref(D)}$ reference output resistance		–	28	–	kΩ
R_o	DAC output resistance		–	0.13	3.0	Ω

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$I_{o(max)}$	maximum output current	(THD + N)/S < 0.1% R_L = 800Ω	–	3.5	–	mA
R_L	load resistance		3	–	–	kΩ
C_L	load capacitance	note 2	–	–	200	pF

Notes

1. All power supply pins (V_{DD} and V_{SS}) must be connected to the same external power supply unit.
2. When higher capacitive loads must be driven, a 100 Ω resistor must be connected in series with the DAC output in order to prevent oscillations in the output operational amplifier.

AC CHARACTERISTICS (ANALOG)

V_{DDD} = V_{DDA} = V_{DDO} = 3.0 V; f_i = 1 kHz; f_s = 44.1 kHz; T_{amb} = 25 °C; R_L = 5 kΩ; all voltages referenced to ground; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Analog-to-digital converter						
$V_{i(rms)}$	input voltage (RMS value)	note 1	–	1.0	–	V
ΔV_i	unbalance between channels		–	0.1	–	dB
(THD + N)/S	total harmonic distortion-plus-noise to signal ratio	at 0 dB				
		f_s = 44.1 kHz	–	–85	–	dB
		f_s = 96 kHz	–	–81	–	dB
		at –60 dB; A-weighted				
		f_s = 44.1 kHz	–	–37	–	dB
		f_s = 96 kHz	–	–35	–	dB
S/N	signal-to-noise ratio	V_i = 0 V; A-weighted				
		f_s = 44.1 kHz	–	97	–	dB
		f_s = 96 kHz	–	95	–	dB
α_{cs}	channel separation		–	100	–	dB
PSRR	power supply rejection ratio	f_{ripple} = 1 kHz; $V_{ripple(p-p)}$ = 1%	–	30	–	dB
Analog-to-digital converter using PGA						
$V_{i(rms)}$	input voltage (RMS value)	0 dB setting	–	1000	–	mV
		3 dB setting	–	708	–	mV
		6 dB setting	–	500	–	mV
		9 dB setting	–	354	–	mV
		12 dB setting	–	250	–	mV
		15 dB setting	–	178	–	mV
		18 dB setting	–	126	–	mV
		21 dB setting	–	89	–	mV
		24 dB setting	–	63	–	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
(THD + N)/S	total harmonic distortion-plus-noise to signal ratio	f_s = 44.1 kHz; at 0 dB				
		0 dB setting	–	–85	–	dB
		3 dB setting	–	tbf	–	dB
		6 dB setting	–	tbf	–	dB
		9 dB setting	–	tbf	–	dB
		12 dB setting	–	tbf	–	dB
		15 dB setting	–	tbf	–	dB
		18 dB setting	–	tbf	–	dB
		21 dB setting	–	tbf	–	dB
		24 dB setting	–	tbf	–	dB
		f_s = 44.1 kHz; at –60 dB; A-weighted				
		0 dB setting	–	–37	–	dB
		3 dB setting	–	tbf	–	dB
		6 dB setting	–	tbf	–	dB
		9 dB setting	–	tbf	–	dB
		12 dB setting	–	tbf	–	dB
		15 dB setting	–	tbf	–	dB
		18 dB setting	–	tbf	–	dB
		21 dB setting	–	tbf	–	dB
		24 dB setting	–	tbf	–	dB
S/N	signal-to-noise ratio	V_i = 0 V; A-weighted; at 44.1 kHz	–	97	–	dB
Digital-to-analog converter						
$V_{o(rms)}$	output voltage (RMS value)		–	900	–	mV
ΔV_o	unbalance between channels		–	0.1	–	dB
(THD + N)/S	total harmonic distortion-plus-noise to signal ratio	at 0 dB				
		f_s = 44.1 kHz	–	–85	–	dB
		f_s = 96 kHz	–	–80	–	dB
		at –60 dB; A-weighted				
		f_s = 44.1 kHz	–	–37	–	dB
		f_s = 96 kHz	–	–35	–	dB
α_{cs}	channel separation		–	100	–	dB
S/N	signal-to-noise ratio	code = 0; A-weighted				
		f_s = 44.1 kHz	–	100	–	dB
		f_s = 96 kHz	–	98	–	dB
		A-weighted; digital silence	–	110	–	dB
PSRR	power supply rejection ratio	f_{ripple} = 1 kHz; $V_{ripple(p-p)}$ = 1%	–	60	–	dB

Note

1. The performance figures and input voltage given are with the PGA gain set to 0 dB.

AC CHARACTERISTICS (DIGITAL)

$V_{DDD} = V_{DDA} = V_{DDO} = 2.7$ to 3.6 V; $T_{amb} = -40$ to +85 °C; $R_L = 5\ k\Omega$; all voltages referenced to ground; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
System clock timing; see Fig.10						
T_{sys}	system clock cycle	$f_{sys} = 256f_s$, note 1	36	88	781	ns
		$f_{sys} = 384f_s$, note 1	24	59	520	ns
		$f_{sys} = 512f_s$, note 2	36	44	390	ns
t_{CWL}	f_{sys} LOW level pulse width	$f_{sys} < 19.2$ MHz	$0.30T_{sys}$	–	$0.70T_{sys}$	ns
		$f_{sys} \geq 19.2$ MHz	$0.40T_{sys}$	–	$0.60T_{sys}$	ns
t_{CWH}	f_{sys} HIGH level pulse width	$f_{sys} < 19.2$ MHz	$0.30T_{sys}$	–	$0.70T_{sys}$	ns
		$f_{sys} \geq 19.2$ MHz	$0.40T_{sys}$	–	$0.60T_{sys}$	ns
t_r	rise time		–	–	20	ns
t_f	fall time		–	–	20	ns
Serial input/output data timing; see Fig.11						
t_{BCK}	bit clock period		$1/128f_s$	–	–	ns
t_{BCKH}	bit clock HIGH time		30	–	–	ns
t_{BCKL}	bit clock LOW time		30	–	–	ns
t_r	rise time		–	–	20	ns
t_f	fall time		–	–	20	ns
$t_{s(DATAI)}$	data input set-up time		20	–	–	ns
$t_{h(DATAI)}$	data input hold time		0	–	–	ns
$t_{d(DATAO-BCK)}$	data output delay time (from BCK falling edge)		–	–	80	ns
$t_{d(DATAO-WS)}$	data output delay time (from WS edge)	MSB-justified format	–	–	80	ns
$t_{h(DATAO)}$	data output hold time		0	–	–	ns
$t_{s(WS)}$	word select set-up time		20	–	–	ns
$t_{h(WS)}$	word select hold time		10	–	–	ns
Address and data transfer mode timing; see Fig 6						
$T_{cy(CLK)(L3)}$	L3CLOCK cycle time		500	–	–	ns
$t_{CLK(L3)H}$	L3CLOCK HIGH period		250	–	–	ns
$t_{CLK(L3)L}$	L3CLOCK LOW period		250	–	–	ns
$t_{su(L3)A}$	L3MODE set-up time	address mode	190	–	–	ns
$t_{h(L3)A}$	L3MODE hold time	address mode	190	–	–	ns
$t_{su(L3)DA}$	L3MODE set-up time	data transfer mode	190	–	–	ns
$t_{h(L3)DA}$	L3MODE hold time	data transfer mode	190	–	–	ns
$t_{su(L3)DAA}$	L3DATA set-up time	data transfer mode and address mode	190	–	–	ns
$t_{h(L3)DAA}$	L3DATA hold time	data transfer mode and address mode	30	–	–	ns
t_{halt}	L3MODE halt time		190	–	–	ns

Notes:

1. Sampling range from 16 to 100 kHz is supported, with f_s = 44.1 kHz typical.
2. Sampling range from 16 to 55 kHz is supported, with f_s = 44.1 kHz typical.

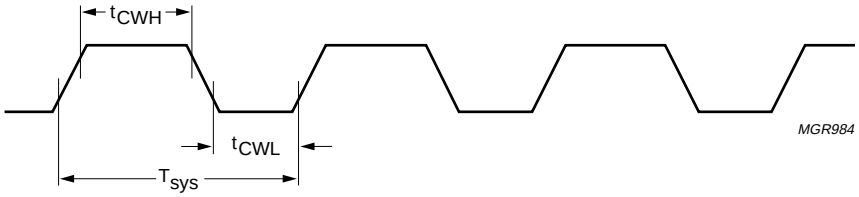


Fig.10 System clock timing.

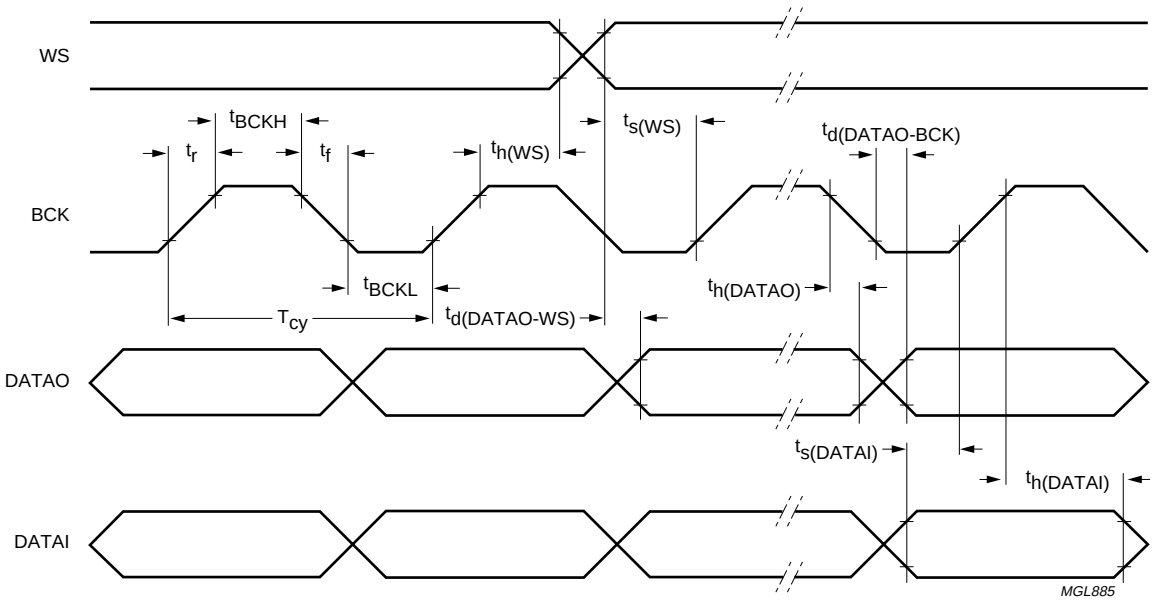


Fig.11 Serial interface timing.

APPLICATION INFORMATION

The application information as given in Fig.12, is an optimum application environment. Simplification is possible at the cost of some performance degradation. The following notes apply:

- The capacitors at the output of the DAC can be reduced. It should be noted that the cut-off frequency of the DC filter also changes.
- The capacitors at the input of the ADC can also be reduced. It should be noted that the cut-off frequency of the capacitor with the 12 kΩ input resistance of the ADC will also change.

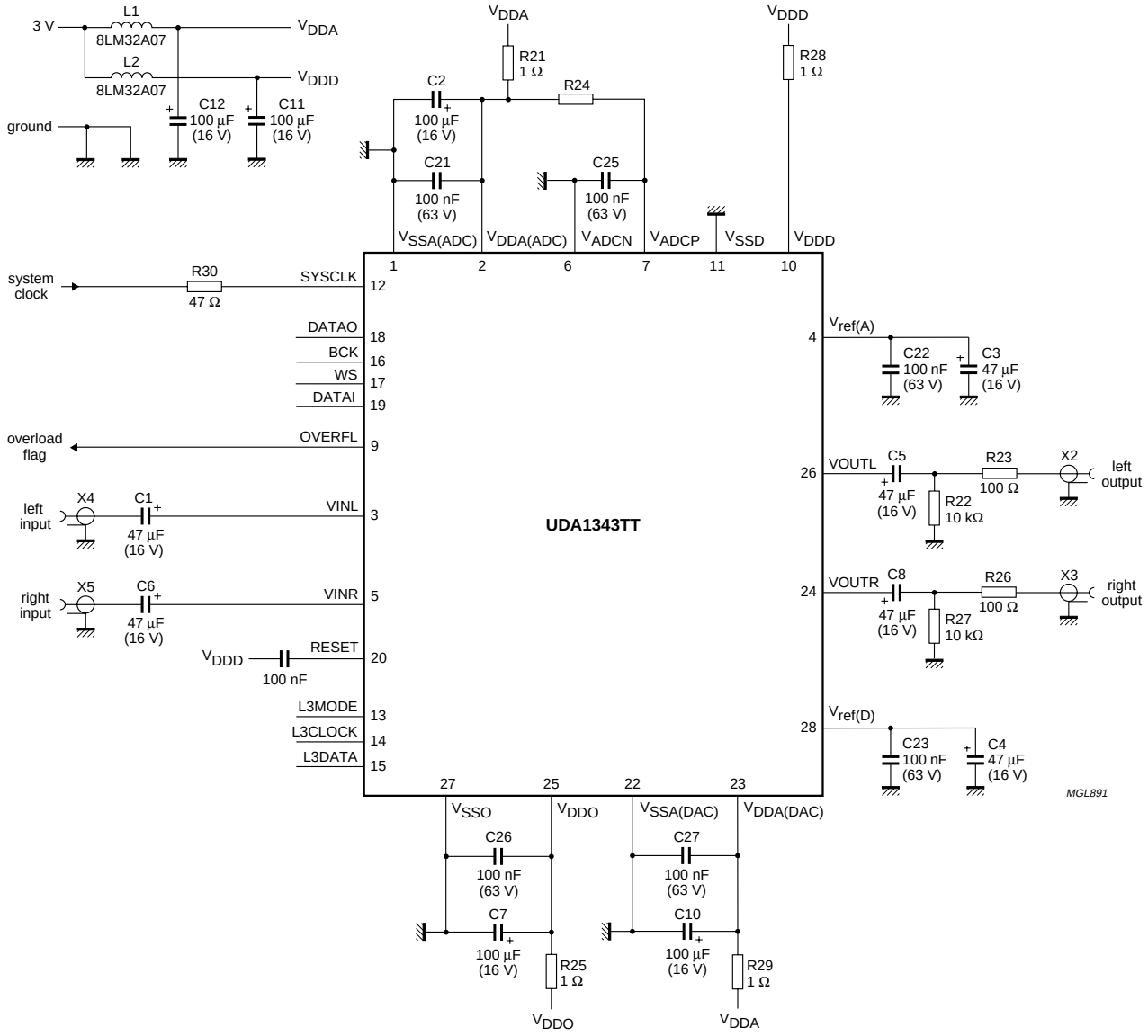
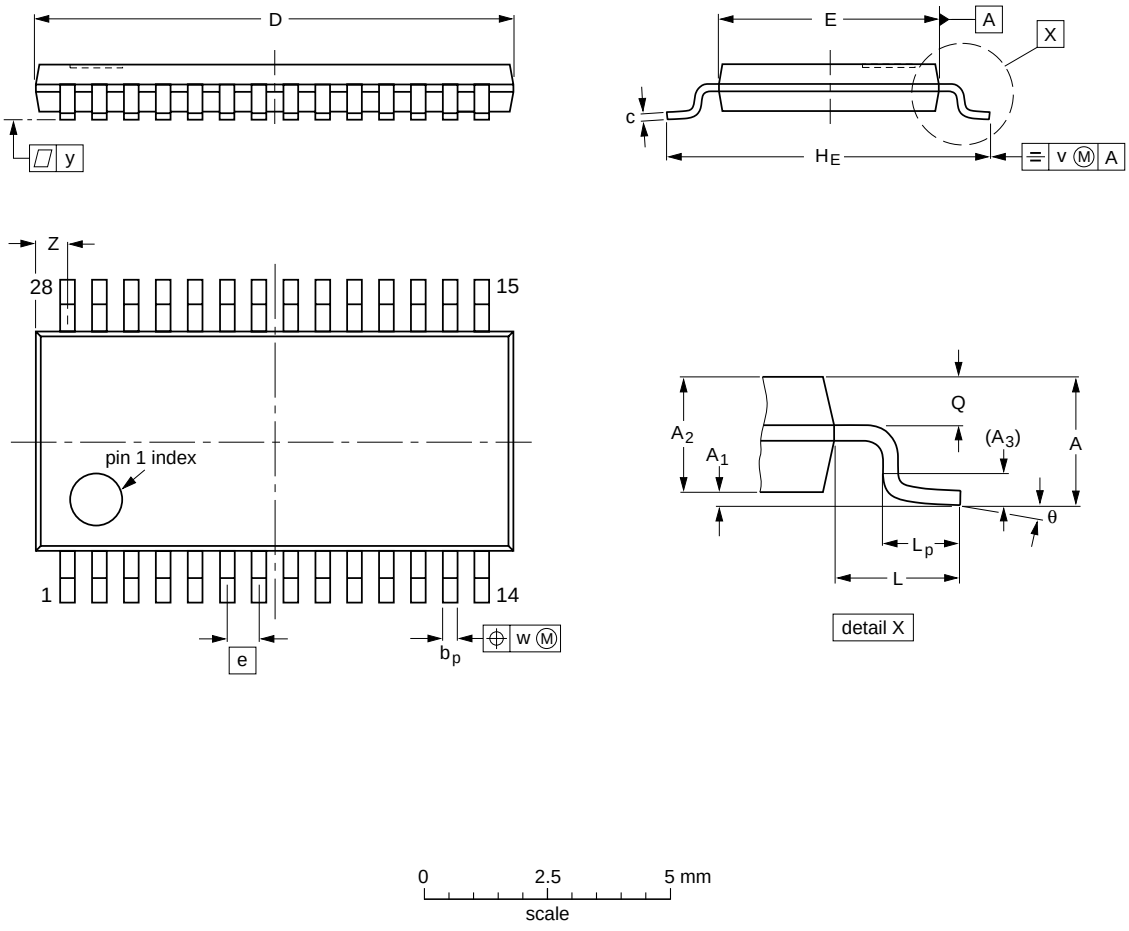


Fig.12 Application diagram.

PACKAGE OUTLINE

TSSOP28: plastic thin shrink small outline package; 28 leads; body width 4.4 mm **SOT361-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	9.8 9.6	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.8 0.5	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT361-1		MO-153				~~95-02-04~~ 99-12-27

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 230 °C.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW(1)
BGA, LFBGA, SQFP, TFBGA	not suitable	suitable
HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, SMS	not suitable(2)	suitable
PLCC(3), SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended(3)(4)	suitable
SSOP, TSSOP, VSO	not recommended(5)	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

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