

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

**TC74VHCT240AF, TC74VHCT240AFW, TC74VHCT240AFT**  
**TC74VHCT244AF, TC74VHCT244AFW, TC74VHCT244AFT**

**OCTAL BUS BUFFER**

**TC74VHCT240AF / AFW / AFT INVERTED, 3 - STATE OUTPUTS**

**TC74VHCT244AF / AFW / AFT NON - INVERTED, 3 - STATE OUTPUTS**

(Note) The JEDEC SOP (FW) is not available in Japan.

The TC74VHCT240A and 244A are advanced high speed CMOS OCTAL BUS BUFFERS fabricated with silicon gate C<sup>2</sup>MOS technology. They achieve the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

The TC74VHCT240A is an inverting 3 - state buffer having two active - low output enables. The TC74VHCT244A is a non - inverting 3 - state buffer, and has two active - low output enables.

These devices are designed to be used with 3 - state memory address drivers, etc.

The input voltage are compatible with TTL output voltage.

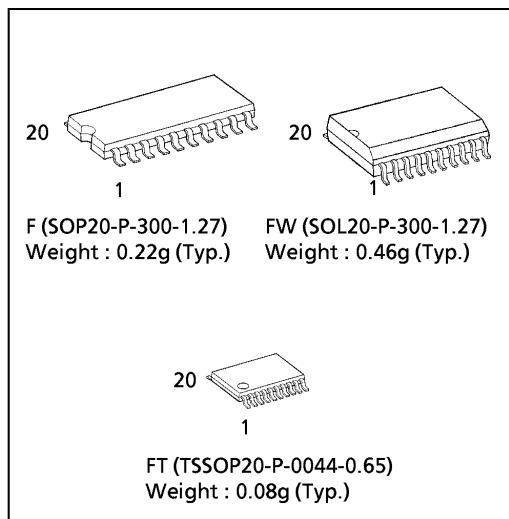
These devices may be used as a level converter for interfacing 3.3V to 5V system.

Input protection and output circuit ensure that 0 to 5.5V can be applied to the input and output\*1 pins without regard to the supply voltage. These structure prevents device destruction due to mismatched supply and input / output voltages such as battery back up, hot board insertion, etc.

\*1: output in off-state

**FEATURES :**

- High Speed..... $t_{pd} = 5.6ns$ (typ.) at  $V_{CC} = 5V$
- Low Power Dissipation..... $I_{CC} = 4\mu A$ (Max.) at  $T_a = 25^\circ C$
- Compatible with TTL outputs ...  $V_{IL} = 0.8 V$  (Max.)  
 $V_{IH} = 2.0 V$  (Min.)
- Power Down Protection is provided on all inputs and outputs
- Balanced Propagation Delays..... $t_{pLH} \approx t_{pHL}$
- Low Noise ..... $V_{OLP} = 1.1V$  (Max.)
- Pin and Function Compatible with the 74 series (74AC / HC / F / ALS / LS etc.) 240 / 244 type.

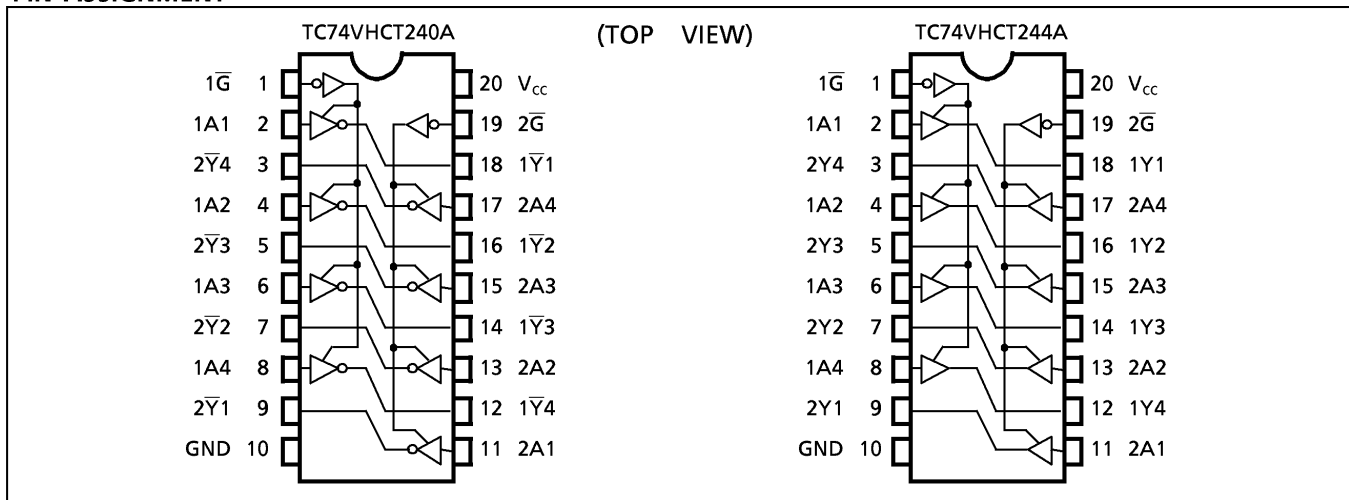


**TRUTH TABLE**

INPUTS		OUTPUTS	
$\bar{G}$	$A_n$	$Y_n$	$\bar{Y}_n$
L	L	L	H
L	H	H	L
H	X	Z	Z

X : Don't Care  
 Z : High Impedance  
 $Y_n$  : TC74VHCT244A  
 $\bar{Y}_n$  : TC74VHCT240A

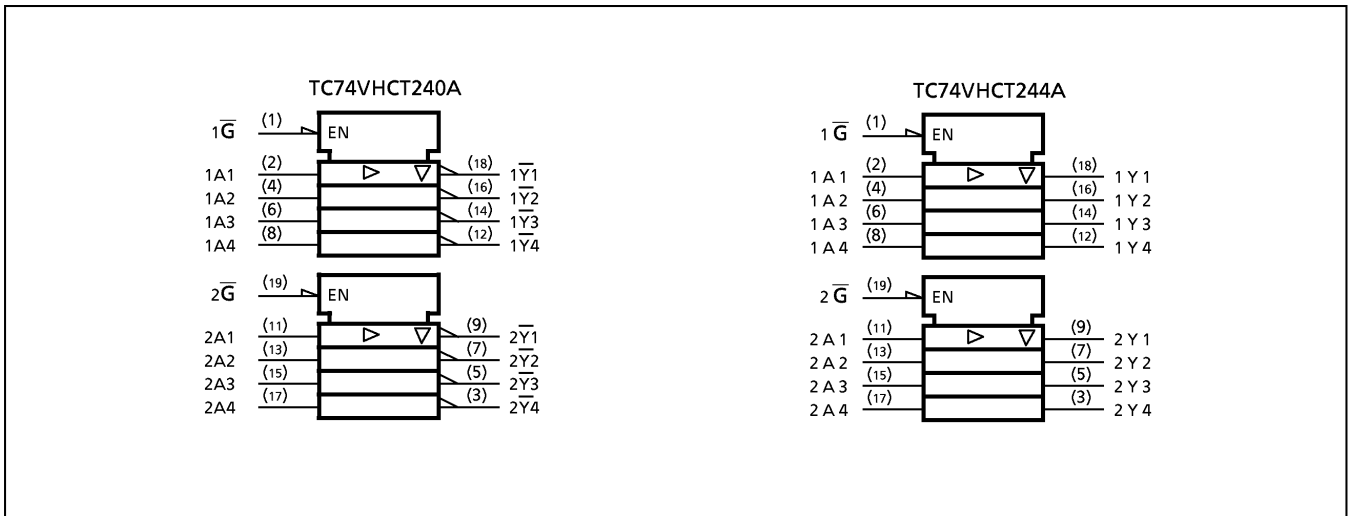
**PIN ASSIGNMENT**



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**IEC LOGIC SYMBOL**



**ABSOLUTE MAXIMUM RATINGS**

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	$V_{CC}$	-0.5~7.0	V
DC Input Voltage	$V_{IN}$	-0.5~7.0	V
DC Output Voltage	$V_{OUT}$	-0.5~7.0 (Note 1)	V
		-0.5~ $V_{CC} + 0.5$ (Note 2)	
Input Diode Current	$I_{IK}$	-20	mA
Output Diode Current	$I_{OK}$	±20 (Note 3)	mA
DC Output Current	$I_{OUT}$	±25	mA
DC Vcc/Ground Current	$I_{CC}$	±75	mA
Power Dissipation	$P_D$	180	mW
Storage Temperature	$T_{stg}$	-65~150	°C

(Note 1) Output in Off-State

(Note 2) High or Low State.  $I_{OUT}$  absolute maximum rating must be observed.

(Note 3)  $V_{OUT} < GND, V_{OUT} > V_{CC}$

**RECOMMENDED OPERATING CONDITIONS**

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	$V_{CC}$	4.5~5.5	V
Input Voltage	$V_{IN}$	0~5.5	V
Output Voltage	$V_{OUT}$	0~5.5 (Note 4)	V
		0~ $V_{CC}$ (Note 5)	
Operating Temperature	$T_{opr}$	-40~85	°C
Input Rise and Fall Time	$dt / dV$	0~20	ns / V

(Note 4) Output in Off-State

(Note 5) High or Low State

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## DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	CONDITON	V <sub>CC</sub> (V)	Ta = 25°C			Ta = -40~85°C		UNIT	
				MIN.	TYP.	MAX.	MIN.	MAX.		
High - Level Input Voltage	V <sub>IH</sub>		4.5~5.5	2.0	—	—	2.0	—	V	
Low - Level Input Voltage	V <sub>IL</sub>		4.5~5.5	—	—	0.8	—	0.8	V	
High - Level Output Voltage	V <sub>OH</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -50μA	4.5	4.40	4.50	—	4.40	—	V
			I <sub>OH</sub> = -8mA	4.5	3.94	—	—	3.80	—	
Low - Level Output Voltage	V <sub>OL</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 50μA	4.5	—	0.0	0.10	—	0.10	V
			I <sub>OL</sub> = 8mA	4.5	—	—	0.36	—	0.44	
3 - State Output Off - State Current	I <sub>OZ</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> V <sub>OUT</sub> = V <sub>CC</sub> or GND	5.5	—	—	±0.25	—	±2.50	μA	
Input Leakage Current	I <sub>IN</sub>	V <sub>IN</sub> = 5.5V or GND	0~5.5	—	—	±0.1	—	±1.0		
Quiescent Supply Current	I <sub>CC</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND	5.5	—	—	4.0	—	40.0		
	I <sub>CCT</sub>	PER INPUT : V <sub>IN</sub> = 3.4V OTHER INPUT : V <sub>CC</sub> or GND	5.5	—	—	1.35	—	1.50	mA	
Output Leakage Current	I <sub>OPD</sub>	V <sub>OUT</sub> = 5.5V	0	—	—	+0.5	—	+5.0	μA	

AC ELECTRICAL CHARACTERISTICS (Input t<sub>r</sub> = t<sub>f</sub> = 3ns)

PARAMETER	SYMBOL	TEST CONDITION	V <sub>CC</sub> (V)	C <sub>L</sub> (pF)	Ta = 25°C			Ta = -40~85°C		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time (TC74VHCT240A)	t <sub>pLH</sub> t <sub>pHL</sub>		5.0 ± 0.5	15	—	5.6	7.8	1.0	9.0	ns
				50	—	6.1	8.8	1.0	10.0	
Propagation Delay Time (TC74VHCT244A)	t <sub>pLH</sub> t <sub>pHL</sub>		5.0 ± 0.5	15	—	5.4	7.4	1.0	8.5	
				50	—	5.9	8.4	1.0	9.5	
3-State Output Enable Time	t <sub>pZL</sub> t <sub>pZH</sub>	R <sub>L</sub> = 1kΩ	5.0 ± 0.5	15	—	7.7	10.4	1.0	12.0	
				50	—	8.2	11.4	1.0	13.0	
3-State Output Disable Time	t <sub>pLZ</sub> t <sub>pHZ</sub>	R <sub>L</sub> = 1kΩ	5.0 ± 0.5	50	—	8.8	11.4	1.0	13.0	
Output to Output Skew	t <sub>osLH</sub> t <sub>osHL</sub>	(Note 6)	5.0 ± 0.5	50	—	—	1.0	—	1.0	
Input Capacitance	C <sub>IN</sub>				—	4	10	—	10	
Output Capacitance	C <sub>OUT</sub>				—	9	—	—	—	
Power Dissipation Capacitance (Note 7)	C <sub>PD</sub>	TC74VHCT240A			—	19	—	—	—	
		TC74VHCT244A			—	18	—	—	—	

(Note 6) Parameter guaranteed by design.  $t_{osLH} = |t_{pLHm} - t_{pLHn}|$ ,  $t_{osHL} = |t_{pHLm} - t_{pHLn}|$

(Note 7) C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation :

$$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 8 \text{ (per bit)}$$

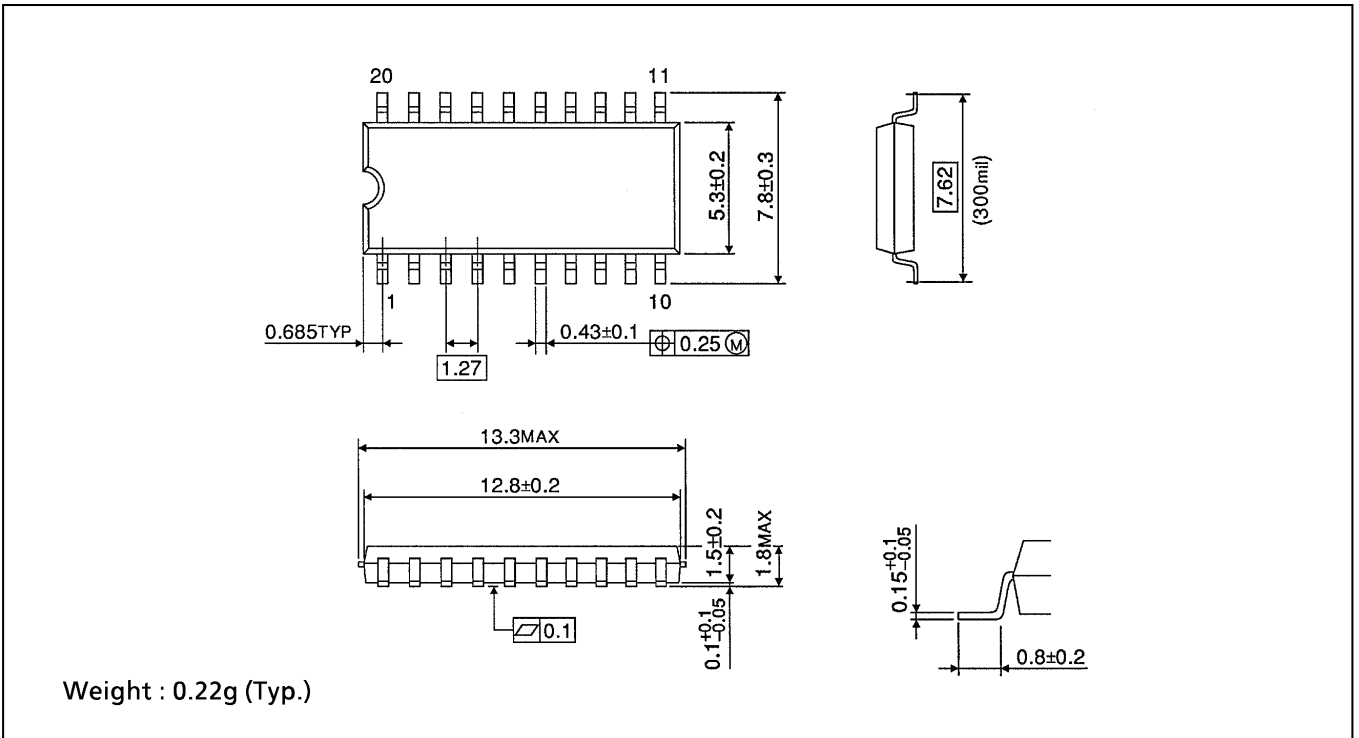
NOISE CHARACTERISTICS (Input  $t_r = t_f = 3\text{ns}$ )

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C		UNIT	
			V <sub>CC</sub> (V)	TYP.		LIMIT
Quiet Output Maximum Dynamic V <sub>OL</sub>	V <sub>OLP</sub>	C <sub>L</sub> = 50pF	5.0	0.8 (0.9)	1.0 (1.1)	V
Quiet Output Minimum Dynamic V <sub>OL</sub>	V <sub>OLV</sub>	C <sub>L</sub> = 50pF	5.0	-0.8 (-0.9)	-1.0 (-1.1)	V
Minimum High Level Dynamic Input Voltage	V <sub>IHD</sub>	C <sub>L</sub> = 50pF	5.0	—	2.0	V
Maximum Low Level Dynamic Input Voltage	V <sub>ILD</sub>	C <sub>L</sub> = 50pF	5.0	—	0.8	V

(Note) The value in ( ) only applies to JEDEC SOP (FW) devices.

**SOP 20PIN (200mil BODY) OUTLINE DRAWING (SOP20-P-300-1.27)**

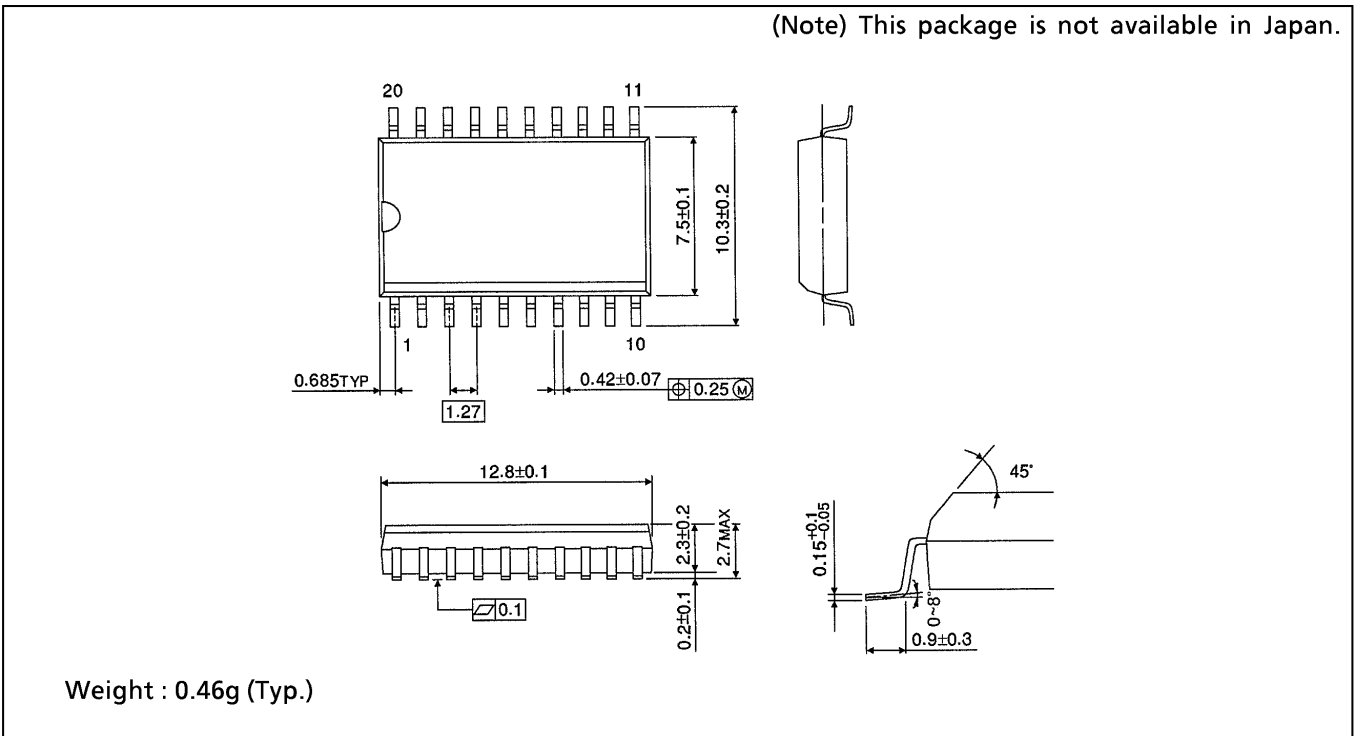
Unit in mm



**SOP 20PIN (300mil BODY) OUTLINE DRAWING (SOP20-P-300-1.27)**

Unit in mm

(Note) This package is not available in Japan.



**TSSOP 20PIN OUTLINE DRAWING (TSSOP20-P-0044-0.65)**

Unit in mm

